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Title: Discussion on Phase Noise Modeling
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1. Introduction

The increasing problem of limited bandwidth and congestion in currently used frequency bands (sub 6GHz) has become a significant limitation for wireless communication systems in recent years. In [1], it is agreed that the new radio access technology (RAT) will consider frequency ranges up to 100GHz. For high frequency spectrum above 6GHz, RF impairments such as phase noise (PN), I/Q imbalance and PA non-linearity will be limiting factors for the performance of high frequency systems. In this contribution we mainly address phase noise, which is caused by imperfect oscillator, in the context of the new RAT with a focus on above-6GHz scenarios where phase noise induces much more difficult than in sub-6GHz scenarios.

In RAN1#85 meeting, the following agreements on phase noise were achieved [2]:

- The PN modeling in TRP is FFS.
- Realistic PN model should consider total oscillator PSD including the impact of reference clock, loop filter noise and VCO sub-components. (e.g. phase-locked loop (PLL)-based model, multi-pole/zero model)
- Each company should provide the model and the parameters used for the evaluation.

Although several PN models have been proposed in [2], it is agreed that other PN model is not precluded. In this contribution, a PN model in TRP based on realistic measurement is proposed and then compared with PN models provided in [2]. Furthermore, we consider a possible PN reduction method for high frequency systems that can be used to significantly reduce the PN within loop bandwidth (BW) and thereby, reduce the PN-induced common phase error (CPE).

2. Phase Noise Measurement/Modeling

■ Proposed phase noise model

Currently there are mainly two types of PN models proposed in 3GPP by now [2], i.e., phase-locked loop (PLL)-based model [3] [4] and multi-pole/zero model [5] (with one-pole model [6] and one-pole-one-zero model [7] as its special cases). The multi-pole/zero model is simply a pure mathematical fitting by adjusting its multiple pole and zero values for each realistic PSD curve of PN it intends to fit, without any physical interpretation. On the other hand, PLL-based model has clear physical representation and has been widely adopted in the literature [8]. Therefore in the following we will mainly consider PLL-based model and then analyze its shortcomings. Finally, a filtered version of PLL-based model is proposed by incorporating noise gains for Ref and PLL.

According to the PLL phase noise model defined in [9], the PSD of the phase noise can be expressed by:

$$S_{Total}(f) = \begin{cases} S_{Ref}(f) + S_{PLL}(f), & \text{when } f \leq \text{loop BW} \\ S_{VCO_v2}(f) + S_{VCO_v3}(f), & \text{when } f > \text{loop BW} \end{cases} \quad (1)$$

where

$$S_{Ref/PLL/VCO_v2/VCO_v3} = PSD0 \cdot \left[\frac{1+(f/f_c)^k}{1+f^k} \right] \text{ (dB)} \quad (2)$$

$$PSD0 = FOM + 20 \log f_c - 10 \log \left(\frac{P}{1 \text{ mW}} \right) \text{ (dB)} \quad (3)$$

In (3), FOM is the figure of merit, f_c is the carrier frequency and P is the consumed power.

This expression (1) is in fact oversimplified based on two assumptions:

- 1). The first assumption is that the sum of $S_{Ref}(f)$ and $S_{PLL}(f)$ at loop bandwidth (Bw) is equal to the sum of $S_{VCO_v2}(f)$ and $S_{VCO_v3}(f)$. Actually the phase noise of VCO at the stop frequency of the loop is much better than that of the reference and PLL chip. So usually there will be a gap between two parts of the lines described by equation (1) and the gap may be about 10-20 dB.
- 2). The second assumption is that there are no noise gains for Ref and PLL. In fact, the noise gains for Ref and PLL are big enough and therefore cannot be ignored. And for equation (3) the **PSD0** can be obtained from vendors, so the equation (3) is no longer used in this contribution.

To compensate this mismatch, we make some corrections on (1) as follows:

$$S_{Total}(f) = (S_{Ref}(f) + S_{PLL}(f)) \cdot W(f) + (S_{VCOv2}(f) + S_{VCOv3}(f)) \cdot W(f)/G(f) \quad (4)$$

where

$$S_{Ref/PLL/VCO_v2/VCO_v3} = PSD0 \cdot \left[\frac{1+(f/f_c)^k}{1+f^k} \right] \text{ (dB)} \quad (5)$$

$W(f)$ represents the closed loop gain of PLL and $G(f)$ is the forward loop gain.

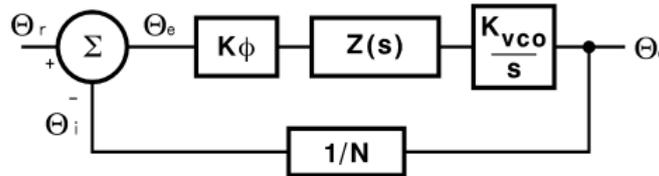


Fig.1. Linear model for PLL loop

The linear model of a PLL is shown in Fig. 1, and according to this model we can define the equations for the phase transfer function as follows:

$$\text{Forward loop gain} = G(s) = \frac{\theta_o}{\theta_e} = \frac{K\phi Z(s)Kvco}{s} \quad (6)$$

$$\text{Reverse loop gain} = H(s) = \frac{\theta_i}{\theta_o} = \frac{1}{N} \quad (7)$$

$$\text{Open loop gain} = H(s)G(s) = \frac{\theta_i}{\theta_e} = \frac{K\phi Z(s)Kvco}{Ns} \quad (8)$$

$$\text{Closed loop gain} = W(s) = \frac{\theta_o}{\theta_r} = \frac{G(s)}{1+H(s)G(s)} \quad (9)$$

where $K\phi$ is the phase detector/charge pump constant, which represents the phase difference between the current output and input; $Kvco$ is VCO tuning voltage constant, which represents the tuning ratio of frequency and voltage; N is the main divider ratio, which represents the ratio of carrier frequency and phase detector input frequency; $Z(s)$ is the impedance of the loop filter; $K\phi$, $Kvco$ and N are constant numbers, which will not affect the shape of $W(s)$ effectively. When the loop filter order, loop Bw and phase margin are set, the shape of the close loop gain is also set, no matter what the values of ϕ , $Kvco$ and N are. N only decides the amplitude of close loop gain, and so is the noise gain of VCO.

■ Model verification

For verification of this model, we check this model with a commercial design. The specification of this design is followed as:

Table 1: Specifications for proposed phase noise models

| | BS, Loop Bw = 30kHz | | | |
|-----------|---------------------|----------|-------------------|-------------------|
| | REF clk | PLL | VCO V2 | VCO V3 |
| Part type | Serdes | HMCXXX | RFVCXXX | |
| FOM | -275 ^① | -221 | -217 ^① | -168 ^① |
| Fz | 1.00E+03, 2.000E+04 | 4.00E+03 | 10.00E+06 | Inf |
| k | 1,1 | 0 | 2 | 3 |

① For comparison with other members' proposals, FOM is taken from PSD of datasheet. The calculation method is: $FOM = PSD - 20 \log f_c$ (dB)

The configuration of the PLL is as follows:

- Reference frequency: 30.72MHz
- VCO frequency: 15GHz

- Divider ratio N: 488.28125
- 2 order low pass loop filter: loop Bw 30kHz & Phase margin 45degree

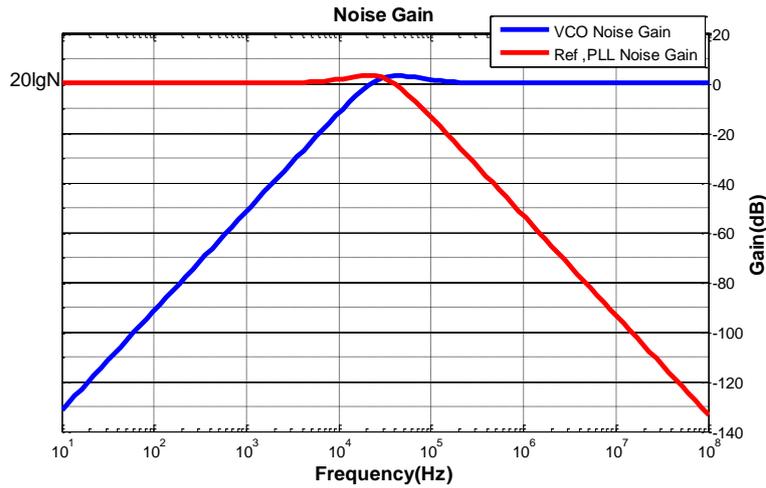


Fig. 2. Noise gain for VCO, PLL and Ref

Fig. 2 describes the noise gain of Ref, PLL and VCO. It can be inferred from this figure that the noise gain for VCO within loop Bw equals to $20\lg N$. For this configuration, the noise gain is 53.8 dB for Ref and PLL. Outside of the loop Bw the noise gain performs like a low-pass filter. That means the noise gain for Ref and PLL is reduced by the loop. The noise gain for VCO performs like a high-pass filter without extra amplification of noise.

By using the compensated PN model defined in (4) and the corresponding parameters proposed in Table 1, our proposed PN model is shown in the following Figs 3-5. In Fig. 3, for 15GHz phase noise, we compared our phase model with the realistic BS phase noise measurement (labeled as 'test result'). The result shows that our proposed PN model can match near perfectly. In addition, by observation and calculation, the gap between our proposed model and other models shown in Fig. 3 comes from the noise gain, which is $20\lg N$ in loop bandwidth and should be added in the model as mentioned above. Fig. 4 and Fig. 5 present the comparison of different models in 30GHz and 70GHz, respectively. In summary, we take the noise gain for Ref, PLL and VCO into consideration. By doing so, the PN model can be made more accurate and can therefore represent the real performance of current nowadays' commercial design level.

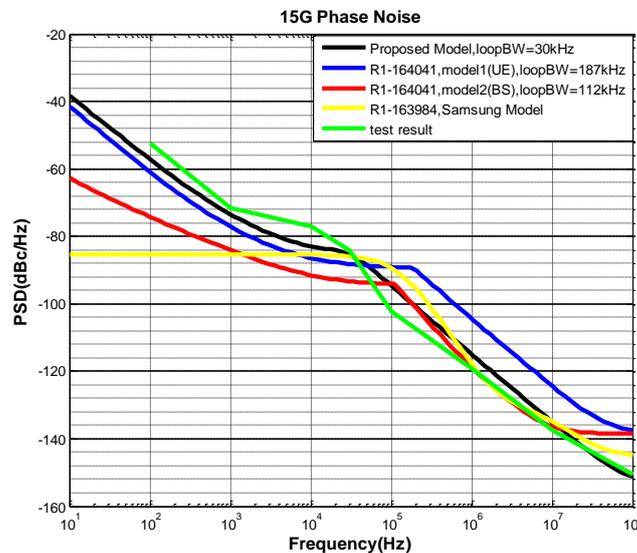


Fig. 3. PSD of our proposed phase noise model ($f_c=15\text{GHz}$)

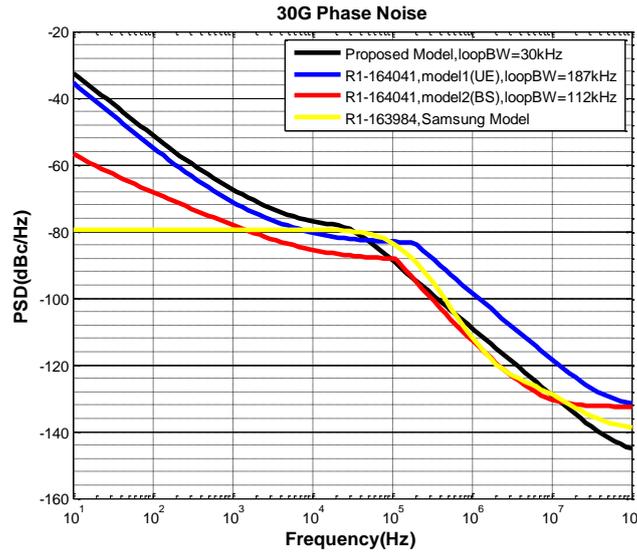


Fig. 4. PSD of our proposed phase noise model ($f_c=30\text{GHz}$)

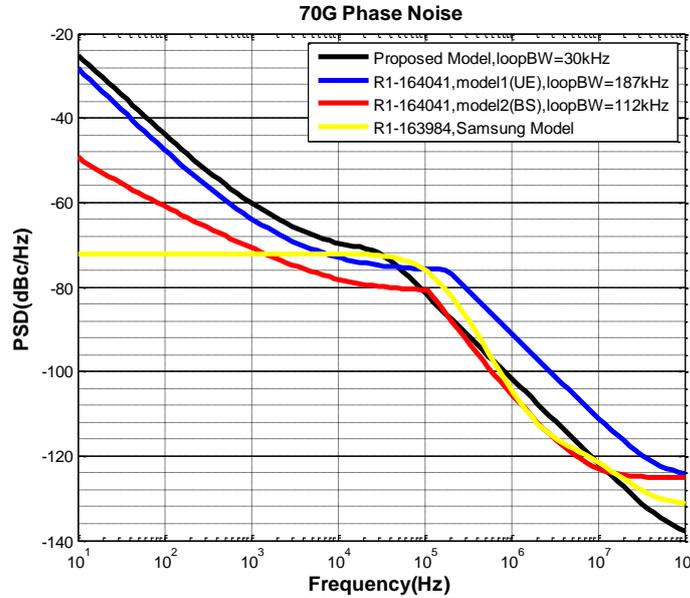


Fig. 5. PSD of our proposed phase noise model ($f_c=70\text{GHz}$)

- **Proposal 1:** The noise gain of PLL, Ref and VCO should be considered in phase noise model.
- **Proposal 2:** The phase noise model proposed by different companies should be compared and corrected with the realistic measurement.
- **Proposal 3:** The compensated phase noise model described in (4) and Table 1 should be adopted for the design and evaluation of the new radio for above 6GHz.

3. A Phase Noise Reduction Method

As can be seen from Fig. 6, the total PSD of a PLL based oscillator consists of the different sub-components on the oscillator circuit, namely reference clock, PLL loop components and the voltage controlled oscillator (VCO). VCO part can be typically understood to further consist of 1/f² and 1/f³ sub-components. Typically, the

reference clock and PLL components dominate the PSD inside the closed loop bandwidth of the PLL, and the VCO is the main impacting sub-component outside the loop bandwidth. Mathematically, the PSD of the phase noise can be expressed by equations (1)-(3).

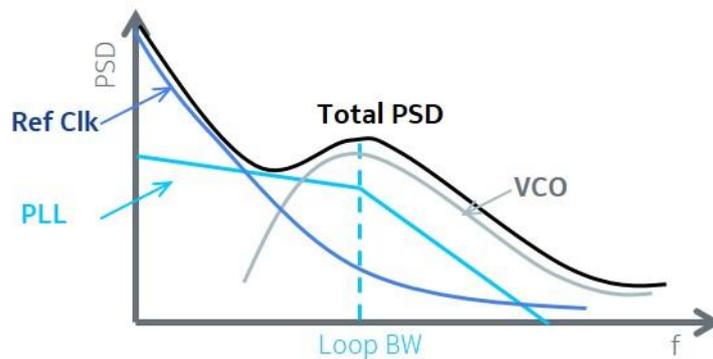


Fig. 6. Basic sub-components of a PLL based oscillator PSD [4]

Currently, the reference clock for RF PLL is mainly below 100MHz. If 30GHz is the target carrier frequency, then the multiplier (i.e., the PLL) will have to multiply the reference clock 300 times to obtain the target carrier frequency, respectively. However, if the reference clock can be increased to 500MHz or even 1GHz in the future, then only 60 and 30 times multiplier is needed to obtain the same target carrier frequency, respectively.

Huge reduction of divider ratio (multiple) means reduction of PN at target carrier frequency, although the PN of higher frequency reference is currently worse than the PN of lower frequency reference. However, with the progress of production process and physical material of oscillator, the PN for higher frequency reference will improve which will finally make the PN of the target carrier frequency better, especially for high frequency systems. Increasing reference clock frequency mainly impact the PN within loop BW, but the VCO part of PN is not impacted by such method. In the following discussion, it is shown that reduce PN level within loop BW is useful for system performance improvement.

The effect of PN on OFDM-based systems is its induced common phase error (CPE) and inter-carrier interference (ICI) [9]. The CPE, which is the average phase shift and is (almost) the same across all subcarriers, can be estimated using pilot symbols and compensated at the receiver. The ICI can be mitigated by increasing the subcarrier spacing [10], with which an increased portion of phase noise will be transformed into CPE and then compensated.

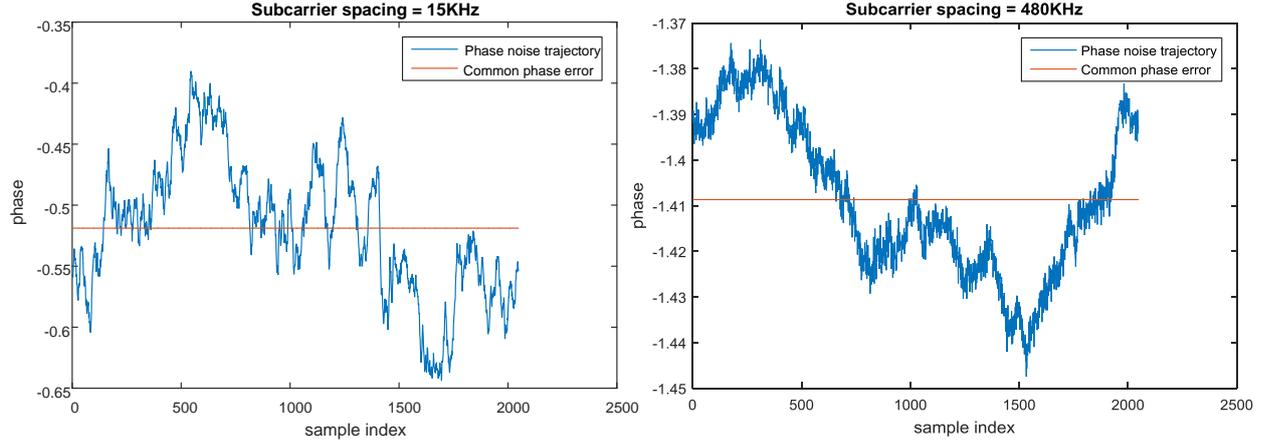


Fig. 7. Example of a phase-noise realization and its common phase error approximation for subcarrier spacing = 15KHz and 480KHz, respectively

CPE is in fact the DC part of a PN process [10], i.e., it belongs to the low-frequency part of PN, as illustrated in Fig. 7. If the PN part within the loop BW can be reduced, the whole PN as well as the effect of CPE can be reduced accordingly (i.e., the common factor that acts on all subcarriers will be smaller) and this will significantly facilitate the following CPE compensation (including the design and the number of CPE-compensation RS, the CPE estimation method and so on).

In summary, by increasing the reference clock frequency and the subcarrier spacing, the PN in high frequency may only need very simple CPE compensation or can even be directly neglected if low order modulation is transmitted.

- **Proposal 4:** *Further investigate whether increasing the reference clock frequency can potentially improve PN for high frequency systems at either BS or UE side.*

4. Conclusions

In this contribution, CMCC's proposed PN model based on realistic measurement is presented, i.e., a filtered version of PLL-based model which incorporates noise gains for Ref and PLL. Furthermore, a possible PN reduction method which increases the reference clock frequency for high frequency systems is proposed. The following proposals are achieved:

- **Proposal 1:** *The noise gain of PLL, Ref and VCO should be considered in phase noise model.*
- **Proposal 2:** *The phase noise model proposed by different companies should be compared and corrected with the realistic measurement.*
- **Proposal 3:** *The compensated phase noise model described in (4) and Table 1 should be adopted for the design and evaluation of the new radio for above 6GHz.*
- **Proposal 4:** *Further investigate whether increasing the reference clock frequency can potentially improve phase noise for high frequency systems at either BS or UE side.*

5. References

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