

**Agenda Item:** 6.4  
**Source:** Broadcom  
**Title:** Flexible and Formulaic Collision-free Memory Accessing for Parallel Turbo decoding with Quadratic polynomial permutation (QPP) Interleave

**Document for:** Discussion/Decision

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**Summary:** Turbo coding was suggested for 3GPP LTE channel coding that needs parallel decoding for high data throughput. One promising candidate is the quadratic polynomial permutation (QPP) [1] interleaver. This document proposes a memory accessing mapping for QPP interleave. The mapping is very simple to calculate (modulo). Furthermore, by using this mapping this document proves that for any practical number of processors  $P$ , the extrinsic memory of the QPP decoder can be accessed without memory contentions by choosing the proper number of memory bank  $C$  and window size  $W$ . Thus QPP-based turbo code can be decoded with maximum flexibility.

## 1 Introduction

The QPP interleaver of size  $L$  is defined by

$$\pi(x) = ax + bx^2 \bmod L$$

In parallel decoding, the decoding algorithm is windowed by dividing the entire block into some subblocks and performing shorter recursions inside the subblock, all assigned to distinct decoding processors working in parallel. Since every processor uses the same algorithm, they all access the memory at the same time instants. This may cause collisions, that is two (or more) accesses at the same time are attempted to the same memory bank. The collisions will weaken the efficiency of the decoding implementation. In [2], it is shown that there always exists collision-free memory accessing for parallel decoding of any degree and for any interleave. However, in general, the method given in [2] is somehow ad-hoc and is not implementation friendly, especially when a big amount of different block sizes (e.g. the coding system for LTE) have to be supported. In [3], one formulaic collision-free mapping is introduced and it is proved in [1] that this mapping is a collision-free memory mapping for QPP [1]. However, this mapping limits number of parallel processors to be a factor of the interleave size. In [4-5] a constructive collision-free mapping for any number of parallel processors is given for Rel.6 [6] interleave. In [7] a formulaic collision-free mapping for any number of parallel processors is developed

for almost regular permutation (ARP). An example of collision-free memory mapping for QPP with the number of processors is not a factor of the interleave size is given in [8]

In this contribution, we propose a flexible but still formulaic memory mapping that will accommodate any number of parallel processors P for any QPP interleaver.

## 2 Parallel decoding and collision-free memory accessing mapping

To carry out a parallel decoding with P parallel processors, one has to partition the interleave size L of turbo code to P subblocks. Since turbo code uses convolutional encoder as its constituent encoder, the consecutive symbols are connected through the states and therefore the subblock has to contain consecutive information bits. We call the subblock a window and its size the *window size*. Let index set of the information sequence be  $I = \{0, 1, \dots, L-1\}$  and the index set of the interleaved information sequence be  $\pi(I) = \{\pi(0), \pi(1), \dots, \pi(L-1)\}$ . Then the index sets of the P windows for I are

$$\{0, 1, \dots, W-1\}, \{W, W+1, \dots, 2W-1\}, \dots, \{(P-1)W, \dots, PW-1\} \quad (\text{EQ-1})$$

Define  $E_i = \{i, W+i, \dots, sW+i, \dots, (P-1)W+i\}$ ,

On the interleaved side, the index sets of the C windows for  $\pi(I)$  are

$$\{\pi(0), \pi(1), \dots, \pi(W-1)\}, \{\pi(W), \pi(W+1), \dots, \pi(2W-1)\}, \dots, \{\pi((P-1)W), \dots, \pi(PW-1)\} \quad (\text{EQ-2})$$

Similarly, we define

$$\hat{E}_i = \{\pi(i), \pi(W+i), \dots, \pi(sW+i), \dots, \pi((P-1)W+i)\}$$

Then a map  $\circ\mathcal{M}$  defined from the index set I and  $\pi(I)$  to the set  $\{0, 1, \dots, C-1\}$  is called a *collision-free mapping* [3] if it satisfies the following condition:

$$j, j' \in E_i \Rightarrow \circ\mathcal{M}(j) \neq \circ\mathcal{M}(j') \text{ and } j, j' \in \hat{E}_i \Rightarrow \circ\mathcal{M}(j) \neq \circ\mathcal{M}(j')$$

for every  $j, j' \in \{0, \dots, L-1\}$ ,  $j \neq j'$  and all possible  $i$ , in other words, the decoded values belonging to the index set at cycle  $i$  should be stored into different memory banks.

## 3 Formulaic and flexible collision-free mapping

For any number C, we define a modulation memory mapping with window size W by

$$\mathcal{M}_{MOD,C,W} : i \mapsto i \bmod C$$

Consider an interleaver  $\pi$  of size  $L$ . In the following two conditions are given for a modulation mapping being collision-free for parallel decoding of any  $P$  processors.

**Condition I:** If  $\pi(x) = \pi(y) \bmod C$  then  $x = y \bmod C$ .

**Condition II:** Let  $W$  be the window size, a)  $W \geq L/P$  and b)  $\gcd(W, C) = 1$ .

**Theorem 1** Let  $P$  be number of parallel decoding processors such that  $P \leq C$ . If  $\pi$  and  $C$  satisfies Condition I and the window size  $W$  satisfies Condition II, then  $\mathcal{M}_{MOD,C,W}$  is a collision-free memory accessing mapping for  $P$  parallel processors.

Proof:

A) In natural - order phase, if  $\mathcal{M}_{MOD,C,W}(s_0W + t) = \mathcal{M}_{MOD,C,W}(s_1W + t)$ , then

$$s_0W \equiv s_1W \bmod C.$$

But  $s_0$  and  $s_1$  are less than  $P \leq C$  (see EQ - 1) and  $\gcd(W, C) = 1$  (Condition 2). So,

$$\mathcal{M}_{MOD,C,W}(s_0W + t) = \mathcal{M}_{MOD,C,W}(s_1W + t) \Rightarrow s_0 = s_1.$$

B) In interleaved - order phase, if  $\mathcal{M}_{MOD,C,W}(\pi(s_0W + t)) = \mathcal{M}_{MOD,C,W}(\pi(s_1W + t))$ ,

then  $\pi(s_0W + t) \equiv \pi(s_1W + t) \bmod C$ . By Condition 1, it implies that

$$(s_0W + t) \equiv (s_1W + t) \bmod C. \text{ So, once again, } s_0 = s_1.$$

Combine A) and B), we prove that  $\mathcal{M}_{MOD,C,W}$  is a collision-free memory accessing mapping for  $\pi$ .

□

It is easy to see that there always exists a smallest  $W$  that satisfies Condition II. To find a  $C$  that satisfies Condition I for QPP a sufficient condition is given in the following theorem.

**Theorem 2** Let  $\pi(x) = ax + bx^2 \bmod L$  be a QPP interleaver of size  $L$ . If  $C$  is a factor of  $L$ , i.e.  $C|L$ . Then  $\pi(x) = \pi(y) \bmod C$  if and only if  $x = y \bmod C$ , i.e. Condition I is satisfied.

Proof. ( $\leftarrow$ ) Suppose  $x = y \bmod C$ . There is an integer  $k$  such that  $x = y + kC$ . Thus

$$\begin{aligned} \pi(y) - \pi(x) &= a(x + kC - x) + b(x^2 + 2kCx + 4k^2C^2 - x^2) \bmod L \\ &= C(ak + 2b^2kx + 4k^2C) \bmod L = 0 \bmod C \end{aligned}$$

since  $C|L$ .

( $\rightarrow$ ) Suppose  $\pi(x) = \pi(y) \bmod C$ . Define two sets

$$S(x) = \{i \mid i = x \bmod C\}, S(y) = \{j \mid j = y \bmod C\}.$$

Assume  $x \neq y \bmod C$ , then  $S(x) \cap S(y) = \emptyset$ . However, by ( $\leftarrow$ ) we have

$$\pi(S(x)) = \{\pi(i) \mid i = x \bmod C\} = \{\pi(i) \mid \pi(i) = \pi(x) \bmod C\} \text{ and}$$

$$\pi(S(y)) = \{\pi(j) \mid j = y \bmod C\} = \{\pi(j) \mid \pi(j) = \pi(y) \bmod C\}$$

Thus  $\pi(S(x)) = \pi(S(y))$ . This contradicts to  $S(x) \cap S(y) = \emptyset$  and  $\pi$  is a permutation. Therefore,  $x = y \bmod C$ .

□

With Theorems 1 and 2, we now can construct a collision-free modulation memory mapping for a QPP that suit for any given  $P$  parallel processors. In the following, two examples are given.

**Example 1:** Consider a QPP  $\pi$  of size  $L = 6144 = 3 * 2^{11}$  in the list of [9]. Let the number of parallel processors  $P=20$ . With this number of parallel processors the formulaic memory mapping in [3] cannot be applied since 20 is not a factor of  $L$ . Let us now take  $C=24$  which is a factor of  $L$  and  $C>P$ . Thus, Condition I holds for this  $C$  by Theorem 2. Let  $W=311$ , then  $W$  satisfies Condition II. Therefore, by Theorem 1,  $\mathcal{M}_{MOD,20,311}$  is a collision-free mapping for this QPP with the number of parallel processors  $P=20$ .

**Example 2:** Consider a QPP  $\pi$  of size  $L = 4736 = 37 * 2^7$  in the list of [9]. Let the number of parallel processors  $P=10$ . Take  $C=16$  we have  $C|L$  and  $P<C$ . Then by Theorem 2, Condition I holds. Let  $W=475$ , then  $W$  satisfy Condition II. Therefore, by Theorem 1,  $\mathcal{M}_{MOD,10,475}$  is a collision-free mapping for this QPP with number of parallel processors  $P=10$ .

**Remarks on  $P$**  (number of parallel processors)

- 1  $P$  is not capped by any fixed number such as 20 or 32, and is continuous beyond 20/32, thus allowing fine granularity in decoder throughput increase.
- 2 The same  $P$  may be used for a wide range of sizes, without being limited by the factors of each size. For example
  - 2.1) Use  $P=1$  for  $L \leq 512$ ;
  - 2.2) Use  $P=2$  for  $512 < L \leq 1024$ ;
  - 2.3) Use  $P=3$  for  $1024 < L \leq 1536$ ,
 etc.

## 4 Conclusion

For any number of processor  $P$ , by carefully choosing the number  $C \geq P$  and  $W$ , the memory mapping  $\mathcal{M}_{MOD,C,W}$  is collision-free mapping for any QPP. Moreover,

memory mapping  $\mathcal{M}_{MOD,C,W}$  provides more freedom for selecting QPP that satisfying parallel decoding with any decoding processors.

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