TSGR1#20(01)0487

Introduction of Rel-5 WI "Gated DPCCH Transmission"

21-25 May 2001

3GPP RAN WG1/WG2/WG3

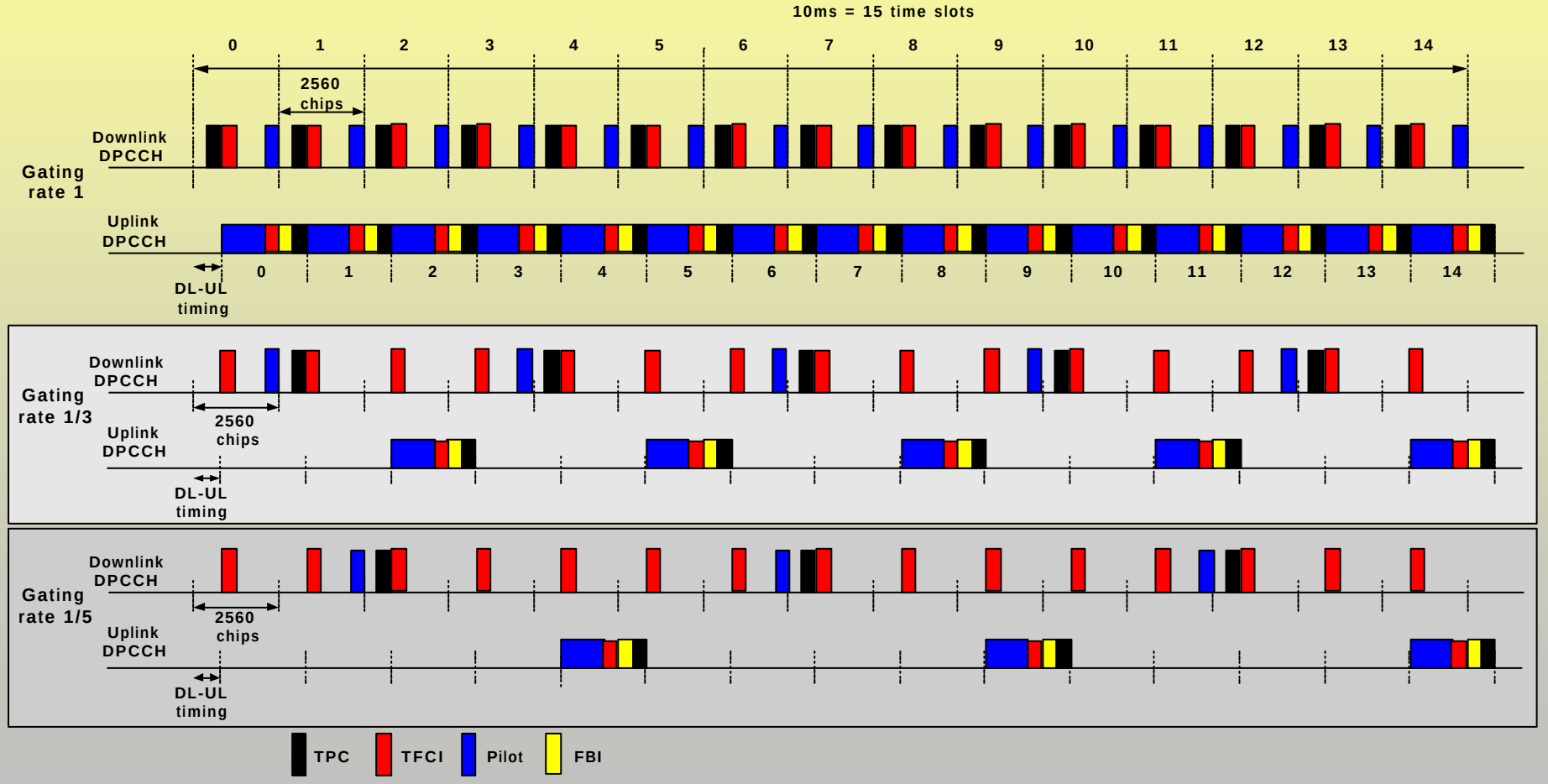
Busan, Korea

Samsung Electronics and Nokia

Overview

- **Battery life is an important resource in UE side and capacity is an important resource in network side**
- **Rel-5 Work item "Gated DPCCH transmission"**
  - **Apply for DCH associated with DSCH in FDD**
  - **Intermittent transmission of DPCCH**
- **Expected gain with respect to Release 99**
  - **UE battery life increase**
  - **Capacity increase due to reduction of interference on both UL and DL**

Gating Operation



DPCCH Switched-On Time Slot

- DL: TPC and PILOT are ‘on’ only for the switched-on time slots, but TFCI is ‘on’ for all time slots
- UL: All control fields (PILOT, TFCI, TPC, and FBI) are ‘on’ only for the switched-on time slots
- Reference pattern for switched-on time slot
  - Pseudo-random pattern based on CFN is used

Gating Structure

- Initiation & Termination
  - Determined by UTRAN
  - Indicated using higher layer signaling
- Parameters
  - Gating rate: 1, 1/3, 1/5
  - Gating mode (Direction)
    - Uplink/Downlink
    - Downlink only
  - TFCS Subset Info
  - RX gating DRX cycle
- Basic Gating and embedded data periods

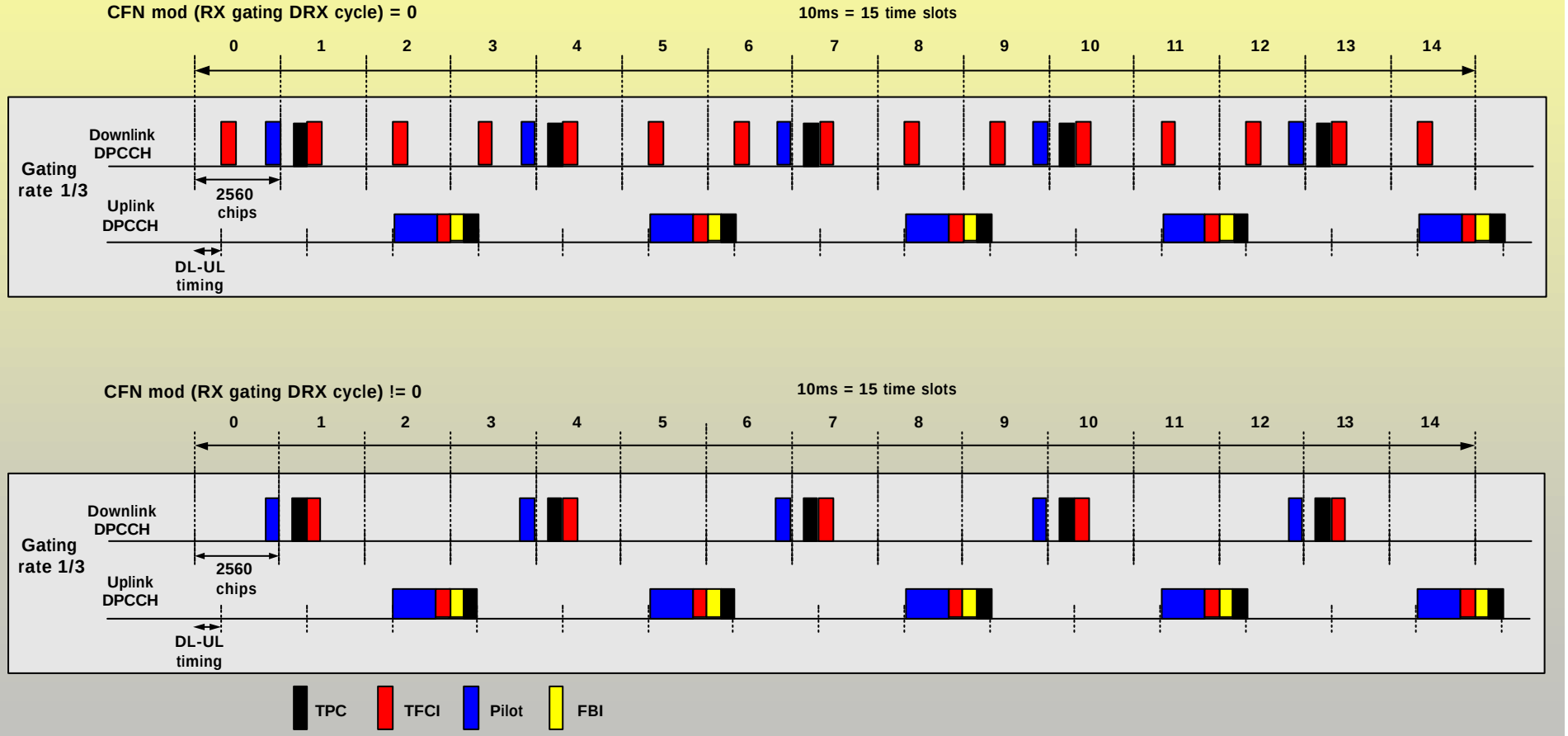
Gating Structure (cont'd)

- Initiation
  - Activated by higher layer signaling when there is no data to transmit on both UL and DL
- Gating period
  - *Basic Gating period*: intermittent transmission of DPCCH only on the specified time slots
  - *Embedded data period*: permission of low rate data transmission on DPDCH under gating
    - Data rate can be restricted by TFCS
- Termination
  - Deactivated by higher layer signaling when there is data to transmit on either UL or DL

RX Gating

- **Battery Saving from the UE RX side**
  - **Achieved by signaling `RX gating DRX cycle' from UTRAN to UE with the other gating parameters**
  - ***Start of DPDCH transmission is allowed if***
    - **CFN mod (RX gating DRX cycle) = 0 and**
    - **CFN corresponds to beginning of each TTI**
- **TFCI is transmitted**
  - **in all slots if CFN mod (RX gating DRX cycle) = 0**
  - **intermittently if CFN mod (RX gating DRX cycle) ? 0**

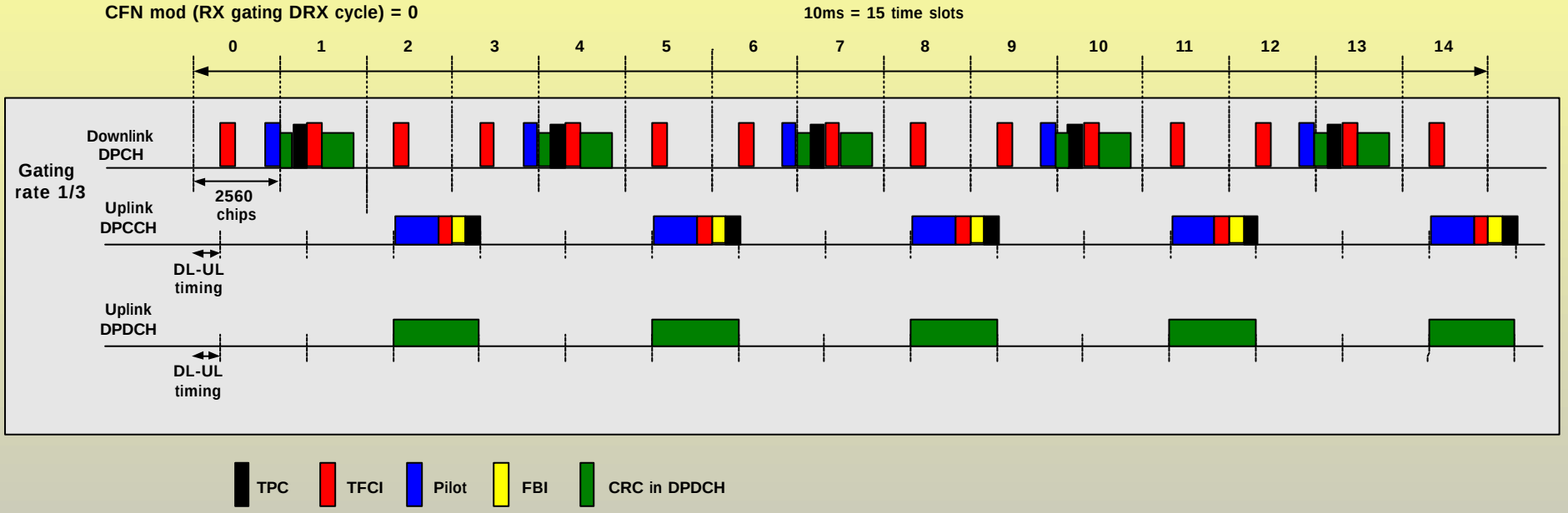
RX Gating (cont'd)



Outer Loop Power Control

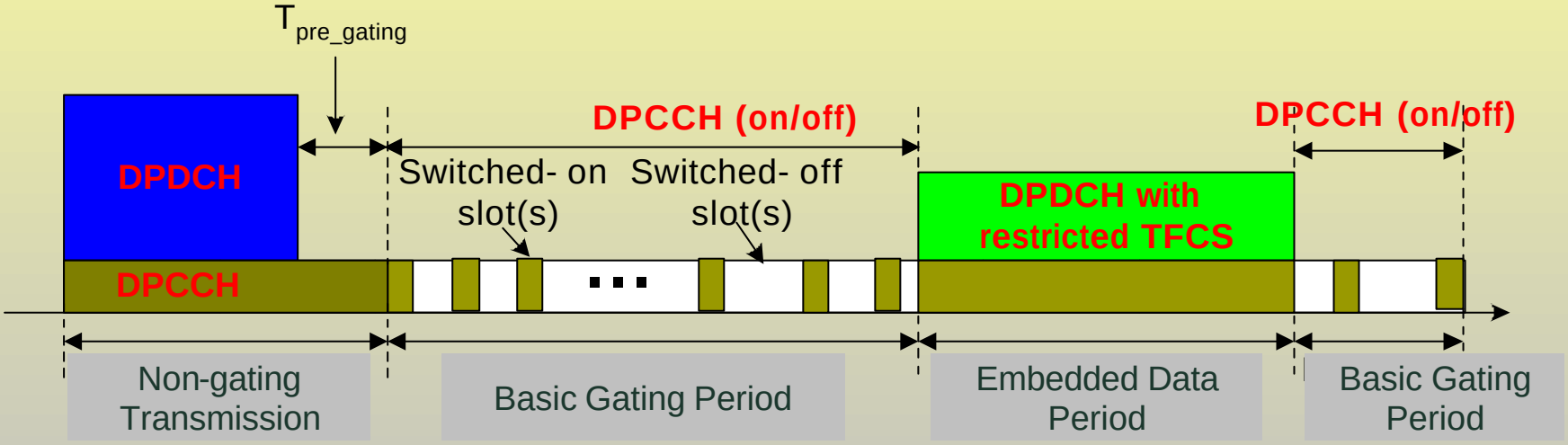
- **Facilitates adequate performance for outer loop power control during gating**
  - **CRC is attached to the zero length transport block**
- **Encoded CRC is transmitted intermittently on DPDCH**
  - **Uplink: encoded CRC is transmitted in the time slots in which DPCCH is transmitted**
  - **Downlink: encoded CRC is transmitted in the time slots in which TPC is transmitted**

Outer Loop Power Control (cont'd)



Basic Gating and Embedded Data Periods

- Example of uplink DPDCH transmission



Embedded Data Period

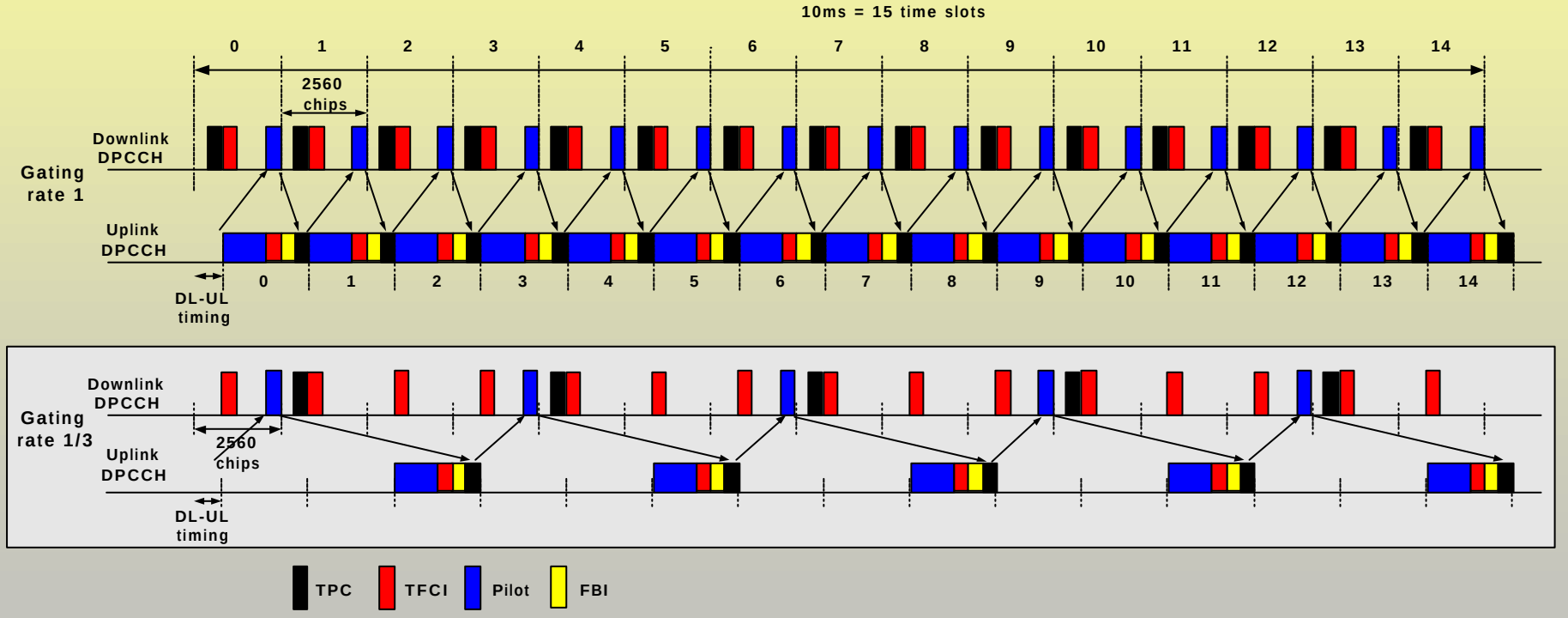
- To transfer low rate data during gating
  - Turning on transmission of DPCCH on all the time slots
  - But TPC shall be updated only for the specified time slots as in basic gating period
  - Restricted TFCS is used for limiting data rate
- Detection of DPDCH during gating
  - DL: Decoding DL TFCI
  - UL: Pilot energy comparison in UTRAN
- Advantage
  - Avoidance of unnecessary signaling to initiate and terminate gating
  - Increase of average duration of gating

Pseudo-Random Pattern Generation

- The generation is based on CFN of period 2.56 sec
- The known CFN enables UTRAN & UE to generate the pseudo-random pattern synchronously
- No extra signaling is required for the synchronized generation of pseudo-random pattern
- EMI problem can be minimized

Power Control for Gating

- **Conceptual diagram of power control operation**



- **Gating results in reduced power control rate**

Power Control for Gating (cont'd)

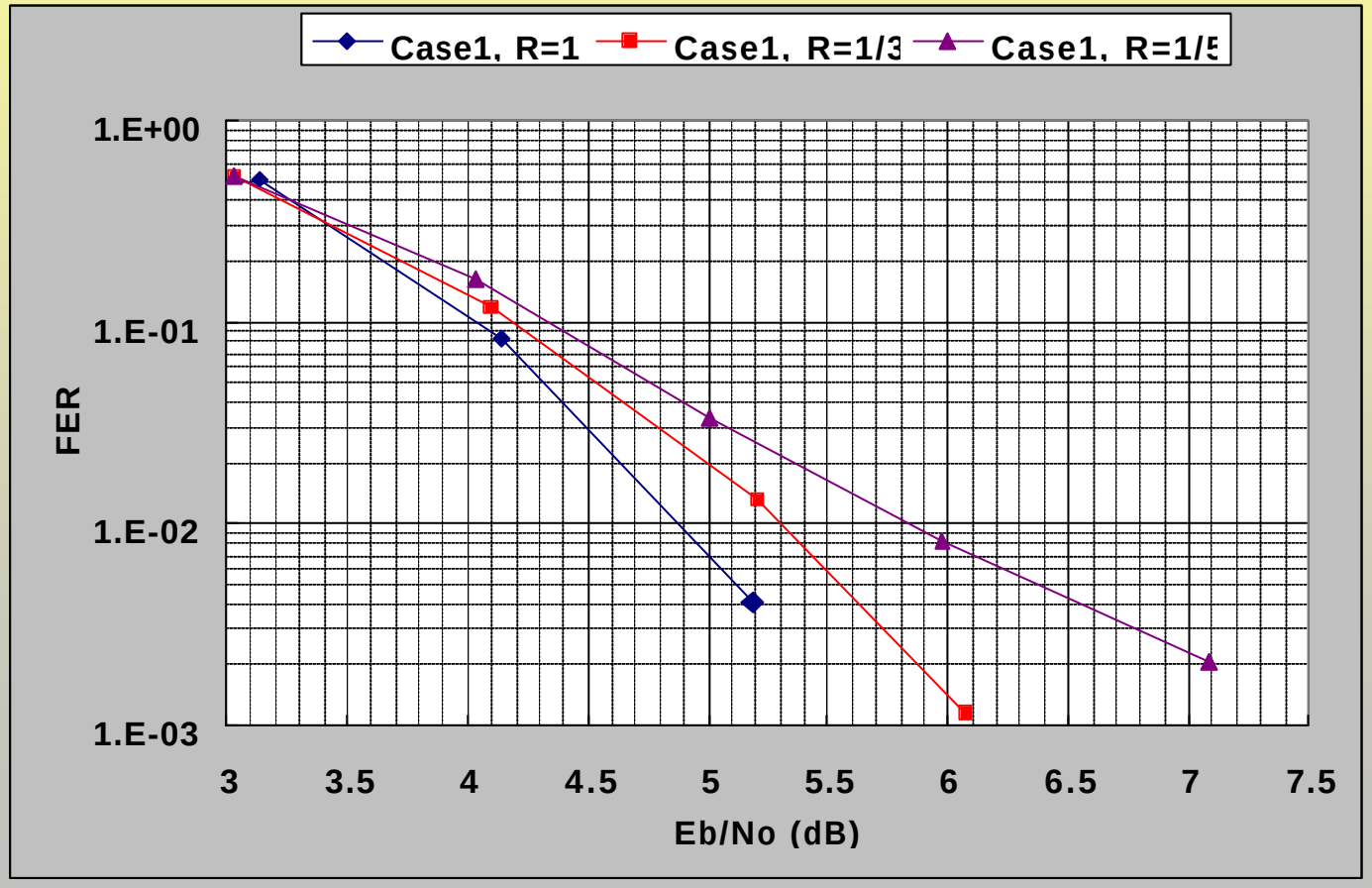
- **Transmit power adjustment**
  - **Performed in response to the latest valid TPC command**
- **TPC command**
  - **Generated based on the latest valid received switched-on time slot**
  - **Transmission power is updated on the earliest valid switched-on time slot**

Power Control Performance

- Link simulation was made to evaluate the required TX E_b/N_0 of UL DPDCH during embedded DPDCH period
- DL gating rates = 1, 1/3, 1/5
- UL channel bit rate
  - DPDCH: 60 kbps
  - DPCCH: 15 kbps
- DPCCH/DPDCH = -5dB
- Power control rate
  - No gating: 1500 Hz
  - Gating: 500 Hz (Gating rate R=1/3), 300 Hz (R=1/5)
- TPC command error = 4%
- Channel coding: convolution code of rate 1/3

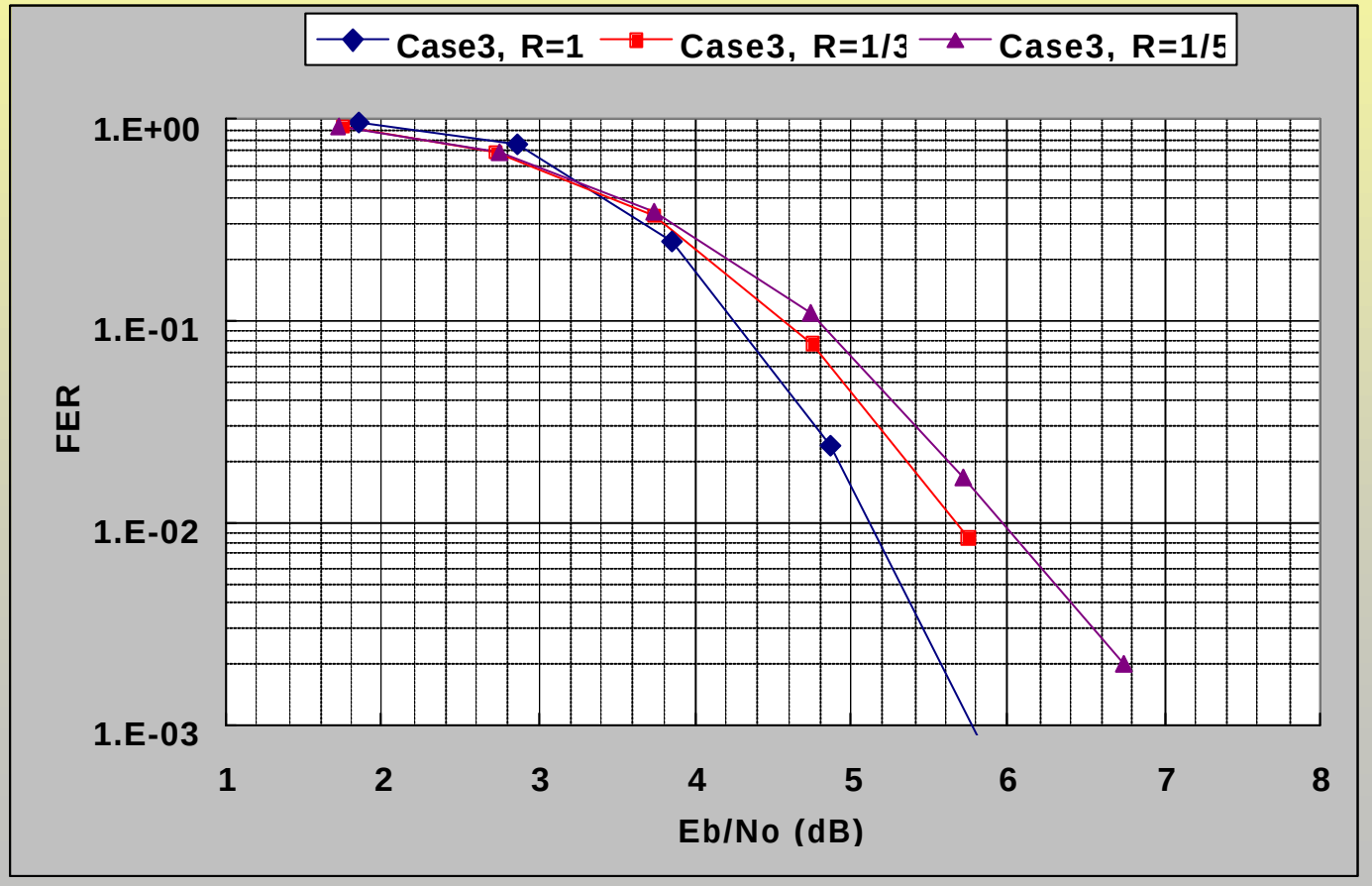
Power Control Performance (cont'd)

- UL DPCH required E_b/N_0 with UE speed = 3 km/h
  - E_b/N_0 increase ? 0.4 dB (R=1/3), 1.0 dB (R=1/5) at FER=1%



Power Control Performance (cont'd)

- UL DPCH required E_b/N_0 with UE speed = 120 km/h
  - E_b/N_0 increase ? 0.6 dB (R=1/3), 0.9 dB (R=1/5) at FER=1%



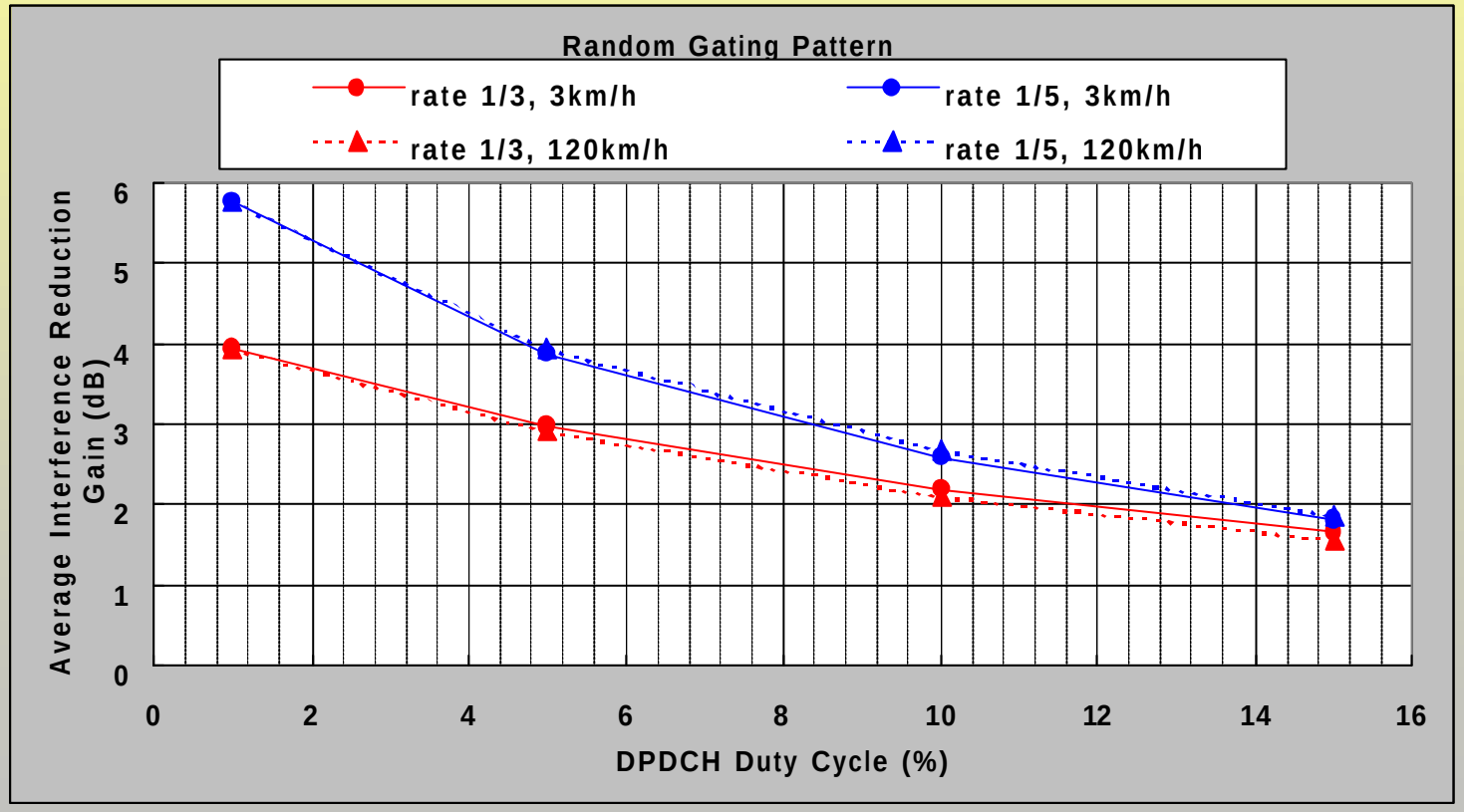
Power Control Performance (cont'd)

- **Summary of simulation results**
  - **Reduced power control rate increases the E_b/N_0 required for DPDCH transmission during embedded data period**
    - **Additional required power < 1 dB**
  - **UL TX power is zero in the switched-off slots during the basic gating period**
  - **The gated transmission can save overall UE TX power**

UL Interference Reduction

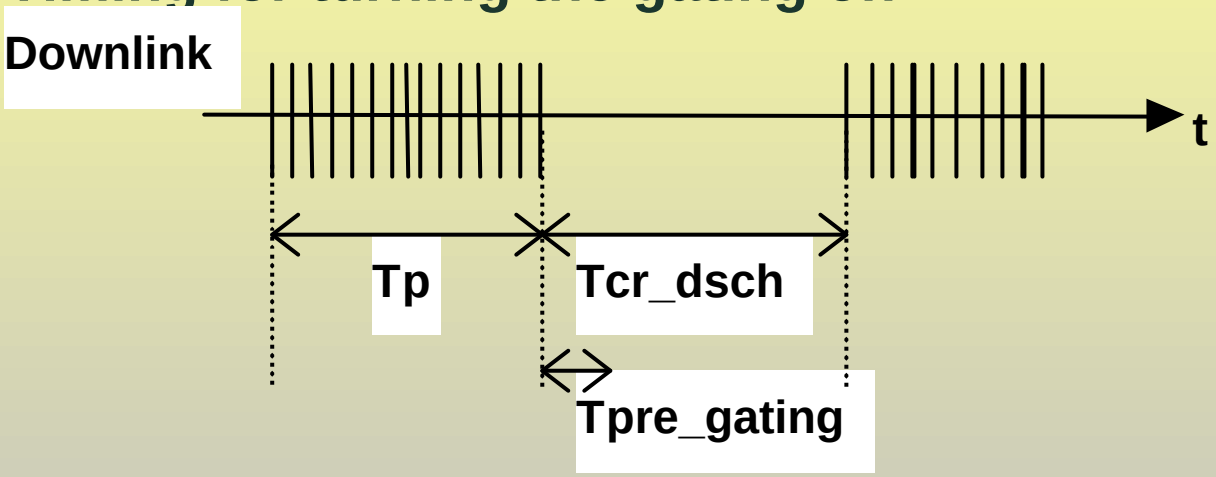
- **Average UL Interference Reduction Gain**

  =(average Tx power when no gating)/(average Tx power when gating)



UE Battery Life Enhancement

- Timing for turning the gating on



- Percentage of time DPCCH gating on for DCH associated with DSCH
  - DPCCH_gating_% = 66 %

UE Battery Life Enhancement (cont'd)

- UE battery life improvement calculation with TX only gating

	Gating rate	UE battery life improvement
Medium range Tx power level	1/3	21 %
	1/5	34 %
Maximum Tx power level	1/3	26 %
	1/5	44 %

UE Battery Life Enhancement (cont'd)

- UE battery life improvement due to TX and RX gating with medium range TX power level

Gating rate	K	UE battery life improvement
1/3	1	21 %
	4	32 %
	8	34 %
1/5	1	34 %
	4	56 %
	8	60 %

  - K: RX gating DRX cycle
  - RX side has to be on during the whole frame in every Kth frame

Conclusion

- Advantage of gating compared to continuous transmission of DPCCH when no DSCH data
  - Improved battery life in UE side
  - Interference reduction (capacity increase) in UTRAN side
- Rx gating
  - More improved battery life
- Outer loop power control during gating
  - CRC attachment to zero length transport block