

**3rd Generation Partnership Project (3GPP);
Technical Specification Group (TSG);
Radio Access Network (RAN);
1.28Mcps functionality for UTRA TDD Physical Layer**



Reference

DTS/TSGR-0125223 (25223-300.PDF)

Keywords

<keyword[, keyword]>

3GPP

Postal address

Office address

Internet

secretariat@3gpp.org
Individual copies of this deliverable
can be downloaded from
<http://www.3gpp.org>

Copyright Notification

No part may be reproduced except as authorized by written permission.
The copyright and the foregoing restriction extend to reproduction in all media.

© 1999, 3GPP Organizational Partners (ARIB, CWTS, ETSI, T1, TTA, TTC).
All rights reserved.

Contents

| | |
|--|----|
| Foreword | 7 |
| 1 Scope | 8 |
| 2 References | 8 |
| 3 Abbreviations | 8 |
| 4 Radio Requirements | 9 |
| 4.1 Radio environments | 9 |
| 4.2 Services | 9 |
| 4.3 Operational requirements | 9 |
| 4.3.1 Deployment scenarios | 9 |
| 4.4 Handover and Cell selection/reselection | 11 |
| 4.5 Particular characteristics of the low chip rate TDD | 11 |
| 5 High level characteristics | 12 |
| 6 Physical layer - General description | 14 |
| 6.1 General description of Layer 1 | 14 |
| 6.1.2 Service provided to higher layers | 14 |
| 6.2 Document structure of the physical layer specification | 14 |
| 6.2.1 Multiple Access | 14 |
| 6.2.2 Channel coding and interleaving | 14 |
| 6.2.3 Modulation and spreading | 14 |
| 6.2.4 Physical layer procedures | 15 |
| 6.2.5 Physical layer measurements | 15 |
| 7 Physical channels and mapping of transport channels onto physical channels | 16 |
| 7.1 Transport channels | 16 |
| 7.1.1 Transport channels | 16 |
| 7.2 Physical channels | 16 |
| 7.2.1 Frame structure | 16 |
| 7.2.2 Dedicated physical channel (DPCH) | 17 |
| 7.2.2.1 Spreading | 17 |
| 7.2.2.2 Burst Types | 17 |
| 7.2.2.2.1 Transmission of TFCI | 18 |
| 7.2.2.2.2 Transmission of TPC | 19 |
| 7.2.2.2.3 Timeslot formats | 23 |
| 7.2.2.2.3 Transmission of SS | 37 |
| 7.2.2.3 Training sequences for spread bursts | 39 |
| 7.2.2.4 Beamforming and Transmit Diversity | 46 |
| 7.2.3 Primary common control physical channel (P-CCPCH) | 47 |
| 7.2.3.1 Primary common control physical channel (P-CCPCH) | 47 |
| 7.2.3.1.1 P-CCPCH Spreading | 48 |
| 7.2.3.1.2 P-CCPCH Burst Types | 48 |
| 7.2.3.1.3 P-CCPCH Training sequences | 48 |
| 7.2.3.2 Secondary common control physical channel (S-CCPCH) | 48 |
| 7.2.3.2.1 S-CCPCH Spreading | 49 |
| 7.2.3.2.2 S-CCPCH Burst Types | 49 |
| 7.2.3.2.3 S-CCPCH Training sequences | 49 |
| 7.2.3.3 Fast Physical Access CHannel (FPACH) | 49 |
| 7.2.3.3.1 FPACH burst | 49 |
| 7.2.3.3.1.1 Signature Reference Number | 49 |
| 7.2.3.3.1.2 Relative Sub-Frame Number | 49 |
| 7.2.3.3.1.3 Received starting position of the UpPCH (UpPCH _{pos}) | 50 |
| 7.2.3.3.1.4 Transmit Power Level Command for the RACH message | 50 |
| 7.2.3.3.2 Coding of the Forward Physical Access Channel (FPACH) information bits | 50 |

| | | |
|---|--|------|
| 7.2.3.3.3 | FPACH Spreading..... | 5051 |
| 7.2.3.3.4 | FPACH Burst Format..... | 5051 |
| 7.2.3.3.5 | FPACH Training sequences..... | 51 |
| 7.2.3.4 | The physical random access channel (PRACH)..... | 51 |
| 7.2.3.4.1 | PRACH Spreading..... | 51 |
| 7.2.3.4.2 | PRACH Burst Types..... | 51 |
| 7.2.3.4.3 | PRACH Training sequences..... | 51 |
| 7.2.3.4.4 | Association between Training Sequences and Channelisation Codes..... | 51 |
| 7.2.3.5 | The synchronisation channel (SCH)..... | 5152 |
| 7.2.3.6 | Physical Uplink Shared Channel (PUSCH)..... | 52 |
| 7.2.3.7 | Physical Downlink Shared Channel (PDSCH)..... | 52 |
| 7.2.3.8 | The Page Indicator Channel (PICH)..... | 52 |
| 7.2.3.8.1 | Mapping of Paging Indicators to the PICH bits..... | 52 |
| 7.2.3.8.2 | Structure of the PICH over multiple radio frames..... | 53 |
| 7.2.4 | Beacon function of physical channels..... | 55 |
| 7.2.4.1 | Location of physical channels with beacon function..... | 55 |
| 7.2.4.2 | Physical characteristics of the beacon function..... | 55 |
| 7.2.5 | Midamble Allocation for Physical Channels..... | 5556 |
| 7.3 | Mapping of transport channels to physical channels..... | 5556 |
| 7.3.1 | Dedicated Transport Channels..... | 56 |
| 7.3.2 | Common Transport Channels..... | 57 |
| 7.3.2.1 | The Broadcast Channel (BCH)..... | 58 |
| 7.3.2.2 | The Paging Channel (PCH)..... | 59 |
| 7.3.2.2 | The Forward Channel (FACH)..... | 59 |
| 7.3.2.3 | The Random Access Channel (RACH)..... | 59 |
| 7.3.2.4 | The Uplink Shared Channel (USCH)..... | 60 |
| 7.3.2.5 | The Downlink Shared Channel (DSCH)..... | 60 |
| Annex A (Normative): Basic Midamble Codes..... | | 60 |
| A.1 | Basic Midamble Codes for Burst Type 1 and PRACH Burst Type..... | 60 |
| A.2 | Association between Midambles and Channelisation Codes..... | 64 |
| A.2.1 | Association for K=16 Midambles..... | 65 |
| A.2.2 | Association for K=8 Midambles..... | 65 |
| A.2.3 | Association for K=4 Midambles..... | 66 |
| A.2.4 | Association for K=2 Midambles..... | 67 |
| A.2.5 | Association for K=14 Midambles..... | 68 |
| A.2.6 | Association for K=12 Midambles..... | 69 |
| A.2.7 | Association for K=10 Midambles..... | 70 |
| A.2.8 | Association for K=6 Midambles..... | 71 |
| Annex B (Informative): CCPCH Multiframe Structure..... | | 73 |
| Annex C (Informative): Examples of the association of DL TPC commands to UL uplink time slots for 1.28 Mcps TDD..... | | 75 |
| Annex D (Informative): Examples of the association of DL SS commands to UL uplink time slots..... | | 76 |
| 8 | Multiplexing and channel coding..... | 77 |
| 8.1 | Transport channel coding/multiplexing..... | 77 |
| 8.1.1 | Error detection..... | 77 |
| 8.1.2 | Transport block concatenation and code block segmentation..... | 77 |
| 8.1.3 | Channel coding..... | 77 |
| 8.1.4 | Radio frame size equalisation..... | 78 |
| 8.1.5 | 1st interleaving..... | 78 |
| 8.1.6 | Radio frame segmentation..... | 78 |
| 8.1.7 | Sub-frame segmentation..... | 78 |
| 8.1.8 | Rate matching..... | 81 |
| 8.1.9 | TrCH multiplexing..... | 81 |
| 8.1.10 | Physical channel segmentation..... | 81 |
| 8.1.11 | 2nd interleaving..... | 81 |
| 8.1.11.1 | Frame related 2nd interleaving..... | 81 |
| 8.1.11.2 | Timeslot related 2 nd interleaving..... | 81 |

| | | |
|-------------|--|--------------------|
| 8.1.12 | Physical channel mapping..... | 81 |
| 8.1.13 | Multiplexing of different transport channels onto one CCTrCH, and mapping of one CCTrCH onto physical channels | 83 |
| 8.1.13.1 | Allowed CCTrCH combinations for one UE..... | 83 |
| 8.1.13.1.1 | Allowed CCTrCH combinations on the uplink..... | 83 |
| 8.1.13.1.2 | Allowed CCTrCH combinations on the downlink..... | 83 |
| 8.1.14 | Transport format detection | 83 |
| 8.2 | Coding for layer 1 control..... | 83 |
| 8.2.1 | Coding of transport format combination indicator (TFCI) | 83 |
| 8.2.1.1 | Coding of transport format combination indicator (TFCI) for 8PSK | 84 |
| 8.2.1.1.1 | Coding of long TFCI lengths..... | 84 |
| 8.2.1.1.2 | Coding of short TFCI lengths | 86 |
| 8.2.1.1.2.1 | Coding very short TFCIs by repetition | 86 |
| 8.2.1.1.2.2 | Coding short TFCIs using bi-orthogonal codes | 86 |
| 8.2.1.1.3 | Mapping of TFCI code word | 87 |
| 8.2.2 | Coding of Synchronisation Shift..... | 88 |
| 8.2.3 | Coding of Transmit Power Control (TPC)..... | 89 |
| 8.2.4 | Coding of the Paging Indicator..... | 90 |
| 9 | Spreading and Modulation | 90 |
| 9.1 | Data modulation..... | 90 |
| 9.1.2 | Mapping of bits onto signal point constellation..... | 90 |
| 9.1.2.1 | QPSK modulation..... | 90 |
| 9.1.2.2 | 8PSK modulation..... | 90 |
| 9.1.3 | Symbol rate..... | 91 |
| 9.2 | Spreading modulation | 91 |
| 9.2.1 | Basic spreading parameters | 91 |
| 9.2.2 | Spreading codes | 91 |
| 9.2.3 | Scrambling codes..... | 91 |
| 9.2.4 | Spread and scrambled signal of data symbols and data blocks | 91 |
| 9.3 | Synchronisation codes | 92 91 |
| 10 | Physical layer procedures | 104 103 |
| 10.1 | Transmitter Power Control..... | 104 103 |
| 10.1.2 | Uplink Control..... | 104 |
| 10.1.2.2 | Common Physical Channel..... | 105 104 |
| 10.1.3 | Downlink Control..... | 106 105 |
| 10.1.3.1 | Common Physical Channel..... | 106 105 |
| 10.1.3.2 | Dedicated Physical Channel..... | 106 105 |
| 10.2 | Timing Advance..... | 106 |
| 10.2.1 | With UL Synchronization..... | 106 |
| 10.2.1.1 | The establishment of uplink synchronization..... | 108 106 |
| 10.2.1.1.1 | Preparation of uplink synchronization (downlink synchronization)..... | 108 106 |
| 10.2.1.1.2 | Establishment uplink synchronization..... | 108 106 |
| 10.2.1.2 | Maintenance of uplink synchronisation..... | 109 106 |
| 10.3 | Synchronisation and Cell Search Procedures | 109 107 |
| 10.3.1 | Cell Search | 109 107 |
| 10.4 | Discontinuous transmission (DTX) of Radio Frames | 110 108 |
| 10.5 | Downlink Transmit Diversity | 110 108 |
| 10.5.1 | Transmit Diversity for DPCH..... | 110 108 |
| 10.5.1.1 | TSTD for DPCH..... | 110 108 |
| 10.5.1.2 | Closed Loop Tx Diversity for DPCH | 111 109 |
| 10.5.2 | Transmit Diversity for DwPCH..... | 112 110 |
| 10.5.3 | Transmit Diversity for P-CCPCH..... | 112 110 |
| 10.5.3.1 | TSTD Transmission Scheme for P-CCPCH | 112 110 |
| 10.6 | Random Access Procedure | 113 111 |
| 10.6.1 | Preparation of random access..... | 113 111 |
| 10.6.2 | Random access procedure | 113 111 |
| 10.6.2.1 | Definitions | 114 111 |
| 10.6.2.2 | Preparation of random access | 114 112 |

| | | |
|------------------------|---|-----------------------|
| 10.6.2.3 | Random access procedure | <u>115</u> <u>113</u> |
| 10.6.2.3.1. | The use and generation of the information fields transmitted in the FPACH..... | <u>115</u> <u>113</u> |
| 10.6.2.3.1.1 | Signature Reference Number..... | <u>116</u> <u>114</u> |
| 10.6.2.3.1.2 | Relative Sub-Frame Number..... | <u>116</u> <u>114</u> |
| 10.6.2.3.1.3 | Received starting position of the UpPCH (UpPCH _{POS})..... | <u>116</u> <u>114</u> |
| 10.6.2.3.1.4 | Transmit Power Level Command for the RACH message..... | <u>116</u> <u>114</u> |
| 10.6.2.4 | Random access collision | <u>116</u> <u>114</u> |
| 10.6.3 | Random access collision | <u>117</u> <u>115</u> |
| A.1 | Example Implementation of Closed Loop Uplink Power Control in Node B for 1.28 Mcps TDD..... | <u>117</u> <u>115</u> |
| A.2 | Example Implementation of Downlink Power Control in UE for 1.28 Mcps TDD when TSTD is used..... | <u>117</u> <u>115</u> |
| A.3 | Example Implementation of open Loop Power Control for access procedure for 1.28 Mcps TDD | <u>118</u> <u>116</u> |
| A.4 | Examples random access procedure for 1.28Mcps TDD..... | <u>118</u> <u>116</u> |
| 11 | Physical layer measurements | <u>120</u> <u>118</u> |
| 11.1 | Control of UE/UTRAN measurements..... | <u>120</u> <u>118</u> |
| 11.1.1 | General measurement concept..... | <u>120</u> <u>118</u> |
| 11.1.2 | Measurements for cell selection/reselection..... | <u>120</u> <u>118</u> |
| 11.1.3 | Measurements for Handover..... | <u>120</u> <u>119</u> |
| 11.1.4 | Measurements for DCA..... | <u>120</u> <u>119</u> |
| 11.1.5 | Measurements for timing advance..... | <u>121</u> <u>119</u> |
| 11.2 | Measurement abilities for UTRA TDD..... | <u>121</u> <u>119</u> |
| 11.2.1 | UE measurement abilities..... | <u>121</u> <u>119</u> |
| 11.2.1.1 | PCCPCH RSCP..... | <u>121</u> <u>119</u> |
| 11.2.1.2 | CPICH RSCP..... | <u>121</u> <u>119</u> |
| 11.2.1.3 | RSCP..... | <u>121</u> <u>119</u> |
| 11.2.1.4 | Timeslot ISCP..... | <u>121</u> <u>119</u> |
| 11.2.1.5 | UTRA carrier RSSI | <u>121</u> <u>119</u> |
| 11.2.1.6 | GSM carrier RSSI..... | <u>121</u> <u>119</u> |
| 11.2.1.7 | SIR | <u>121</u> <u>119</u> |
| 11.2.1.8 | CPICH Ec/No..... | <u>121</u> <u>119</u> |
| 11.2.1.9 | Physical channel BER..... | <u>121</u> <u>119</u> |
| 11.2.1.10 | Transport channel BLER..... | <u>121</u> <u>119</u> |
| 11.2.1.11 | UE transmitted power..... | <u>121</u> <u>119</u> |
| 11.2.1.12 | SFN-SFN observed time difference | <u>122</u> <u>120</u> |
| 11.2.1.13 | Observed time difference to GSM cell..... | <u>122</u> <u>120</u> |
| 11.2.1.14 | Timing Advance (T _{ADV}) for 1.28 Mcps TDD..... | <u>122</u> <u>120</u> |
| 11.2.2 | UTRAN measurement abilities | <u>122</u> <u>120</u> |
| 11.2.2.1 | RSCP..... | <u>122</u> <u>120</u> |
| 11.2.2.2 | Timeslot ISCP..... | <u>122</u> <u>120</u> |
| 11.2.2.3 | RSSI..... | <u>122</u> <u>120</u> |
| 11.2.2.4 | SIR | <u>122</u> <u>120</u> |
| 11.2.2.5 | Physical channel BER..... | <u>122</u> <u>120</u> |
| 11.2.2.6 | Transport channel BLER..... | <u>122</u> <u>120</u> |
| 11.2.2.7 | Transmitted carrier power..... | <u>122</u> <u>120</u> |
| 11.2.2.8 | Transmitted code power..... | <u>122</u> <u>120</u> |
| 11.2.2.9 | RX Timing Deviation | <u>123</u> <u>120</u> |
| 11.2.2.9.1 | Received SYNC-UL Timing Deviation for 1.28 Mcps TDD | <u>123</u> <u>121</u> |
| Annex A (informative): | Monitoring GSM from low chip rate TDD: Calculation Results | <u>124</u> <u>122</u> |
| 12 | Performance analysis of the low chip rate | <u>128</u> <u>126</u> |
| 13 | Examples of service mapping | <u>136</u> <u>134</u> |
| 14 | History | <u>146</u> <u>144</u> |

Foreword

This Technical Report has been produced by the 3GPP.

The contents of the present document are subject to continuing work within the TSG and may change following formal TSG approval. Should the TSG modify the contents of this TS, it will be re-released by the TSG with an identifying change of release date and an increase in version number as follows:

Version 3.y.z

where:

- x the first digit:
 - 1 presented to TSG for information;
 - 2 presented to TSG for approval;
 - 3 Indicates TSG approved document under change control.
- y the second digit is incremented for all changes of substance, i.e. technical enhancements, corrections, updates, etc.
- z the third digit is incremented when editorial only changes have been incorporated in the specification.

1 Scope

This Technical Report describes the 1.28Mcps functionality for UTRA TDD physical layer, identifies commonalties and explains the differences to the 3.84Mcps chip rate. Suggestions for alignment will be provided too.

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

?? References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.

?? For a specific reference, subsequent revisions do not apply.

?? For a non-specific reference, the latest version applies.

- [1] TS 25.201: "Physical Layer - General Description"
- [2] TS 25.221: "Physical channels and mapping of transport channels onto physical channels (TDD)"
- [3] TS 25.222: "Multiplexing and channel coding (TDD)"
- [4] TS 25.223: "Spreading and modulation (TDD)"
- [5] TS 25.224: "Physical layer procedures (TDD)"
- [6] TS 25.225: "Physical layer – Measurements (TDD)"

3 Abbreviations

For the purposes of the present document, the following abbreviations apply:

| | |
|------|-------------------------------|
| CDMA | Code Division Multiple Access |
| PN | Pseudo Noise |
| QPSK | Quadrature Phase Shift Keying |
| RACH | Random Access Channel |

4 Radio Requirements

4.1 Radio environments

The radio environment recommended by ITU like indoor environment, pedestrian environment, vehicular environment (120km/h) should be well supported by the low chip rate TDD option.

4.2 Services

As one option of TDD mode, the low chip rate option should provide the basic service (bearer service). For a IMT-2000 compliant system corresponding to ITU requirement, for the indoor environment, up to 2Mbps data service should be provided. And for outdoor pedestrian environment, the data service should be up to 384kbps and more. For the UE in moving environment (vehicular speed less than 120km/h), the data rate supported should be 384 and more kbps.

4.3 Operational requirements

The low chip rate TDD option should provide the flexibility to be used for high spot or high density area to provide high speed data service or to provide enhanced coverage or be used alone as macro cell to provide the service coverage. It should allow deployment together with FDD system, with high chip rate TDD system, and be similar as high chip rate TDD deploying with GSM.

4.3.1 Deployment scenarios

For the low chip rate TDD option, the deployment should be flexible for all the scenarios like macro cell, micro cell and pico cell, etc. and also should provide the fixed wireless access.

[Description:]

For the low chip rate TDD option, the deployment should be flexible for all the scenarios like macro cell, micro cell and pico cell, etc. and also should provide the fixed wireless access.

Dependent on the kind of interference accepted by the operator, the operator can vary the max. cell radius in a trade-off with UL - DL interference with the following limitations:

Table: Interference scenarios and the corresponding max. cell radius

| Case | Max. cell radius |
|--|------------------|
| no UpPTS – DwPTS interference allowed | 11.25 km |
| UpPTS – DwPTS interference allowed, but no interference to TS0 allowed | 22.5 km |
| no TS1 – DwPTS interference allowed, other interference allowed | 30 km |
| TS1 – DwPTS interference allowed, but no interference to TS0 allowed | 41.25 km |

[Rational:]

The guard period of 75 μ s between the DwPTS and the UpPTS is designed to avoid interference between the UpPTS (UL) and the DwPTS (DL). Therefore the cell size ensuring the interference free reception of the DwPTS is guaranteed to a size of approximately 10 km in radius (exact value 11.25 km, assuming no delay spread).

Consequently, for bigger cell radii there is a conflict that the advanced UpPTS interfering the DwPTS reception of another UE being close by.

Even though the UpPTS – DwPTS interference is possible for bigger cell radii then 11.25 km, the impact on the quality of service can be low and acceptable for an operator willing to operate bigger cells.

There are three reasons for that:

The probability that the a UE is close to another UE is low - especially for big cells

The DwPTS needs not to be received by every mobile in every frame. A few DwPTSs being not received during initial cell search mean no big degradation.

The UpPTS is not transmitted every frame it is only needed for random access or handover. So the probability of disturbance is rather low.

It is recommended that the operator avoids interference of TS1 to TS0 by means of the choice of the cell radius. This interference would mean permanent interference for TS0.

The operators can judge the trade-off between quality of service and range and select the range accordingly.

The maximum cell radius d_{max} is dependent on the time t_{gap} between the potentially interfering UL signal and the potentially interfered DL signal by to following equation:

$$d_{max} \approx \frac{c \cdot t_{gap}}{2}; c \text{ is velocity of light.}$$

The following table shows the possible trade-offs between cell radius and interference:

Allowed cell radius for the occurrence of the special UL - DL interference

| Potentially interfering UL signal | Potentially interfered DL signal | t_{gap} in μ s | d_{max} in km |
|-----------------------------------|----------------------------------|----------------------|-----------------|
| UpPTS | DwPTS | 75 | 11.25 |
| UpPTS | TS0 | 150 | 22.5 |
| TS1 | DwPTS | 200 | 30 |
| TS1 | TS0 | 275 | 41.25 |

[Explanation difference:]

For the high chip rate option there is no DwPTS – guard – UpPTS structure. Here, the UL time slots are following the DL time slots immediately. Thus, there is only one step in degree and quality of interference between DL and UL signals.

For the low chip rate option, it makes a difference in quality and degree whether the DwPTS or TS is interfered by the UpPTS or TS1. Hence the trade-off between cell range and interference is more manifold for the low chip rate option.

4.4 Handover and Cell selection/reselection

The low chip rate TDD option should support the handover between UTRA modes (e.g. low chip rate TDD to high chip rate TDD, low chip rate TDD to FDD), and between systems (e.g. low chip rate TDD to GSM, etc.).

4.5 Particular characteristics of the low chip rate TDD

The features of uplink synchronization, smart antenna (beam forming) etc. have been discussed. These features were agreed to be included in this technical report as they may provide potential performance improvement.

5 High level characteristics

| Parameter/Feature | Value/Expression | Note |
|--|--|----------------|
| Chip rate | 1.28 Mcps | |
| Modulation | QPSK (8PSK) | |
| Spreading Factor | 1/2/4/8/16 | |
| Nominal Channel Spacing | 1.6MHz / Carrier | |
| Burst Format | 1 burst type | |
| Radio Frame Length | 10ms (divided into 2 sub-frames) | |
| Sub-frame length | 5ms | |
| Number of traffic Time-time slots number (traffic) | 7 | |
| Time slot length (us) | 675 | |
| Downlink pilot slot (us) | 75 | DwPTS |
| Uplink pilot slot (us) | 125 | UpPTS |
| Guard Period (us) | 75 | GP After DwPTS |
| Range of uplink slot | 1 – 6 | |
| Range of downlink slot | 1 – 6 | |
| Receiver type | Multi-user Detection (option), Rake | |
| Pilot aided detection | DwPTS, UpPTS, Midamble | |
| Synchronization aspect | Downlink and uplink synchronization | |
| Precision for UL sync. | 1/8 chip | |
| Antenna processing | Smart antenna with beam forming | Option |
| Switching point | Two switching points / sub-frame | |
| Power control / rate | Open loop power control Closed loop power control / 200Hz (max rate) | |
| Variable bit rate service | Supported (using TFCI) | |
| Basic resource unit | One code, one slot with Spreading factor =16 (use of same resource in both consecutive sub-frames) | |
| Service mapping | Multi-code, multi-slot combination (variable spreading factor) | |
| Interleaving period | 10/20/40/80ms | |
| HO capability | Low chip rate TDD to High chip rate TDD, FDD, | |

| | | |
|--------------|--|--------------------------------|
| | GSM, etc. | |
| Tx Diversity | <p>same capability as high chip rate TDD for DwPTS <u>DwPCH, DPCH and P-CCPCH, and TSTD</u> can also be applied to P-CCPCH, <u>DwPCH and DPCH (optional)</u>, but not for P-CCPCH; the Tx Diversity scheme used for the DPCH is used for the FPACH, as well.</p> | Refer to sub clause 10.5 of TR |

6 Physical layer - General description

6.1 General description of Layer 1

Common with the high chip rate TDD mode

6.1.2 Service provided to higher layers

The physical layer offers data transport services to higher layers. The access to these services is through the use of transport channels via the MAC sub-layer. In addition to the functions listed in TS25.201, the physical layer for the low chip rate TDD option is expected to perform the following functions in order to provide the data transport service:

- beamforming
- synchronisation shift control

6.2 Document structure of the physical layer specification

6.2.1 Multiple Access

In contrast to the high chip rate TDD option, the access scheme is Direct-Sequence Code Division Multiple Access (DS-SS) with information spread over approximately 1.6 MHz bandwidth only, thus also often denoted as low chip rate TDD option due that nature.

The frame structure of the low chip rate options differs from the high chip rate option in the following way: A 10 ms radio frame is divided into 2 sub-frames of 5ms. The frame structure (e.g. switching points) for each sub-frame in the 10ms frame length is the same. The sub-frame is divided into 7 traffic slots (864 chip/slot at the chip rate 1.28 Mcps) as described in subclause 7.2.1 'Frame Structure' and 3 timeslots with special functionality.

The information rate of the channel is different from the high chip rate option and varies with the symbol rate being derived from the 1.28 Mcps chip rate, the spreading factor and the modulation mode.

6.2.2 Channel coding and interleaving

Common with the high chip rate TDD mode

6.2.3 Modulation and spreading

The ordinary modulation scheme is QPSK, as for the the high chip rate option. In addition to that 8PSK is also possible.

For separating different cells the following solutions are additionally supported in the low chip rate option:

- SYNC sequences, ~~SYNC~~ SYNC-UL sequences.

For separating different UEs the following code families are additionally defined:

- ~~SYNC1~~ SYNC-UL sequences

6.2.4 Physical layer procedures

There are several physical layer procedures involved with low chip rate TDD operation that are different and in addition to the high chip rate option. Such procedures covered by physical layer description are:

- 1) The power control, for low chip rate TDD mode close loop control in both uplink and downlink.
- 2) Cell search operation.
- 3) Uplink synchronisation for low chip rate TDD mode.
- 4) Random access
- 5) Beamforming (optional)

6.2.5 Physical layer measurements

Common with the high chip rate TDD mode

[Explanation difference to section 6]

Most of the physical characters of the low chip rate TDD option are same as the high chip rate TDD option. But due to the different operation frequency band width and some other different implementation consideration such as power control method, uplink synchronization, there still exist some difference and all these differences will be discussed in the main part of TR25.928.

7 Physical channels and mapping of transport channels onto physical channels

7.1 Transport channels

7.1.1 Transport channels

'Common with the high chip rate TDD mode'

7.2 Physical channels

7.2.1 Frame structure

[Description:]

For low chip rate option, the frame length is 10ms and the 10ms frame is divided into 2 sub-frames of 5ms. The frame structure for each sub-frame in the 10ms frame length is the same.

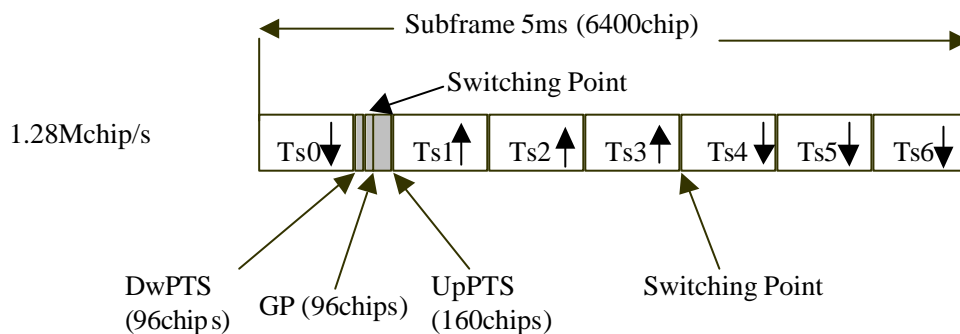


Figure Structure of the sub-frame for low chip rate option

The frame structure for each sub-frame is shown in Figure above.

T_{sn} (n from 0 to 6): the nth normal-traffic time slot, 864 chips duration;

DwPTS: downlink pilot time slot, 96 chips duration;

UpPTS: uplink pilot time slot, 160 chips duration;

GP: main guard period for TDD operation, 96 chips duration;

[Rationale:]

In the figure above, the total number of normal-traffic time-slots for uplink and downlink is 7, and the length for each normal-traffic time-slot is 864 chips duration. Among the 7 normal-traffic time-slot, Ts#0 is always allocated as downlink while Ts#1 is always allocated as uplink. The time slots for the uplink and the downlink are separated by a switching point. Between the downlink time slots and uplink time slots, the special period is the switching point to separate the uplink and downlink. In each sub-frame of 5ms for low chip rate option,

there are two switching points (uplink to downlink and vice versa). The proposed frame structure has taken some new technologies into consideration, either the smart antenna (beam forming) technology or the uplink synchronisation will be well supported.

Using the above frame structure, the low chip rate TDD option can operate on both symmetric and asymmetric mode by properly configuring the number of downlink and uplink time slots; (note that whatever the time slot configuration will be, the GP and DwPTS position within the frame should not change in order not to desynchronise the UEs and in order to allow Node B on air synchronisation procedures which make use of the DwPTS channel). It should be noted that in asymmetric operation mode, at least one normal-traffic uplink time slot and one downlink time slot will be allocated for traffic (Ts#0 for downlink and Ts#1 for uplink). The guard period GP of 96 chips can support the cell radius d up to about 11 km for uplink synchronization operation where the uplink transmission is advanced in macro-, micro- and pico- cell of small cells in cities or large cells in rural areas. Here the GP insures that an UE transmitting the UpPTS does not disturb the reception of the DwPTS for other UEs being close by. If this distortion is accepted in the network the cell radius can be bigger. (Note that the UpPTS is not continuously transmitted and the DwPTS is not continuously received.)

The only difference to the last version of the frame structure proposal for low chip rate is the improving of the numbering of the time slots. The physical layer behaviour does not change.

[Explanation of difference:]

For both high chip rate option and low chip rate option, the frame length is 10 ms , But for low chip rate option the 10 ms length is divided into 2 sub-frame of 5 ms to allow the fast update of power control, uplink synchronization, and smart antenna beamforming.

For high chip rate option , each 10 ms frame consists of 15 time slots, each allocated to either the uplink or the downlink . So it has both single and multiple-switching point configuration both for symmetric and asymmetric allocation. While in the low chip rate option, the position of the big Guard Period GP and of the DwPTS and UpPTS physical channels, is always between Ts0 and Ts1 whatever the level of asymmetry be.

7.2.2 Dedicated physical channel (DPCH)

7.2.2.1 Spreading

'Common with the high chip rate TDD mode'

7.2.2.2 Burst Types

[Description:]

In correspondence to the frame structure described above, the burst structures for Ts_n, DwPTS and UpPTS are proposed. The burst structure for normal-traffic time slot (Ts_{#n}) is described in Figure below.

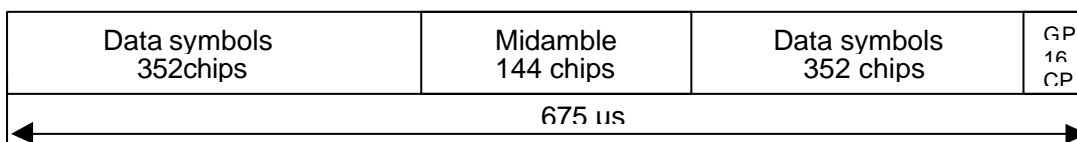


Figure Burst structure for normal-traffic time slot

The structure for DwPTS and UpPTS is described in Figures below.

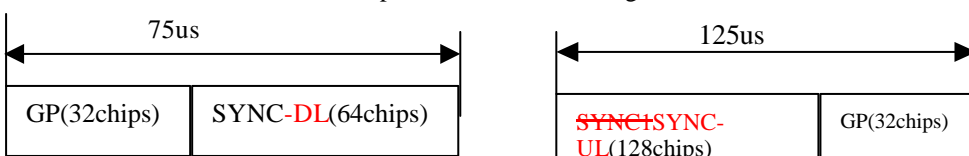


Figure Structure for DwPTS

Figure Structure for UpPTS

[Rationale:]

In the burst structure figure, the data symbols in each side of the midamble are 352 chips. The TPC bits for power control, the TFCI bits and the additional uplink synchronization bits (synchronization shift) are included in the Data symbols fields of the burst if they are needed. The amount of TFCI bits used is depending on the service and the details for TFCI, synchronization shift and TPC bits should be provided later with service mapping. For the power control symbols, the uplink synchronization control symbols and the TFCI the symbols around the midamble are used.

The GP field in the same figure for each time slot is used for protection between time slots to avoid the long delay multi-path interference. It should be noted that the GP of the TS0 together with the guard period in DwPTS is 48 chips long which is different with other normal guard period of 16 chips between time slots. This 'super long' guard period can be used to avoid the interference between the last ~~normal~~ downlink ~~traffic~~ time slot and the downlink synchronization pilot burst. Otherwise, the interference to the last downlink time slot from the strong powered pilot will be serious to the traffic; and vice versa, the interference to the downlink pilot burst from the last downlink time slot will decrease the performance on downlink synchronization and cell search. Note that if the UEs serving Node B is far away and the UE makes handover measurements it will receive the beginning of the DwPTS of a close by Node B inside these 48 chip. 48 chip corresponds to 11 km difference in distance to the Node B. If the other Node B is more distant to the serving Node B, big guard period can be used for receiving the DwPTS of the handover candidate Node B.

In DwPTS and UpPTS, the content of ~~SYNC~~ ~~SYNC-DL~~ and ~~SYNC1~~ ~~SYNC-UL~~ field are used for downlink and uplink pilot. The GP fields are used to separate the downlink (uplink) pilot from the ~~normal~~ ~~traffic~~ downlink (uplink) time slot.

It should be pointed out that the uplink synchronization burst (~~SYNC1~~ ~~SYNC-UL~~) is not followed by a RACH immediately. First the UL synchronization burst UpPTS is sent by the UE. This UpPTS is used for Node B to determine the received power level and the received timing. Second, the Node B transmits timing and power control information to the UE using the FPACH (one burst message) within the next 4 ~~sub~~-frames. Then the P-RACH is transmitted. ~~Both~~ ~~The~~ ~~FPACH~~ ~~and~~ ~~P-RACH~~ ~~are~~ ~~is~~ carrying single burst messages transmitted on a ~~normal~~ traffic time slot (see Burst structure figure). This two phase procedure which is different with the GSM of one phase procedure has better performance than the classical approach as used in GSM. In this case, the ~~normal~~ traffic burst and access burst can be active in the same time slot and the interference is reduced for each other if they are time-aligned.

Note that the UpPTS has to be transmitted by the UE in advance (starting in the big GP) to arrive at the Node B at the position indicated in the burst structure figure. The UpPTS can also be received at a different position if the UE cannot or does not aim at the RX position indicated in the burst structure figure. Thus, the UpPTS can also start within the guard interval (RX, TX), depending on the situation in the system. This means relaxation to estimate timing in UE, e.g. from pathloss on P-CCPCH.

And the proposed frame structure can support all the environments of macro-, micro- and pico- cells. In vehicular environment, the speed can be more than 120km/h. Also in the proposed frame structure, some specific properties for low chip rate option such as smart antenna technology, uplink synchronisation, beamforming, etc can be well supported.

[Explanation difference:]

In high chip rate option, there are 2 burst types of DPCH. They have different midamble lengths. And there is only one burst type of DPCH in the low chip rate option. The use of the same burst structure for RACH and for traffic will guarantee that the RACH can be handled with conventional traffic on the same UL time slots since the RACH is already UL synchronised.

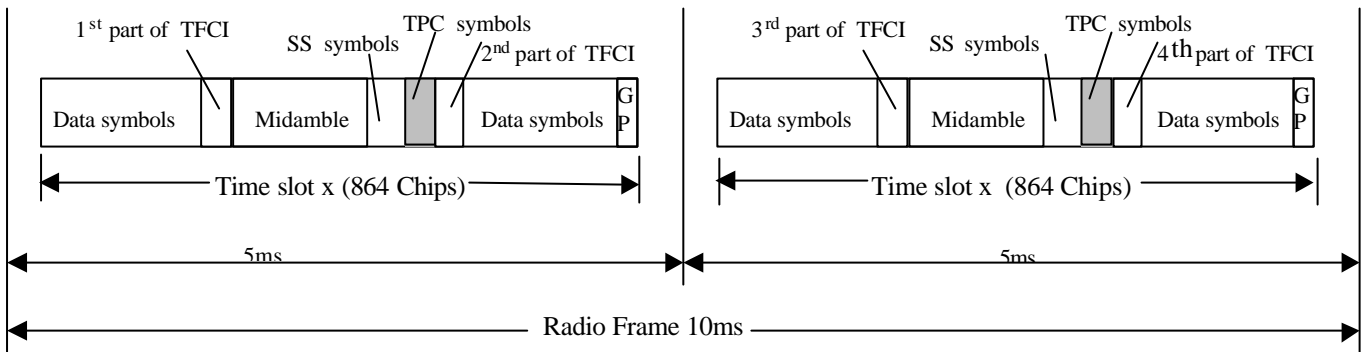
7.2.2.2.1 Transmission of TFCI

[Description:]

There is only one burst type for **normal-traffic** time slot in the low chip rate option. It provides the possibility for transmission of TFCI both in up- and downlink. For every user the TFCI information is to be transmitted once per 10ms radioframe. If no TPC and SS are applied, the TFCI information is to be transmitted directly adjacent to the midamble of the 5ms subframe of the assigned frame. The position in case of TPC and/or SS application is shown in the figures below.

[Rationale:]

There is only one burst type for **normal-traffic** time slot in the low chip rate option. It provides the possibility for transmission of TFCI both in up- and downlink. For every user the TFCI information is to be transmitted once per 10ms radioframe. The transmission of TFCI is negotiated at call setup and can be re-negotiated during the call. For each CTrCH it is indicated by higher layer signalling, which TFCI format is applied. Additionally for each allocated timeslot it is signalled individually whether that timeslot carries the TFCI or not. If a time slot contains the TFCI, then it is always transmitted using the first allocated channelisation code in the timeslot,



Position of TFCI information in the traffic burst in case of L1 control signals

according to the order in the higher

layer allocation message. The transmission of TFCI is done in the data parts of the respective physical channel, this means TFCI and data bits are subject to the same spreading procedure. The encoded TFCI symbols are both equally distributed between the subframes and between the data blocks. Hence the midamble structure and length is not changed. If no TPC and SS are applied, the TFCI information is to be transmitted directly adjacent to the midamble of the 5ms subframe of the assigned frame. The position in case of TPC and/or SS application is shown in the figures above. Figure above shows the position of the TFCI in a traffic burst, if L1 control signals, SS (synchronization shift) and TPC (Transmit Power Control), is transmitted.

[Explanation difference:]

In high chip rate option, both burst types 1 and 2 provide the possibility for transmission of TFCI both in up- and downlink. The TFCI information is to be transmitted directly adjacent to the midamble if no TPC is transmitted. In the low chip rate option, there is only one burst type for **normal-traffic** time slot. It provides the possibility for transmission of TFCI both in up- and downlink. For every user the TFCI information is to be transmitted once per 10ms radioframe. The TFCI information is to be transmitted directly adjacent to the midamble of the 5ms subframe of the assigned frame if no TPC and SS is applied. The position of the TFCI in case of TPC and/or SS transmission is analogous to the high chiprate option and depicted in figure above.

7.2.2.2.2 Transmission of TPC

[Description:]

There is only one burst type for **normal-traffic** time slot in the low chip rate option. It provides the possibility for transmission of L1 control signal "TPC" both in up- and downlink. For every user the TPC information is to be transmitted once per 5ms subframe.

[Rational:]

Hence the midamble structure and length is not changed. The TPC information is to be transmitted directly after SS. Figure below shows the position of the TPC in a traffic burst.

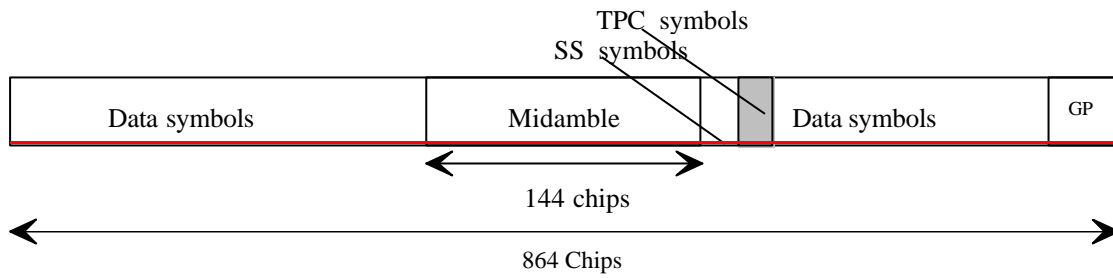


Figure : Position of TPC information in the traffic burst

For the number of layer 1 symbols there are 3 possibilities configurable for each channelisation code during the call setup:

1) one SS and TPC symbol

2) no SS and TPC symbols

3) 16/SF SS and 16/SF TPC symbols (note: there is a need to study this further)

The burst type for dedicated channels provides the possibility for transmission of TPC in uplink and downlink.

The transmission of TPC is done in the data parts of the traffic burst. Hence the midamble structure and length is not changed. The TPC information is to be transmitted directly after the SS information, which is transmitted after the midamble. Figure 25 shows the position of the TPC command in a traffic burst.

For every user the TPC information is to be transmitted at least once per 5ms sub-frame. If applied, transmission of TPC is done in the data parts of the traffic burst and it can be transmitted using the first allocated channelisation code and the first allocated timeslot (according to the order in the higher layer allocation message). Other allocations (more than one TPC transmission in one sub-frame) of TPC are also possible. The TPC is spread with the same spreading factor (SF) and spreading code as the data parts of the respective physical channel.

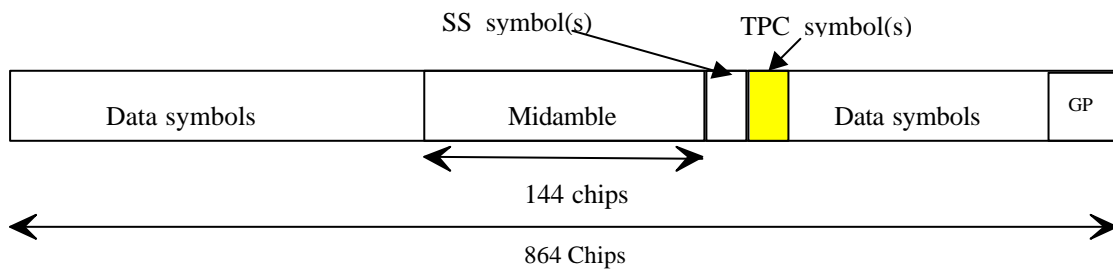


Figure 25: Position of TPC information in the traffic burst in downlink and uplink

For the number of layer 1 symbols per channelisation code there are 3 possibilities for each channelisation code, configured by higher layers:

- 1) one SS and one TPC symbol
- 2) no SS and no TPC symbols
- 3) 16/SF SS and 16/SF TPC symbols

So, in case 3), when SF=1, there are 16 TPC symbols which correspond to 32 bits (for QPSK) and 48 bits (for 8PSK).

In the following the uplink is described only. For the description of the downlink, downlink (DL) and uplink (UL) have to be interchanged.

Each of the TPC symbols for uplink power control in the DL will be associated with an UL time slot and an UL CCH pair. This association varies with

- ?? the number of allocated UL time slots and UL CCHs on these time slots (time slot and CCH pair) and
- ?? the allocated TPC symbols in the DL.

In case a UE has

~~more than one channelisation code~~

and/or

~~channelisation codes being of lower spreading factor than 16 and using 16/SF SS and 16/SF TPC symbols.~~

the TPC commands for each ULtime slot CCH pair (all channelisation codes on that time slot belonging to the same time slot and CCH pair have the same TPC command) will be distributed to the following rules:

1. The ULtime slots and CCH pairs the TPC commands are intended for will be numbered from the first to the last ULtime slot and CCH pair allocated to the regarded UE (starting with 0). The number of a time slot and CCH pair is smaller than the number of another time slot and CCH pair within the same time slot if its spreading code with the lowest SC number according to the following table has a lower SC number than the spreading code with the lowest SC number of the other time slot and CCH pair.
2. The commanding TPC symbols on all DL CCHs allocated to one UE are numbered consecutively starting with zero according to the following rules:
 - a) The numbers of the TPC commands of a regarded DL time slot are lower than those of DL time slots being transmitted after that time slot
 - b) Within a DL time slot the numbers of the TPC commands of a regarded channelisation code are lower than those of channelisation codes having a higher spreading code number

The spreading code number is defined by the following table (see[8]):

| SC number | SF (Q) | Walsh code number (k) |
|-----------|--------|------------------------|
| 0 | 16 | $c_{Q^{?16}}^{(k?1)}$ |
| | ... | |
| 15 | 16 | $c_{Q^{?16}}^{(k?16)}$ |
| 16 | 8 | $c_{Q^{?8}}^{(k?1)}$ |
| | ... | |
| 23 | 8 | $c_{Q^{?8}}^{(k?8)}$ |
| 24 | 4 | $c_{Q^{?4}}^{(k?1)}$ |
| | ... | |
| 27 | 4 | $c_{Q^{?4}}^{(k?4)}$ |
| 28 | 2 | $c_{Q^{?2}}^{(k?1)}$ |

| | | |
|-----------|----------|-------------------|
| <u>29</u> | <u>2</u> | $c_{Q?2}^{(k?2)}$ |
| <u>30</u> | <u>1</u> | $c_{Q?1}^{(k?1)}$ |

Note: Spreading factors 2-8 are not used in DL

c) Within a channelisation code numbers of the TPC commands are lower than those of TPC commands being transmitted after that time

The following equation is used to determine the UL time slot which is controlled by the regarded TPC symbol in the DL:

$$UL_{pos} = (SFN' \cdot N_{UL_TPCsymbols} + TPC_{DLpos}) \bmod (N_{ULslot})$$

where

UL_{pos} is the number of the controlled uplink time slot and CCTrCH pairs.

SFN' is the system frame number counting the sub-frames. The system frame number of the radio frames (SFN) can be derived from SFN' by

SFN = SFN' div 2, where div is the remainder free division operation.

N_{UL_TPCsymbols} is the number of UL TPC symbols in a sub-frame.

TPC_{DLpos} is the number of the regarded UL TPC symbol in the DL within the sub-frame.

N_{ULslot} is the number of UL slots and CCTrCH pairs in a frame.

In Annex G two examples of the association of TPC commands to time slots and CCTrCH pairs are shown.

Coding of TPC: The relationship between the TPC Bits and the transmitter power control command for QPSK is the same as in the 3.84Mcps TDD cf. [5.2.2.5 'Transmission of TPC'].

The relationship between the TPC Bits and the transmitter power control command for 8PSK is given in table [12]

Table 12: TPC Bit Pattern for 8PSK

| <u>TPC Bits</u> | <u>TPC command</u> | <u>Meaning</u> |
|-----------------|--------------------|--------------------------|
| <u>000</u> | <u>'Down'</u> | <u>Decrease Tx Power</u> |
| <u>110</u> | <u>'Up'</u> | <u>Increase Tx Power</u> |

[Explanation difference:]

In high chip rate option, both burst types 1 and 2 provide the possibility for transmission of TPC only in uplink.

While in the low chip rate option, there is only one burst type for ~~normal-traffic~~ time slot. For the number of layer 1 symbols there are 3 possibilities configurable for each channelisation code during the call setup. It provides the possibility for transmission of TPC both in up- and downlink. For every user the TPC information is to be transmitted once per 5ms subframe. So it gives faster power control functionality in the low chip rate option than it does in high chip rate option. This is advantageous, because the lower chip rate has less frequency diversity which can be compensated with faster control algorithms. The smart antenna feature increases the demand on the speed of the control algorithms, because the smart antenna algorithms tend to focus on one DOA which has more Rayleigh fading than all DOAs received at a single antenna.

Note: This is to be verified by performance analysis

7.2.2.2.3 Timeslot formats

[Description:]

The timeslot format depends on the spreading factor, midamble length, the TPC and SS signals presence and on the number of the TFCI bits. In the case that L1 signals is used, different amount of bits are mapped to the two data fields. For the transmission of the TPC/SS, there are three possible configurations for the number of TPC/SS symbols:

1. 1 symbol TPC and 1 symbol SS
2. No TPC and No SS.
3. 16/SF symbol TPC and 16/SF symbol SS.

So, in case 3 , when SF=1 , the number of TPC/SS is 16 symbol corresponding 32 bits (for QPSK) and 48 bits (for 8PSK).

16/SF TPC/SS symbols is for the case that the number of L1 signalling bits of one given RU after spreading are same although different SFs are used. Thus, the mapping of user data on the payload can stay the same regardless what the spreading factor is.

The timeslot formats are depicted in the following subclause.

7.2.2.3.1 Timeslot formats for Downlink

Table : Time slot formats for the Downlink

| Slot Format # | Spreading Factor | Midamble length (chips) | N_{TFCI} (bits) | $N_{\text{SS}} \& N_{\text{TPC}}$ (bits) | Bits/slot | $N_{\text{Data/Slot}}$ (bits) | $N_{\text{data/data field(1)}}$ (bits) | $N_{\text{data/data field(2)}}$ (bits) |
|---------------|------------------|-------------------------|--------------------------|--|-----------|-------------------------------|--|--|
| 0 | 16 | 144 | 0 | 0 & 0 | 88 | 88 | 44 | 44 |
| 1 | 16 | 144 | 4 | 0 & 0 | 88 | 86 | 42 | 44 |
| 2 | 16 | 144 | 8 | 0 & 0 | 88 | 84 | 42 | 42 |
| 3 | 16 | 144 | 16 | 0 & 0 | 88 | 80 | 40 | 40 |
| 4 | 16 | 144 | 32 | 0 & 0 | 88 | 72 | 36 | 36 |
| 5 | 16 | 144 | 0 | 2 & 2 | 88 | 84 | 44 | 40 |
| 6 | 16 | 144 | 4 | 2 & 2 | 88 | 82 | 42 | 40 |
| 7 | 16 | 144 | 8 | 2 & 2 | 88 | 80 | 42 | 38 |
| 8 | 16 | 144 | 16 | 2 & 2 | 88 | 76 | 40 | 36 |
| 9 | 16 | 144 | 32 | 2 & 2 | 88 | 68 | 36 | 32 |
| 10 | 1 | 144 | 0 | 0 & 0 | 1408 | 1408 | 704 | 704 |
| 11 | 1 | 144 | 4 | 0 & 0 | 1408 | 1406 | 702 | 704 |
| 12 | 1 | 144 | 8 | 0 & 0 | 1408 | 1404 | 702 | 702 |

| Slot Format # | Spreading Factor | Midamble length (chips) | N_{TFCI} (bits) | N_{SS} & N_{TPC} (bits) | Bits/slot | $N_{Data/Slot}$ (bits) | $N_{data/data\ field(1)}$ (bits) | $N_{data/data\ field(2)}$ (bits) |
|---------------|------------------|-------------------------|-------------------|-----------------------------|-----------|------------------------|----------------------------------|----------------------------------|
| 13 | 1 | 144 | 16 | 0 & 0 | 1408 | 1400 | 700 | 700 |
| 14 | 1 | 144 | 32 | 0 & 0 | 1408 | 1392 | 696 | 696 |
| 15 | 1 | 144 | 0 | 2 & 2 | 1408 | 1404 | 704 | 700 |
| 16 | 1 | 144 | 4 | 2 & 2 | 1408 | 1402 | 702 | 700 |
| 17 | 1 | 144 | 8 | 2 & 2 | 1408 | 1400 | 702 | 698 |
| 18 | 1 | 144 | 16 | 2 & 2 | 1408 | 1396 | 700 | 696 |
| 19 | 1 | 144 | 32 | 2 & 2 | 1408 | 1388 | 696 | 692 |
| 20 | 1 | 144 | 0 | 32 & 32 | 1408 | 1344 | 704 | 640 |
| 21 | 1 | 144 | 4 | 32 & 32 | 1408 | 1342 | 702 | 640 |
| 22 | 1 | 144 | 8 | 32 & 32 | 1408 | 1340 | 702 | 638 |
| 23 | 1 | 144 | 16 | 32 & 32 | 1408 | 1336 | 700 | 636 |
| 24 | 1 | 144 | 32 | 32 & 32 | 1408 | 1328 | 696 | 632 |

| Slot Format # | Spreading Factor | Midamble length (chips) | N_{TFCI} (bits) | N_{SS} & N_{TPC} (bits) | Bits/slot | $N_{Data/Slot}$ (bits) | $N_{data/data\ field(1)}$ (bits) | $N_{data/data\ field(2)}$ (bits) |
|---------------|------------------|-------------------------|-------------------|-----------------------------|-----------|------------------------|----------------------------------|----------------------------------|
| 0 | 16 | 144 | 0 | 0 & 0 | 88 | 88 | 44 | 44 |

| Slot Format # | Spreading Factor | Midamble length (chips) | N_{TECL} (bits) | N_{SS} & N_{TFC} (bits) | Bits/slot | $N_{Data/Slot}$ (bits) | $N_{data/data_field(1)}$ (bits) | $N_{data/data_field(2)}$ (bits) |
|---------------|------------------|-------------------------|-------------------|-----------------------------|-----------|------------------------|----------------------------------|----------------------------------|
| 1 | 16 | 144 | 4 | 0 & 0 | 88 | 84 | 42 | 42 |
| 2 | 16 | 144 | 8 | 0 & 0 | 88 | 80 | 40 | 40 |
| 3 | 16 | 144 | 16 | 0 & 0 | 88 | 72 | 36 | 36 |
| 4 | 16 | 144 | 32 | 0 & 0 | 88 | 56 | 28 | 28 |
| 5 | 16 | 144 | 0 | 2 & 2 | 88 | 84 | 44 | 40 |
| 6 | 16 | 144 | 4 | 2 & 2 | 88 | 80 | 42 | 38 |
| 7 | 16 | 144 | 8 | 2 & 2 | 88 | 76 | 40 | 36 |
| 8 | 16 | 144 | 16 | 2 & 2 | 88 | 68 | 36 | 32 |
| 9 | 16 | 144 | 32 | 2 & 2 | 88 | 52 | 28 | 24 |
| 10 | 4 | 144 | 0 | 0 & 0 | 1408 | 1408 | 704 | 704 |
| 11 | 4 | 144 | 4 | 0 & 0 | 1408 | 1404 | 702 | 702 |
| 12 | 4 | 144 | 8 | 0 & 0 | 1408 | 1400 | 700 | 700 |
| 13 | 4 | 144 | 16 | 0 & 0 | 1408 | 1392 | 696 | 696 |
| 14 | 4 | 144 | 32 | 0 & 0 | 1408 | 1376 | 688 | 688 |
| 15 | 4 | 144 | 0 | 2 & 2 | 1408 | 1404 | 704 | 700 |
| 16 | 4 | 144 | 4 | 2 & 2 | 1408 | 1400 | 702 | 698 |

| Slot Format # | Spreading Factor | Midamble length (chips) | N_{TECL} (bits) | $N_{SS} & N_{TPC}$ (bits) | Bits/slot | $N_{Data/Slot}$ (bits) | $N_{data/data\ field(1)}$ (bits) | $N_{data/data\ field(2)}$ (bits) |
|---------------|------------------|-------------------------|-------------------|---------------------------|-----------|------------------------|----------------------------------|----------------------------------|
| 17 | 4 | 144 | 8 | 2 & 2 | 1408 | 1396 | 700 | 696 |
| 18 | 4 | 144 | 16 | 2 & 2 | 1408 | 1388 | 696 | 692 |
| 19 | 4 | 144 | 32 | 2 & 2 | 1408 | 1372 | 688 | 684 |
| 20 | 4 | 144 | 0 | 32 & 32 | 1408 | 1344 | 704 | 640 |
| 21 | 4 | 144 | 4 | 32 & 32 | 1408 | 1340 | 702 | 638 |
| 22 | 4 | 144 | 8 | 32 & 32 | 1408 | 1336 | 700 | 636 |
| 23 | 4 | 144 | 16 | 32 & 32 | 1408 | 1328 | 696 | 632 |
| 24 | 4 | 144 | 32 | 32 & 32 | 1408 | 1312 | 688 | 624 |

7.2.2.2.3.2 Timeslot formats for Uplink

Table : Time slot formats for the Uplink

| Slot Format # | Spreading Factor | Midamble length (chips) | N_{TECL} (bits) | $N_{SS} & N_{TPC}$ (bits) | Bits/slot | $N_{Data/Slot}$ (bits) | $N_{data/data\ field(1)}$ (bits) | $N_{data/data\ field(2)}$ (bits) |
|---------------|------------------|-------------------------|-------------------|---------------------------|-----------|------------------------|----------------------------------|----------------------------------|
| 0 | 16 | 144 | 0 | 0 & 0 | 88 | 88 | 44 | 44 |
| 1 | 16 | 144 | 4 | 0 & 0 | 88 | 86 | 42 | 44 |
| 2 | 16 | 144 | 8 | 0 & 0 | 88 | 84 | 42 | 42 |

| Slot Format # | Spreading Factor | Midamble length (chips) | N_{TFCI} (bits) | N_{SS} & N_{TPC} (bits) | Bits/slot | $N_{Data/Slot}$ (bits) | $N_{data/data\ field(1)}$ (bits) | $N_{data/data\ field(2)}$ (bits) |
|---------------|------------------|-------------------------|-------------------|-----------------------------|-----------|------------------------|----------------------------------|----------------------------------|
| 3 | 16 | 144 | 16 | 0 & 0 | 88 | 80 | 40 | 40 |
| 4 | 16 | 144 | 32 | 0 & 0 | 88 | 72 | 36 | 36 |
| 5 | 16 | 144 | 0 | 2 & 2 | 88 | 84 | 44 | 40 |
| 6 | 16 | 144 | 4 | 2 & 2 | 88 | 82 | 42 | 40 |
| 7 | 16 | 144 | 8 | 2 & 2 | 88 | 80 | 42 | 38 |
| 8 | 16 | 144 | 16 | 2 & 2 | 88 | 76 | 40 | 36 |
| 9 | 16 | 144 | 32 | 2 & 2 | 88 | 68 | 36 | 32 |
| 10 | 8 | 144 | 0 | 0 & 0 | 176 | 176 | 88 | 88 |
| 11 | 8 | 144 | 4 | 0 & 0 | 176 | 174 | 86 | 88 |
| 12 | 8 | 144 | 8 | 0 & 0 | 176 | 172 | 86 | 86 |
| 13 | 8 | 144 | 16 | 0 & 0 | 176 | 168 | 84 | 84 |
| 14 | 8 | 144 | 32 | 0 & 0 | 176 | 160 | 80 | 80 |
| 15 | 8 | 144 | 0 | 2 & 2 | 176 | 172 | 88 | 84 |
| 16 | 8 | 144 | 4 | 2 & 2 | 176 | 170 | 86 | 84 |
| 17 | 8 | 144 | 8 | 2 & 2 | 176 | 168 | 86 | 82 |
| 18 | 8 | 144 | 16 | 2 & 2 | 176 | 164 | 84 | 80 |

| <u>Slot Format #</u> | <u>Spreading Factor</u> | <u>Midamble length (chips)</u> | <u>N_{TFCI} (bits)</u> | <u>N_{SS} & N_{TPC} (bits)</u> | <u>Bits/slot</u> | <u>N_{Data/Slot} (bits)</u> | <u>N_{data/data field(1)} (bits)</u> | <u>N_{data/data field(2)} (bits)</u> |
|----------------------|-------------------------|--------------------------------|--------------------------------|--|---------------------|-------------------------------------|--|--|
| 19 | 8 | 144 | 32 | 2 & 2 | 176 | 156 | 80 | 76 |
| 20 | 8 | 144 | 0 | 4 & 4 | 176 | 168 | 88 | 80 |
| 21 | 8 | 144 | 4 | 4 & 4 | 176 | 166 | 86 | 80 |
| 22 | 8 | 144 | 8 | 4 & 4 | 176 | 164 | 86 | 78 |
| 23 | 8 | 144 | 16 | 4 & 4 | 176 | 160 | 84 | 76 |
| 24 | 8 | 144 | 32 | 4 & 4 | 176 | 152 | 80 | 72 |
| 25 | 4 | 144 | 0 | 0 & 0 | 352 | 352 | 176 | 176 |
| 26 | 4 | 144 | 4 | 0 & 0 | 352 | 350 | 174 | 176 |
| 27 | 4 | 144 | 8 | 0 & 0 | 352 | 348 | 174 | 174 |
| 28 | 4 | 144 | 16 | 0 & 0 | 352 | 344 | 172 | 172 |
| 29 | 4 | 144 | 32 | 0 & 0 | 352 | 336 | 168 | 168 |
| 30 | 4 | 144 | 0 | 2 & 2 | 352 | 348 | 176 | 172 |
| 31 | 4 | 144 | 4 | 2 & 2 | 352 | 346 | 174 | 172 |
| 32 | 4 | 144 | 8 | 2 & 2 | 352 | 344 | 174 | 170 |
| 33 | 4 | 144 | 16 | 2 & 2 | 352 | 340 | 172 | 168 |
| 34 | 4 | 144 | 32 | 2 & 2 | 352 | 332 | 168 | 164 |

| <u>Slot Format #</u> | <u>Spreading Factor</u> | <u>Midamble length (chips)</u> | <u>N_{TFCI} (bits)</u> | <u>N_{SS} & N_{TPC} (bits)</u> | <u>Bits/slot</u> | <u>N_{Data/Slot} (bits)</u> | <u>N_{data/data field(1)} (bits)</u> | <u>N_{data/data field(2)} (bits)</u> |
|----------------------|-------------------------|--------------------------------|--------------------------------|--|---------------------|-------------------------------------|--|--|
| 35 | 4 | 144 | 0 | 8 & 8 | 352 | 336 | 176 | 160 |
| 36 | 4 | 144 | 4 | 8 & 8 | 352 | 334 | 174 | 160 |
| 37 | 4 | 144 | 8 | 8 & 8 | 352 | 332 | 174 | 158 |
| 38 | 4 | 144 | 16 | 8 & 8 | 352 | 328 | 172 | 156 |
| 39 | 4 | 144 | 32 | 8 & 8 | 352 | 320 | 168 | 152 |
| 40 | 2 | 144 | 0 | 0 & 0 | 704 | 704 | 352 | 352 |
| 41 | 2 | 144 | 4 | 0 & 0 | 704 | 702 | 350 | 352 |
| 42 | 2 | 144 | 8 | 0 & 0 | 704 | 700 | 350 | 350 |
| 43 | 2 | 144 | 16 | 0 & 0 | 704 | 696 | 348 | 348 |
| 44 | 2 | 144 | 32 | 0 & 0 | 704 | 688 | 344 | 344 |
| 45 | 2 | 144 | 0 | 2 & 2 | 704 | 700 | 352 | 348 |
| 46 | 2 | 144 | 4 | 2 & 2 | 704 | 698 | 350 | 348 |
| 47 | 2 | 144 | 8 | 2 & 2 | 704 | 696 | 350 | 346 |
| 48 | 2 | 144 | 16 | 2 & 2 | 704 | 692 | 348 | 344 |
| 49 | 2 | 144 | 32 | 2 & 2 | 704 | 684 | 344 | 340 |
| 50 | 2 | 144 | 0 | 16 & 16 | 704 | 672 | 352 | 320 |

| <u>Slot Format #</u> | <u>Spreading Factor</u> | <u>Midamble length (chips)</u> | <u>N_{TCI} (bits)</u> | <u>N_{SS} & N_{TPC} (bits)</u> | <u>Bits/slot</u> | <u>N_{Data/Slot} (bits)</u> | <u>N_{data/data field(1)} (bits)</u> | <u>N_{data/data field(2)} (bits)</u> |
|----------------------|-------------------------|--------------------------------|-------------------------------|--|----------------------|-------------------------------------|--|--|
| 51 | 2 | 144 | 4 | 16 & 16 | 704 | 670 | 350 | 320 |
| 52 | 2 | 144 | 8 | 16 & 16 | 704 | 668 | 350 | 318 |
| 53 | 2 | 144 | 16 | 16 & 16 | 704 | 664 | 348 | 316 |
| 54 | 2 | 144 | 32 | 16 & 16 | 704 | 656 | 344 | 312 |
| 55 | 1 | 144 | 0 | 0 & 0 | 1408 | 1408 | 704 | 704 |
| 56 | 1 | 144 | 4 | 0 & 0 | 1408 | 1406 | 702 | 704 |
| 57 | 1 | 144 | 8 | 0 & 0 | 1408 | 1404 | 702 | 702 |
| 58 | 1 | 144 | 16 | 0 & 0 | 1408 | 1400 | 700 | 700 |
| 59 | 1 | 144 | 32 | 0 & 0 | 1408 | 1392 | 696 | 696 |
| 60 | 1 | 144 | 0 | 2 & 2 | 1408 | 1404 | 704 | 700 |
| 61 | 1 | 144 | 4 | 2 & 2 | 1408 | 1402 | 702 | 700 |
| 62 | 1 | 144 | 8 | 2 & 2 | 1408 | 1400 | 702 | 698 |
| 63 | 1 | 144 | 16 | 2 & 2 | 1408 | 1396 | 700 | 696 |
| 64 | 1 | 144 | 32 | 2 & 2 | 1408 | 1388 | 696 | 692 |
| 65 | 1 | 144 | 0 | 32 & 32 | 1408 | 1344 | 704 | 640 |
| 66 | 1 | 144 | 4 | 32 & 32 | 1408 | 1342 | 702 | 640 |

| Slot Format # | Spreading Factor | Midamble length (chips) | N_{TFCI} (bits) | N_{SS} & N_{TPC} (bits) | Bits/slot | $N_{Data/Slot}$ (bits) | $N_{data/data\ field(1)}$ (bits) | $N_{data/data\ field(2)}$ (bits) |
|---------------|------------------|-------------------------|-------------------|-----------------------------|-----------|------------------------|----------------------------------|----------------------------------|
| 7 | 1 | 144 | 12 | 3 & 3 | 2112 | 2100 | 1053 | 1047 |
| 8 | 1 | 144 | 24 | 3 & 3 | 2112 | 2094 | 1050 | 1044 |
| 9 | 1 | 144 | 48 | 3 & 3 | 2112 | 2082 | 1044 | 1038 |
| 10 | 1 | 144 | 0 | 48 & 48 | 2112 | 2016 | 1056 | 960 |
| 11 | 1 | 144 | 6 | 48 & 48 | 2112 | 2013 | 1053 | 960 |
| 12 | 1 | 144 | 12 | 48 & 48 | 2112 | 2010 | 1053 | 957 |
| 13 | 1 | 144 | 24 | 48 & 48 | 2112 | 2004 | 1050 | 954 |
| 14 | 1 | 144 | 48 | 48 & 48 | 2112 | 1992 | 1044 | 948 |
| 15 | 16 | 144 | 0 | 0 & 0 | 132 | 132 | 66 | 66 |
| 16 | 16 | 144 | 6 | 0 & 0 | 132 | 129 | 63 | 66 |
| 17 | 16 | 144 | 12 | 0 & 0 | 132 | 126 | 63 | 63 |
| 18 | 16 | 144 | 24 | 0 & 0 | 132 | 120 | 60 | 60 |
| 19 | 16 | 144 | 48 | 0 & 0 | 132 | 108 | 54 | 54 |
| 20 | 16 | 144 | 0 | 3 & 3 | 132 | 126 | 66 | 60 |
| 21 | 16 | 144 | 6 | 3 & 3 | 132 | 123 | 63 | 60 |
| 22 | 16 | 144 | 12 | 3 & 3 | 132 | 120 | 63 | 57 |

| Slot Format # | Spreading Factor | Midamble length (chips) | N_{TFCI} (bits) | N_{SS} & N_{TPC} (bits) | Bits/slot | $N_{Data/Slot}$ (bits) | $N_{data/data\ field(1)}$ (bits) | $N_{data/data\ field(2)}$ (bits) |
|---------------|------------------|-------------------------|-------------------|-----------------------------|-----------|------------------------|----------------------------------|----------------------------------|
| 23 | 16 | 144 | 24 | 3 & 3 | 132 | 114 | 60 | 54 |
| 24 | 16 | 144 | 48 | 3 & 3 | 132 | 102 | 54 | 48 |

| Slot Format # | Spreading Factor | Midamble length (chips) | N_{TFCI} (bits) | N_{SS} & N_{TPC} (bits) | Bits/slot | $N_{Data/Slot}$ (bits) | $N_{data/data\ field(1)}$ (bits) | $N_{data/data\ field(2)}$ (bits) |
|---------------|------------------|-------------------------|-------------------|-----------------------------|-----------|------------------------|----------------------------------|----------------------------------|
| 0 | 4 | 144 | 0 | 0 & 0 | 2112 | 2112 | 1056 | 1056 |
| 1 | 4 | 144 | 6 | 0 & 0 | 2112 | 2106 | 1053 | 1053 |
| 2 | 4 | 144 | 12 | 0 & 0 | 2112 | 2100 | 1050 | 1050 |
| 3 | 4 | 144 | 24 | 0 & 0 | 2112 | 2088 | 1044 | 1044 |
| 4 | 4 | 144 | 48 | 0 & 0 | 2112 | 2064 | 1032 | 1032 |
| 5 | 4 | 144 | 0 | 3 & 3 | 2112 | 2106 | 1056 | 1050 |
| 6 | 4 | 144 | 6 | 3 & 3 | 2112 | 2100 | 1053 | 1047 |
| 7 | 4 | 144 | 12 | 3 & 3 | 2112 | 2094 | 1050 | 1044 |
| 8 | 4 | 144 | 24 | 3 & 3 | 2112 | 2082 | 1044 | 1038 |
| 9 | 4 | 144 | 48 | 3 & 3 | 2112 | 2058 | 1032 | 1026 |
| 10 | 4 | 144 | 0 | 48 & 48 | 2112 | 2016 | 1056 | 960 |

| Slot Format # | Spreading Factor | Midamble length (chips) | N_{TECL} (bits) | N_{SS} & N_{TPC} (bits) | Bits/slot | $N_{Data/Slot}$ (bits) | $N_{data/data\ field(1)}$ (bits) | $N_{data/data\ field(2)}$ (bits) |
|---------------|------------------|-------------------------|-------------------|-----------------------------|-----------|------------------------|----------------------------------|----------------------------------|
| 11 | 1 | 144 | 6 | 48 & 48 | 2112 | 2010 | 1053 | 957 |
| 12 | 1 | 144 | 12 | 48 & 48 | 2112 | 2004 | 1050 | 954 |
| 13 | 1 | 144 | 24 | 48 & 48 | 2112 | 1992 | 1044 | 948 |
| 14 | 1 | 144 | 48 | 48 & 48 | 2112 | 1968 | 1032 | 936 |
| 15 | 16 | 144 | 0 | 0 & 0 | 132 | 132 | 66 | 66 |
| 16 | 16 | 144 | 6 | 0 & 0 | 132 | 126 | 63 | 63 |
| 17 | 16 | 144 | 12 | 0 & 0 | 132 | 120 | 60 | 60 |
| 18 | 16 | 144 | 24 | 0 & 0 | 132 | 108 | 54 | 54 |
| 19 | 16 | 144 | 48 | 0 & 0 | 132 | 84 | 42 | 42 |
| 20 | 16 | 144 | 0 | 3 & 3 | 132 | 126 | 66 | 60 |
| 21 | 16 | 144 | 6 | 3 & 3 | 132 | 120 | 63 | 57 |
| 22 | 16 | 144 | 12 | 3 & 3 | 132 | 114 | 60 | 54 |
| 23 | 16 | 144 | 24 | 3 & 3 | 132 | 102 | 54 | 48 |
| 24 | 16 | 144 | 48 | 3 & 3 | 132 | 78 | 42 | 36 |

[Explanation difference:]

Based on the burst structure and the TFCI,SS and TPC control signals, the low chip rate TDD option has a different burst type from that of high chip rate TDD option.
~~When 2M service is transmitted, the timeslot formats are based on 8PSK modulation, but the timeslot formats in table 3 are not restricted to the use for 2Mbps only.~~

7.2.2.2.3 Transmission of SS

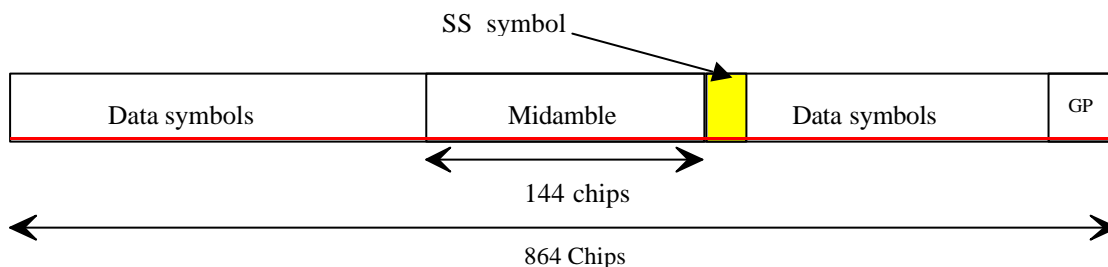
[Description:]

The SS is utilized to command a timing adjustment each M frame. The SS, as one of L1 signals, is to be transmitted once per 5ms subframe in downlink.

[Rationale:]

~~The SS is utilized to command a timing adjustment $(k/8)T_c$ each M frames, where T_c is the chip period. The default k and M values are signaled by the network by means of system information that is broadcast in the cell. The SS information is to be transmitted directly after the midamble in downlink. Figure 1 shows the position of the SS in a burst. The SS, as one of L1 signals, is to be transmitted once per 5ms subframe.~~

~~M (1-8) and k (1-8) can be adjusted during call setup or readjusted during the call.~~



Position of SS information in a burst in downlink and uplink

Note that for the uplink where there's no SS symbol used, the SS symbol space is reserved for future use. This can keep the UL and DL slot same structure.

For the number of layer 1 symbols there are 3 possibilities configurable for each channelisation code during the call setup:

- ? one SS and TPC symbol
- ? no SS and TPC symbols
- ?? 16/SF SS and 16/SF TPC symbols

The burst type for dedicated channels provides the possibility for transmission of uplink synchronisation control (ULSC).

The transmission of ULSC is done in the data parts of the traffic burst. Hence the midamble structure and length is not changed. The ULSC information is to be transmitted directly after the midamble. Figure XX shows the position of the SS command in a traffic burst.

For every user the ULSC information shall be transmitted at least once per transmitted sub-frame. By default the following rules apply:

1. If TFCI is applied for a CCTrCH, the SS command(s) shall be transmitted using the same channelisation code and the same timeslots as the TFCI.
2. If no TFCI is applied for a CCTrCH, the SS command(s) shall be transmitted using the first allocated channelisation code and the first allocated timeslot, according to the order in the higher layer allocation message.

Apart from the default rules other allocations of SS commands are possible according higher layer signalling – e.g. the transmission of more than one SS command (on more than one time slot).

The SS command is spread with the same spreading factor (SF) and spreading code as the data parts of the respective physical channel.

The SS is utilised to command a timing adjustment by $(k/8) T_c$ each M sub-frames, where T_c is the chip period. The default k and M values are signalled by the network by means of system information that is broadcast in the cell. The SS, as one of L1 signals, is to be transmitted once per 5ms sub-frame.

M (1-8) and k (1-8) can be adjusted during call setup or readjusted during the call.

Note: The smallest step for the SS signalled by the UTRAN is $1/8 T_c$. For the UE capabilities regarding the SS adjustment of the UE it is suggested to set the tolerance for the executed command to be $[1/9; 1/7] T_c$.

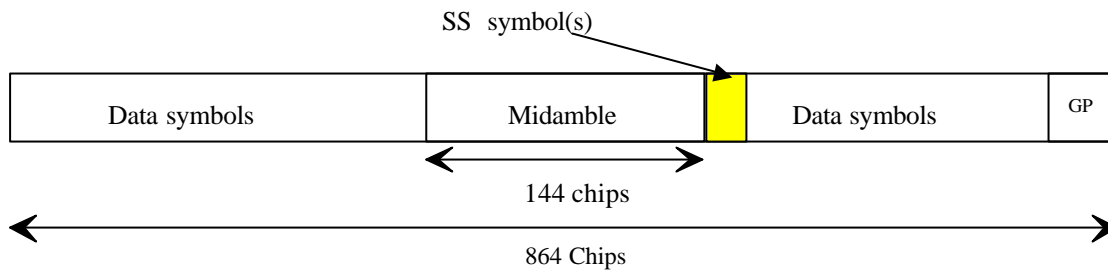


Figure XX Position of ULSC information in the traffic burst (downlink and uplink)

*Note that for the uplink where there's no SS symbol used, the SS symbol space is reserved for future use. This can keep UL and DL slots the same structure.

For the number of layer 1 symbols there are 3 possibilities configurable for each channelisation code during the call setup:

- ?? one SS symbol
- ?? no SS symbol
- ?? 16/SF SS symbols

So, in case 3, when SF=1, there are 16 SS symbols which correspond to 32 bits (for QPSK) and 48 bits (for 8PSK).

Each of the SS symbols in the DL will be associated with an UL time slot depending on the allocated UL time slots and the allocated SS symbols in the DL.

Note: Even though the different time slots of the UE are controlled with independent SS commands, the UE is not in need to execute SS commands leading to a deviation of more than [3] chip with respect to the average timing advance applied by the UE.

The synchronisation shift commands for each UL time slot (all channelisation codes on that time slot have the same SS command) will be distributed to the following rules:

1. The UL time slots the SS commands are intended for will be numbered from the first to the last UL time slot occupied by the regarded UE (starting with 0) considering all CCTrCHs allocated to that UE.
2. The commanding SS symbols on all downlink CCTrCHs allocated to one UE are numbered consecutively starting with zero according to the following rules:
 - a) The numbers of the SS commands of a regarded DL time slot are lower than those of DL time slots being transmitted after that time slot
 - b) Within a DL time slot the numbers of the SS commands of a regarded channelisation code are lower than those of channelisation codes having a bigger spreading code number

The spreading code number is defined by the following table: (see TS 25.223)

| <u>Spreading code number</u> | <u>SF (Q)</u> | <u>Walsh code number (k)</u> |
|------------------------------|---|---------------------------------------|
| <u>0</u> | <u>16</u> | <u>$c_{Q?16}^{(k?1)}$</u> |
| | <u>...</u> | |
| <u>15</u> | <u>16</u> | <u>$c_{Q?16}^{(k?16)}$</u> |
| | <u>Spreading factors 2-8 are not used in DL</u> | |
| <u>30</u> | <u>1</u> | <u>$c_{Q?1}^{(k?1)}$</u> |

c) Within a channelisation code numbers of the SS commands are lower than those of SS commands being transmitted after that time

The following equation is used to determine the UL time slot which is controlled by the regarded SS symbol:

$$UL_{pos} = (SFN' \cdot N_{SSsymbols} + SS_{pos}) \bmod (N_{ULslot})$$

where

UL_{pos} is the number of the controlled uplink time slot.

SFN' is the system frame number counting the sub-frames. The system frame number of the radio frames (SFN) can be derived from SFN' by

SFN = SFN' div 2, where div is the remainder free division operation.

N_{SSsymbols} is the number of SS symbols in a frame.

SS_{pos} is the number of the regarded SS symbol within the sub-frame.

N_{ULslot} is the number of UL slots in a frame.

[Explanation difference:]

In high chip rate TDD option, SS information is not transmitted as L1 signal on each frame. Because of uplink synchronization in the low chip rate TDD option, SS information is transmitted in downlink, as one of L1 signals, once per 5ms subframe.

7.2.2.3 Training sequences for spread bursts

[Description:]

The training sequences, i.e. midambles, of different users active in the same time slot are time shifted versions of a single periodic basic code. Different cells use different periodic basic midamble codes, i.e. different midamble sets. In this way joint channel estimation for the channel impulse responses of all active users within one time slot can be done by one single cyclic correlation. The different user specific channel impulse response estimations are obtained sequentially in time at the output of the correlator.

Up to 16 midambles are possible within the low chip rate TDD option.

The generation of midamble is different from high chip rate TDD option. The difference of training sequences for spread bursts for low chip rate is described here.

[Rationale:]

The burst structure for low chip rate TDD option is different with high chip rate TDD option. These bursts contain L_m midamble chips, which are also termed midamble elements. The L_m elements $\underline{m}_i^{(k)}$; $i=1 \dots L_m$; $k=1, \dots, K$; of the midamble codes $\underline{\mathbf{m}}^{(k)}$; $k=1, \dots, K$; of the K users are taken from the complex set

$$\underline{V}_m = \{1, j, -1, -j\} \quad (14)$$

The elements $\underline{m}_i^{(k)}$ of the complex midamble codes $\underline{\mathbf{m}}^{(k)}$ fulfil the relation

$$\underline{m}_i^{(k)} = (j)^i \underline{m}_i^{(k)} \quad \underline{m}_i^{(k)} = \{1, j\}; i = 1, \dots, L_m; k = 1, \dots, K. \quad (22)$$

Hence, the elements $\underline{m}_i^{(k)}$ of the complex midamble codes $\underline{\mathbf{m}}^{(k)}$ of the K users are alternating real and imaginary.

With W being the number of taps of the impulse response of the UE radio channels, the L_m binary elements $m_i^{(k)}$; $i = 1, \dots, L_m$; $k = 1, \dots, K$; of (2) for the complex midamble $\underline{\mathbf{m}}^{(k)}$; $k=1, \dots, K$; of the K users are generated according to Steiner's method [1] from a single periodic basic code

$$\underline{\mathbf{m}} = \{m_1, m_2, \dots, m_{L_m \cdot (K-1)W}\}^T \quad m_i = \{1, j\}; i = 1, \dots, (L_m \cdot (K-1)W). \quad (33)$$

The elements m_i ; $i = 1, \dots, (L_m \cdot (K-1)W)$, of (3) fulfil the relation

$$m_i = m_{i+P} \quad \text{for the subset } i = (P-1), \dots, (L_m \cdot (K-1)W). \quad (44)$$

The P elements m_i ; $i = 1, \dots, P$, of one period of m according to (3) are contained in the vector

$$\underline{\mathbf{m}}_P = \{m_1, m_2, \dots, m_P\}^T. \quad (55)$$

With $\underline{\mathbf{m}}$ according to (3) the L_m binary elements $m_i^{(k)}$; $i = 1, \dots, L_m$; $k = 1, \dots, K$; of (2) for the midamble of the K users are generated based on Steiner's formula

$$m_i^{(k)} = m_{i+(K-1)W} \quad i = 1, \dots, L_m; k = 1, \dots, K. \quad (66)$$

In the following the term 'a midamble code set' or 'a midamble code family' denotes K specific midamble codes $\underline{\mathbf{m}}^{(k)}$; $k=1, \dots, K$. Different midamble code sets $\underline{\mathbf{m}}^{(k)}$; $k=1, \dots, K$; are in the following specified based on different periods $\underline{\mathbf{m}}_P$ according to (5).

In adjacent cells of the cellular UE radio system, different midamble codes sets $\underline{\mathbf{m}}^{(k)}$; $k=1, \dots, K$; should be used to guarantee a proper channel estimation.

As mentioned above a single midamble code set $\underline{\mathbf{m}}^{(k)}$; $k=1, \dots, K$; consisting of K midamble codes is based on a single period $\underline{\mathbf{m}}_P$ according to (5).

In the following several exemplary periods \mathbf{m}_P according (5) which can be used to generate different midamble code sets $\mathbf{m}^{(k)}$; $k=1, \dots, K$; will be listed in tables in a hexadecimal representation. As shown in the table below always 4 binary elements m_i are mapped on a single hexadecimal digit.

Table : Mapping of 4 binary elements on a single hexadecimal digit

| 4 binary elements m_i | Mapped on hexadecimal digit |
|-------------------------|-----------------------------|
| -1 -1 -1 -1 | 0 |
| -1 -1 -1 1 | 1 |
| -1 -1 1 -1 | 2 |
| -1 -1 1 1 | 3 |
| -1 1 -1 -1 | 4 |
| -1 1 -1 1 | 5 |
| -1 1 1 -1 | 6 |
| -1 1 1 1 | 7 |
| 1 -1 -1 -1 | 8 |
| 1 -1 -1 1 | 9 |
| 1 -1 1 -1 | A |
| 1 -1 1 1 | B |
| 1 1 -1 -1 | C |
| 1 1 -1 1 | D |
| 1 1 1 -1 | E |
| 1 1 1 1 | F |

The mean degradation's which serve as a quality information of the periods \mathbf{m}_P according to (5) and hence of the specified midamble code sets $\mathbf{m}^{(k)}$; $k=1, \dots, K$; will be also given.

Table: Basic Midamble Codes

| Code ID | Basic Midamble Codes of length 128 |
|---------|------------------------------------|
| 0 | B2AC420F7C8DEBFA69505981BCD028C3 |
| 1 | 0C2E988E0DBA046643F57B0EA6A435E2 |
| 2 | D5CEC680C36A4454135F86DD37043962 |
| 3 | E150D08CAC2A00FF9B32592A631CF85B |
| 4 | E0A9C3A8F6E40329B2F2943246003D44 |
| 5 | FE22658100A3A683EA759018739BD690 |
| 6 | B46062F89BB2A1139D76A1EF32450DA0 |

| | |
|----|----------------------------------|
| 7 | EE63D75CC099092579400D956A90C3E0 |
| 8 | D9C0E040756D427A2611DAA35E6CD614 |
| 9 | EB56D03A498EC4FEC98AE220BC390450 |
| 10 | F598703DB0838112ED0BABB98642B665 |
| 11 | A0BC26A992D4558B9918986C14861EFF |
| 12 | 541350D109F1DD68099796637B824F88 |
| 13 | 892D344A962314662F01F9455F7BC302 |
| 14 | 49F270E29CCD742A40480DD4215E1632 |
| 15 | 6A5C0410C6C39AA04E77423C355926DE |
| 16 | 7976615538203103D4DBCC219B16A9E1 |
| 17 | A6C3C3175845400BD2B738C43EE2645F |
| 18 | A0FD56258D228642C6F641851C3751ED |
| 19 | EFA48C3FC84AC625783C6C9510A2269A |
| 20 | 62A8EB1A420334B23396E8D76BC19740 |
| 21 | 9E96235699D5D41C9816C921023BC741 |
| 22 | 4362AE4CAE0DCC32D60A3FED1341A848 |
| 23 | 454C068E6C4F190942E0904B95D61DFB |
| 24 | 607FEEA6E2E99206718A49C0D6A25034 |
| 25 | E1D1BCDA39A09095B5C81645103A077C |
| 26 | 994B445E558344DE211C8286DDD3D1A3 |
| 27 | C15233273581417638906ADB61FDCA3C |
| 28 | 8B79A274D542F096FB1388098230F8A1 |
| 29 | DF58AC1C5F44B2A40266385CF1DA5640 |
| 30 | B5949A1CC69962C464401D05FF5C1A7A |
| 31 | 85AC489841ED3EAA2D83BBB0039CC707 |
| 32 | AE371CC144BC95923CA8108D8B49FE82 |
| 33 | 7F188484A649D1C22BDA1F09D49B5117 |
| 34 | ADAA3C657089DEF7C0284903A491C9B0 |
| 35 | C3F96893C7504DC3B51488604AF64F4C |
| 36 | B4002F5AE0CE8623AC979D368E9148C1 |
| 37 | 0EEBCC0C795C02A106C24ABB36D08C6E |
| 38 | 4B0F537E384A893F58971580D9894433 |

| | |
|----|-----------------------------------|
| 39 | 08E0035AB29B7ECC53C15DAA0687CC8F |
| 40 | 8611ACBC4C82781D77654EE862506D60 |
| 41 | 63315261A8F1CB02549802DBFD197C07 |
| 42 | 9A2609A434F43E7DCADC0E22B2EF4012 |
| 43 | F4C9F0A127A88461209ABF8C69CE4D00 |
| 44 | C79124EE3FFC28C5C4524D2B01670D42 |
| 45 | C91985C4FED53D09361914354BA80E79 |
| 46 | 82AA517260779ECFF26212C1A10BDC29 |
| 47 | 561DE2040ACB458E0DBD354E43E111D9 |
| 48 | 2E58C7202D17392BC1235782CEFAAB09 |
| 49 | C4FAA121C698047650F6503126A577C1 |
| 50 | E7B75206A9B410E44346E0DAE842A23C |
| 51 | 3F8B1C32682B28D098D3805ED130EA7F |
| 52 | 8D5FC2C1C6715F824B401434C8D4BB82 |
| 53 | 0B2A43453ACC028FE6EB6E1CB0740B59 |
| 54 | BC56948FC700BA4883262EE73E12D82A |
| 55 | 558D136710272912FA4F183D1189A7FD |
| 56 | 5709E7F82DC6500B7B12A3072D182645 |
| 57 | 86D4F161C844AE5E20EE39FD5493B044 |
| 58 | 8729B6EDC382B152185885F013DAE222 |
| 59 | 154C45B50720F4C362C14C77FE8335A1 |
| 60 | C6A0962890351F4EB802DE43A7662C9E |
| 61 | D19D69D6B380B4B22457CB80033519F0 |
| 62 | C7D89509FB0DAE9255998E0A00C2B262 |
| 63 | DFD481C652C0C905D61D66F1732C4AA2 |
| 64 | 06C848619AF1D6C910A8EAC4B622FC06 |
| 65 | 0635E29D4E7AC8ABC189890241F45ECA |
| 66 | B272B020586AAD7B093AC2F459076638 |
| 67 | B608ACE46E1A6BC96181FEEDD88B54140 |
| 68 | 0A516092B3ED7849B168AFE223B8670E |
| 69 | D1A658C5009E04D0D7D5E9205EE663E8 |
| 70 | AC316DC39B91EB60B1AABD8280740432 |

| | |
|-----|----------------------------------|
| 71 | E3F06825476A026CD287625E514519FC |
| 72 | A56D092080DDE8994F387C175CC56833 |
| 73 | 15EA799DE587C506D0CD99A408217B05 |
| 74 | A59C020BAB9AF6D3F813C391CA244CD2 |
| 75 | 74B0101EB9F3167434B94BABC8378882 |
| 76 | CE752975C8DA9B0100386DB82A8C3D20 |
| 77 | BBB38DCDB1E9118570AC147DC05241A4 |
| 78 | 944ABBF0866098101F6971731AB2E986 |
| 79 | 2BB147B2A30C68B4853F90481A166EB6 |
| 80 | 444840ACCF3F23C45B56D7704BF18283 |
| 81 | 87604F7450D1AD188C452981A5C7FC9B |
| 82 | 8C3842EBC948A65BC4C8B387F11B7090 |
| 83 | 10B4767D071CF5DB2288E4029576135A |
| 84 | 6F07AAB697CD0089572C6B062E2018E4 |
| 85 | D3D65B442057E613A8655060C8D29E27 |
| 86 | 5EDA330514C604BF4E0894E09EC57A74 |
| 87 | B0899CD094060724DED82AE85F18A43A |
| 88 | B2D999B86DF902BC25015CAE3A0823C4 |
| 89 | C23CD40F04242B92D46EED82CD9A9A18 |
| 90 | D22DDCC5CB82960125DD24655F3C8788 |
| 91 | 54987218FBD99AE4340FD4C9458E9850 |
| 92 | BE4341822997A7B11EA1E8A1A2767005 |
| 93 | 255200FBA6EE48E6DE0A82B0461B8D0F |
| 94 | 6FBD58A663932423503690CF9C171701 |
| 95 | D215033A4AA87EC1C232BAC7EDA09370 |
| 96 | CA0959B01AE48E80204F1E4A3F29CE55 |
| 97 | 582043413B9B825903E3A3545ED59463 |
| 98 | 5016541922971C703D16E284CBDF633B |
| 99 | 7347EF160A1733CA98D43608A83A920B |
| 100 | 908B22AD433CCA00B3FD47C691F1A290 |
| 101 | BB22A272FC6923DF1B43BA4118806570 |
| 102 | 0FA75C87474836B47DC7624D61193802 |

| | |
|-----|----------------------------------|
| 103 | A22EBA0658A4D0FF1E9CA5030A65CC06 |
| 104 | 6C9C51CA15F1F4981F4C46180A6A6697 |
| 105 | 4C847ACF8BC15359C405322851C9BDE2 |
| 106 | C1D29499C0082C9DE473ED15B14D63E0 |
| 107 | 7E85ECC98AC761005076C5572869A431 |
| 108 | D8F11121595B8F49F78A7039E44126A0 |
| 109 | 1A0BC814445FD71C8E5B1A9163ED2059 |
| 110 | A7591F27F8B0C00C68CC41697954FA04 |
| 111 | 6CA2CE595E7406D79C4840183D41B9D0 |
| 112 | C093D3CC701FC20E66F5AB22516C5460 |
| 113 | D0E0CDE9B595546B96C4F8066B469020 |
| 114 | E99F743A451431C8B427054A4E6F2007 |
| 115 | C0D21A344A2C07DF2A6E6E6250C7B91E |
| 116 | F031223E282CF7A4D8EF174A908668AE |
| 117 | E4BD244AC16C55C7137FB068FD44280C |
| 118 | C44920DE2028F19FC2AAB36A0DCFDAD0 |
| 119 | 3FA7054E77135250699E6C8A11600742 |
| 120 | D5740B4D8870C1C5B5A214C4266FC537 |
| 121 | F0B7942D43BB6F38446442EB8126AB80 |
| 122 | 83DB9534EAD6238FA8968798CDF04848 |
| 123 | EB9663CDDC2B291690703125BABC800 |
| 124 | 84D547225D4BBD20DEF1A583240C6E0F |
| 125 | B51F6A771838BE934724AEA6A2669802 |
| 126 | D92AC05E10496794BBDC115233B1C068 |
| 127 | D3ACF0078EDA9856BBB0AF8651132103 |

[Explanation difference:]

The midamble used in the burst for low chip rate TDD is different from high chip rate TDD. And this is mainly coming from different chip rate and burst format. Different chip rate lead to different length of channel impulse response and the different length of training sequence (midamble).

The maximum channel impulse response is scalable. This evokes a different midamble generation scheme as used for high chip rate TDD.

7.2.2.3.1 Selection of length of channel impulse response

[Description:]

The training sequences, i.e. Midambles, of different users active in the same slot are time shifted versions of one single periodic basic code. Different cells use different periodic basic codes, i.e. different midamble sets. In this way a joint channel estimation for the channel impulse responses of all active users within one time slot can be done by one single cyclic correlation. The different user specific channel impulse response estimates are obtained sequentially in time at the output of the correlator. Up to 16 midambles in one time slot are possible within the low chip rate TDD option.

In both low and high chip rate systems, W , the length of the impulse response of the mobile radio channels, is an important parameter. There is only one burst type for ~~normal~~ traffic time slot in the low chip rate TDD option, and the length of midambles is different from the high chip rate option, so the selection of W needs to be defined separately.

[Rational:]

The midamble has a length of $L_m=144$, which is corresponding to:

$$K=2, 4, 6, 8, 10, 12, 14, 16, W = \frac{?P?}{?K?}, P=128.$$

Note: that $?x?$ denotes the largest integer number less or equal to x .

Depending on the possible delay spread cells are configured to use midambles which are generated from the Basic Midamble Codes.

The cell configuration is broadcast on BCH.

7.2.2.4 Beamforming and Transmit Diversity

[Description:]

A smart antenna system is composed of an array of multiple antenna elements and coherent transceivers with advanced digital signal processing algorithms. Instead of a single fixed beam pattern from a traditional antenna, the smart antenna can dynamically generate multiple beam patterns, each of them is pointed to a particular UE, and such beam patterns can adapt to follow any UE intelligently. On the Rx side of Node B, such a feature, i.e., spatial selective reception at the Node B can greatly minimize co-channel interference from the co-channel UEs at different locations, thus increase the Rx sensitivity and lead to higher capacity. It can also effectively incorporate multipath components to combat multipath fading. On the Tx side of Node B, intelligent spatially selective Tx (downlink) beamforming can also greatly reduce the interference to other co-channel UEs, then dramatically save the output power requirement and lead to higher capacity. It should be noted that this section only describes a preferred approach to beamforming, other high performance techniques may also be applicable.

The low chip rate option is mainly based on the smart antenna technology. Some main technical features of the low chip rate TDD option such as 5 ms sub-frame structure are based on the smart antenna request.

When DL beamforming or TX Diversity is used, at least for the resource units beamforming/Tx Diversity is applied to and which are allocated to dedicated channels, the resource units shall get one individual midamble per user or per resource unit according to midamble generation, even in DL.

[Rationale:]

The smart antenna array is composed of N antenna elements, N related feed cables and N coherent RF transceivers in RF part. By use of the A/D converters or D/A converters in analog baseband (ABB), the Rx and Tx analog signals are interfaced to the digital baseband (DBB) part over the high-speed data bus. In this model, all antenna elements related feed cables and coherent RF transceivers will be calibrated before operating.

Beamforming

For the Node B is equipped with smart antenna array and DBB DSP, when a signal comes from one UE within the coverage of the Node B, each antenna element and coherent RF receiver will get it. Because of the different location of the different antenna element, the phase of the Rx signal will be different. In case of multipath propagation, each path will come from different directions with different amplitude and delay. Then the Rx signal at each antenna element will show different phase and amplitude. After the front-end processing in RF part and A/D converters processing in ABB, digitized Rx signal with the phase and amplitude information will be sent to DSP in DBB part. After despreading in the DBB processor, the Rx data of each code channel may be obtained.

The purpose of smart antenna in uplink is to find the best E_b/I_0 after the combination. Theoretically, spatial reception at Node B can add up all useful signals while canceling all multipath interference. The next step is to realise downlink beamforming. The Tx signal of the each code channel is got by some algorithms that enable the UE to obtain the best E_b/I_0 . In TDD system, because of the symmetrical performance in wave propagation, it is possible to directly use the spatial reception at Node B results to downlink beamforming.

Fast beamforming

It is always very important to reach fast beamforming to catch the time variation in mobile network. The Node B should have a in-time reaction to the fast changing beam patterns. And this is the reason that the TDD interval in low chip rate option is 5ms while 10ms in high chip rate option. This value is a compromise in considering both the number of time slots and the switching speed of RF components.

In smart antenna system, the BTS need receive the UpLink data first, then decide the UE's position, and then beamform to UE in Downlink, but the UE does not need to transmit regularly for the Node B to determine the antenna weights when it is in idle mode.

[Explanation difference:]

For high chip rate option, the chapter about beamforming already exists.

Like the high chip rate option is that not only each user can get one midamble but also each resource allocated to that user can (but need not to) get an individual midamble. The benefit of this is that the signalling overhead is reduced.

7.2.3 Primary common control physical channel (P-CCPCH)

7.2.3.1 Primary common control physical channel (P-CCPCH)

The BCH as described in subclause 'Common Transport Channels' is mapped onto the Primary Common Control Physical Channels (P-CCPCH1 and P-CCPCH2). The position (time slot / code) of the P-CCPCHs is fixed in the 1.28Mcps TDD. The P-CCPCHs are mapped onto the first two code channels of timeslot#0 with spreading factor of 16. see subclause 'Common Transport Channels'. The P-CCPCH is always transmitted with an antenna pattern configuration that provides whole cell coverage.

~~The BCH as described in subclause 7.3.2 'Common Transport Channels' is mapped onto the Primary Common Control Physical Channels (P-CCPCH1 and P-CCPCH2). The position (time slot / code) of the P-CCPCHs is fixed in low chip rate TDD option, see subclause 7.3.2 'Common Transport Channels'. An encoded bit identifies whether the interleaving frame in the P-CCPCH contains a BCH (1) or not (0).~~

7.2.3.1.1 P-CCPCH Spreading

The P-CCPCH uses fixed spreading with a spreading factor SF = 16. The P-CCPCH1 and P-CCPCH2 always use channelisation code $C_{Q^{16}}^{(k?1)}$ and $C_{Q^{16}}^{(k?2)}$ respectively. ~~0 and 1 respectively.~~

7.2.3.1.2 P-CCPCH Burst Types

Only one burst type in low chip rate option. No TFCI is applied for the P-CCPCH.

7.2.3.1.3 P-CCPCH Training sequences

The training sequences, i.e. midambles, as described in the subclause on midamble generation are used for the P-CCPCH. The basic midamble code $m^{(1)}$ is used for P-CCPCHs as training sequence.

~~The training sequences, i.e. midambles, as described in the MA-generation chapter are used for the P-CCPCHs. The basic midamble code $m^{(1)}$ is used for P-CCPCHs as training sequence.~~

~~As mentioned in sub-clause of P-CCPCH in 25.928, P-CCPCHs are mapped onto first two code channels of Ts0 with spreading factor of 16. Other code channel in Ts0 should also use spreading factor of 16.~~

~~Each transport channel assigned in TS0 has channel impulse response estimation window of maximum length $W=16$ such that there are 8 midamble codes used for TS0.~~

~~Ts0 is configured in the following way: Each of the 8 midamble codes is assigned to 2 code channels of spreading factor 16. The first midamble code is assigned to the first 2 code channels of spreading factor 16. The next midamble code to the next 2 code channels of spreading factor 16 and so forth. The P-CCPCHs are assigned to the first midamble code. In order to provide flexibility, it is possible that the Node B uses for channels other than P-CCPCHs a certain midamble code assigned to only 1 code channel of spreading factor 16. In that case, the second code that is assigned to the same midambles is not used by another UE.~~

[Explanation difference:]

~~In high chip rate option, the P-CCPCH always contains only the BCH. The position (time slot / code) of the P-CCPCH is known from the Synchronisation Channel (SCH).~~

~~In low chip rate option, the P-CCPCH can also contain the PCH and FACH as well as the BCH. The P-CCPCHs are mapped onto two code channels of the DL time slot (time slot 0) which is followed by the DwPTS~~

~~Other methods for BCH indication and their compatibility with models in TSG RAN-WG2 are to be considered.~~

There are two kinds of burst types in high chip option and the burst type 1 is used for the P-CCPCH.

There is only one burst type in the low chip rate option. In order to to make the same capacity available, 2 codes with SF16 are used for the P-CCPCH. The coding of the BCH is 1/3, because the usage of 2 codes allows more efficient coding.

~~If both the uplink and downlink physical channels are work under the synchronization mode and if "smart antenna" method is used, the interference on P-CCPCH is thought to be very little in low chip rate TDD option. As a result, "Tx diversity" has not been considered currently to be applied in low chip rate TDD. As this may not hold in all cases, the Block STTD applied for P-CCPCH is to be studied.~~

7.2.3.2 Secondary common control physical channel (S-CCPCH)

PCH and FACH are mapped onto one or more secondary common control physical channels (S-CCPCH). In this way the capacity of PCH and FACH can be adapted to the different requirements. The time slot and codes used for the S-CCPCH are broadcast on the BCH.

~~PCH and FACH can be mapped onto one or more secondary common control physical channels (S-CCPCH). In this way the capacity of PCH and FACH can be adapted to the different requirements. The time slot and codes~~

used for the S-CCPCH are broadcast via cell information. An encoded bit identifies that the interleaving frame in the S-CCPCH contains no BCH. This bit is always 0.

7.2.3.2.1 S-CCPCH Spreading

The S-CCPCH uses fixed spreading with a spreading factor SF = 16. The S-CCPCHs (S-CCPCH 1 and S-CCPCH 2) are always used in pairs, mapped onto two code channels with spreading factor 16. There can be more than one pair of S-CCPCHs in use in one cell. There are two S-CCPCHs (S-CCPCH 1 and S-CCPCH 2) mapped onto two codes of spreading factor 16. There can be also more than a single pair in use.

7.2.3.2.2 S-CCPCH Burst Types

Same burst type as for the P-CCPCH. TFCI may be applied for S-CCPCHs.

7.2.3.2.3 S-CCPCH Training sequences

The training sequences, i.e. midambles as described in the MA-generation chapter, are used for the S-CCPCH.

7.2.3.3 Fast Physical Access Channel (FPACH)

The Fast Physical Access CHannel (FPACH) is used by the Node B to carry, in a single burst, the acknowledgement of a detected signature with timing and power level adjustment indication to a user equipment. FPACH makes use of one resource unit only at spreading factor 16, so that its burst is composed by 44 symbols. The spreading code, training sequence and time slot position are configured by the network and signalled on the BCH.

7.2.3.3.1 FPACH burst

The FPACH burst contains 32 information bits.

Table X reports the content description of the FPACH information bits and their priority order.

Table X: FPACH information bits description

| <u>Information field</u> | <u>Length (in bits)</u> |
|--|-------------------------|
| <u>Signature Reference Number</u> | <u>3 (MSB)</u> |
| <u>Relative Sub-Frame Number</u> | <u>2</u> |
| <u>Received starting position of the UpPCH (UpPCH_{pos})</u> | <u>11</u> |
| <u>Transmit Power Level Command for RACH message</u> | <u>7</u> |
| <u>Reserved bits (default value: 0)</u> | <u>9 (LSB)</u> |

7.2.3.3.1.1 Signature Reference Number

The reported number corresponds to the numbering principle for the cell signatures as described in sub-clause 9.3. The Signature Reference Number value range is 0 – 7 coded in 3 bits such that:

bit sequence(0 0 0) corresponds to the first signature of the cell; ...; bit sequence (1 1 1) corresponds to the 8th signature of the cell.

7.2.3.3.1.2 Relative Sub-Frame Number

The Relative Sub-Frame Number value range is 0 – 3 coded such that:

bit sequence (0 0) indicates one sub-frame difference; ...; bit sequence (1 1) indicates 4 sub-frame difference.

7.2.3.3.1.3 Received starting position of the UpPCH (UpPCH_{pos})

The received starting position of the UpPCH value range is 0 – 2047 coded such that:

bit sequence (0 0 ... 0 0 0) indicates the received starting position zero chip; ...; bit sequence (1 1 ... 1 1 1) indicates the received starting position 2047*1/8 chip.

7.2.3.3.1.4 Transmit Power Level Command for the RACH message

The transmit power level command is transmitted in 7 bits.

7.2.3.3.2 Coding of the Forward Physical Access Channel (FPACH) information bits

The FPACH burst is composed by 32 information bits which are block coded and convolutional coded, and then delivered in one sub-frame as follows:

1. The 32 information bits are protected by 8 parity bits for error detection as described in sub-clause 4.2.1.1.
2. Convolutional code with constraint length 9 and coding rate 1/2 is applied as described in sub-clause 4.2.3.1. The size of data block c(k) after convolutional encoder is 96 bits.
3. To adjust the size of the data block c(k) to the size of the FPACH burst, 8 bits are punctured as described in sub-clause 4.2.7 with the following clarifications:

?? $N_{i,j}=96$ is the number of bits in a radio sub-frame before rate matching

?? $N_{i,j}=-8$ is the number of bits to punctured in a radio sub-frame

?? $e_{ini}=a \times N_{i,j}$

The 88 bits after rate matching are then delivered to the intra-frame interleaving.

4. The bits in input to the interleaving unit are denoted as {x(0), ..., x(87)}. The coded bits are block rectangular interleaved according to the following rule: the input is written row by row, the output is read column by column.

| | | | | | | |
|---|---------|---------|---------|---|---------|---|
| ? | $x(0)$ | $x(1)$ | $x(2)$ | □ | $x(7)$ | ? |
| ? | $x(8)$ | $x(9)$ | $x(10)$ | □ | $x(15)$ | ? |
| ? | □ | □ | □ | □ | □ | ? |
| ? | $x(80)$ | $x(81)$ | $x(82)$ | □ | $x(87)$ | ? |

Hence, the interleaved sequence is denoted by y (i) and are given by:

$y(0), y(1), \dots, y(87)=x(0), x(8), \dots, x(80), x(1), \dots, x(87).$

7.2.3.3.3 FPACH Spreading

The FPACH uses only spreading factor SF=16. The set of admissible spreading codes for use on the FPACH are broadcast on the BCH (within the FPACH configuration parameters on the BCH).

7.2.3.3.4 FPACH Burst Format

The burst format as described in section 7.2.2.2 is used for the FPACH.

7.2.3.3.5 FPACH Training sequences

The training sequences, i.e. midambles, of different users active in the same time slot are time shifted versions of a single periodic basic code. The basic midamble codes as described in the subclause about midamble generation are used for FPACH.

7.2.3.3.4 The physical random access channel (PRACH)

The RACH is mapped onto one or more uplink physical random access channels (PRACH). In such a way the capacity of the RACH can be flexibly scaled depending on the operators need.

7.2.3.3.4.1 PRACH Spreading

The uplink PRACH uses either spreading factor SF=16 or SF=8 or SF=4 as described in subclause 6.2.1. The set of admissible spreading codes for use on the PRACH and the associated spreading factors are broadcast on the BCH (within the RACH configuration parameters on the BCH).

~~The uplink PRACH uses either spreading factor SF=16 or SF=8 as described in subclause 7.3.2.3 'The Random Access Channel (RACH)'. The PRACH configuration (time slot number and assigned spreading codes) is broadcast through the BCH information.~~

7.2.3.3.4.2 PRACH Burst Types

The burst type used on the PRACH is the same as for a traffic channel.

7.2.3.3.4.3 PRACH Training sequences

The training sequences, i.e. midambles, of different users active in the same time slot are time shifted versions of a single periodic basic code. The basic midamble codes as described in subclause about midamble generation are used for PRACH.

~~The training sequences, i.e. midambles as described in the MA-generation chapter, are used for the PRACH.~~

7.2.3.3.4.4 Association between Training Sequences and Channelisation Codes

The association between training sequences and channelisation codes of PRACH in the 1.28McpsTDD is same as that of the DPCH.

~~In the low chip rate TDD option there is a different concept for the RACH. Resource units on the traffic time slots are used for the random access channels. For this reason the PRACH is described and allocated as e.g. the DPCH. Thus, there is no additional association between training sequences and channelisation codes like in the high chip rate TDD option.~~

[Explanation difference:]

In subclause 10.6.2 "random access procedure", it has been mentioned that the random access procedure of low chip rate option has two-step approach. The ~~SYNC~~SYNC-UL word is used to carry out uplink synchronisation and to resolve the access collision. This two-step procedure enables the PRACH to be transmitted with high synchronisation precision as DPCH. So in low chip rate TDD option, the PRACH is uplink synchronized with other uplink traffic, the burst type used on the PRACH is the same as for DPCH while in high chip rate TDD option the burst type of the PRACH is ~~a little~~ different from that of DPCH. The use of SF4 is necessary to support large RACH messages.

7.2.3.4.5 The synchronisation channel (SCH)

[Description:]

There are two dedicated physical synchronisation channels —DwPTS and UpPTS in each subframe of the low chip rate option as described in subclause 7.2.1 ‘Frame Structure’ and 7.2.2.2 ‘Burst Types’.

[Rationale:]

The burst structures used for DwPTS and UpPTS are different from that used for other physical channels. The detailed description of the burst structure of DwPTS and UpPTS can be found in subclause 7.2.2.2 ‘Burst Types’.

As described in subclause 7.2.2.2 ‘Burst Types’, there are no training sequences in DwPTS and UpPTS. The ~~SYNC~~SYNC-DL code in DwPTS and the ~~SYNC~~SYNC-UL code in UpPTS are not spread.

[Explanation difference:]

In low chip rate option, there are two dedicated Physical Synchronisation Channels, DwPTS for the down link synchronisation and UpPTS for the uplink synchronisation.

In high chip rate option, there is only one dedicated Physical Synchronisation Channel for down link synchronisation

7.2.3.56 Physical Uplink Shared Channel (PUSCH)

‘Common with the high chip rate TDD mode’

7.2.3.67 Physical Downlink Shared Channel (PDSCH)

‘Common with the high chip rate TDD mode’

7.2.3.7.8 The Page Indicator Channel (PICH)

[Description:]

The Page Indicator Channel (PICH) is a physical channel used, as in 3.84 MCPS TDD option, to carry the Page Indicators (PI).

The PICH ~~is can be~~ transmitted time multiplexed with a P/S-CCPCH and it is ~~sent at the same reference power level and~~ with the same antenna pattern configuration as the P-CCPCH. The power offset of PICH compared to the P-CCPCH is broadcast on BCH.

The Paging Indicator Channel (PICH) is a physical channel used to carry the paging indicators.

7.2.3.8.1 Mapping of Paging Indicators to the PICH bits

Figure X1 depicts the structure of a PICH transmission and the numbering of the bits within the bursts. The burst type as described in [6.2.2 ‘Burst Format’] is used for the PICH. N_{PIB} bits are used to carry the paging indicators, where $N_{PIB}=352$.

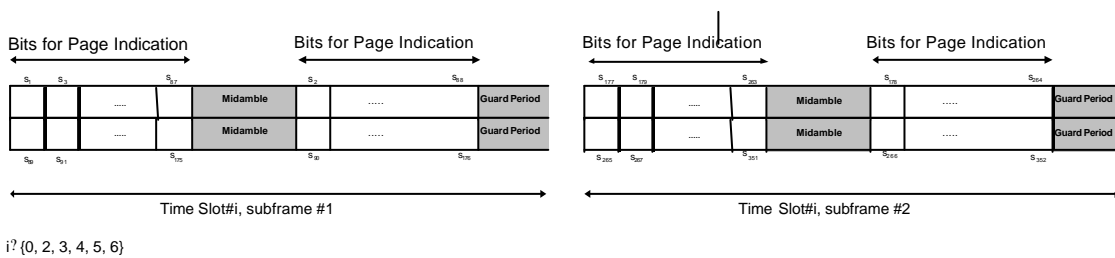


Figure X1: Transmission and numbering of paging indicator carrying bits in the PICH bursts

Each paging indicator P_q (where $P_q, q = 0, \dots, N_{PI}-1, P_q \in \{0, 1\}$) in one radio frame is mapped to the bits $\{s_{2L_{PI} \cdot q+1}, \dots, s_{2L_{PI} \cdot (q+1)}\}$ in subframe #1 or subframe #2. There are $N_{PIB} = 2 \cdot N_{PI} \cdot L_{PI}$ bits used for the paging indicator transmission in one radio frame. The mapping of the paging indicators to the bits $s_i, i = 1, \dots, N_{PIB}$ is shown in table X1.

Table X1: Mapping of the paging indicator

| P_q | Bits $\{s_{2L_{PI} \cdot q+1}, \dots, s_{2L_{PI} \cdot (q+1)}\}$ | Meaning |
|-------|--|---|
| 0 | $\{0, 0, \dots, 0\}$ | There is no necessity to receive the PCH |
| 1 | $\{1, 1, \dots, 1\}$ | There is the necessity to receive the PCH |

The bits $s_k, k = 1, \dots, S$ are then transmitted over the air as shown in [7].

In each radio frame, N_{PI} paging indicators are transmitted, using $L_{PI}=2, L_{PI}=4$ or $L_{PI}=8$ symbols. In table X2 this number is shown for the different possibilities of paging indicator lengths.

Table X2: Number N_{PI} of paging indicators per radio frame for different paging indicator lengths L_{PI}

| | $L_{PI}=2$ | $L_{PI}=4$ | $L_{PI}=8$ |
|--------------------------|------------|------------|------------|
| N_{PI} per radio frame | 88 | 44 | 22 |

7.2.3.8.2 Structure of the PICH over multiple radio frames

The structure of the PICH over multiple radio frames is common with 3.84 Mcps TDD, cf. [5.3.7.2 Structure of the PICH over multiple radio frames]

As in the 1.28 MCPS TDD option one burst type only is defined having a different structure with respect to the ones foreseen in the 3.84 MCPS TDD, the PICH structure will be different as well. The structure is chosen so that without defining reserved bits and for all possible PI lengths the bits corresponding to one PI can be symmetrically located in the time slot with respect to the midamble, as in 3.84 MCPS TDD. Moreover, the usage of two codes allows an easy time multiplexing with the P/S-CCPCH and about the same number of PIs per slot as in the 3.84 MCPS TDD mode. Figure below depicts the PICH structure and the numbering order of the transported bits, N_{PIB} , where N_{PIB} is equal to 176 bits.

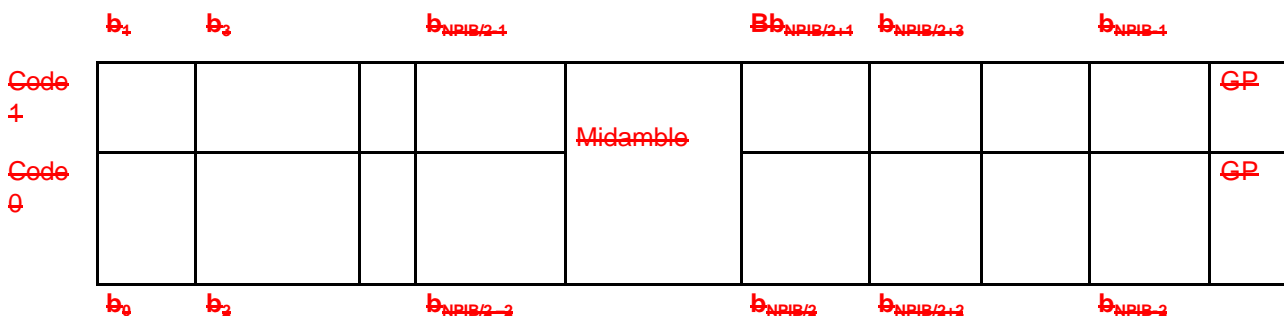


Figure: Transmission and numbering of PI carrying bits on the PICH

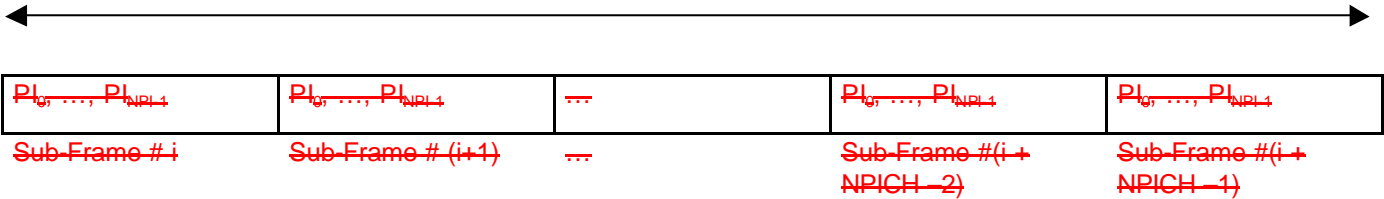
As in high chip rate TDD, Page Indicators can have different length (L_{PI}), where $L_{PI} = 2$ or 4 or 8 symbols respectively, as configured by the network. Therefore, the number of page indicators in a PICH burst are the ones reported in Table below.

Table : Number of Page Indicators (PI) in a PICH burst for the different PI length (P_L)

| | $L_{PI}=2$ | $L_{PI}=4$ | $L_{PI}=8$ |
|------------------------|------------|------------|------------|
| Number of PI per burst | 44 | 22 | 11 |

Similar to the 3.84 MCPS TDD option, Page Indicators can be transmitted for N_{PICH} consecutive sub-frames, which form a PICH block as described in figure. N_{PICH} is configurable by the higher layers so that $N = N_{PICH} * N_{PI}$. Page Indicators are transmitted in each PICH block.

1 PICH block



The structure of a paging block, consisting of a PICH and a PCH block is the same as in the high chip rate TDD option. As for the high chip rate TDD option, Page Indicator and Paging Group (PG) for a given user are computed by the higher layers in the network, where PI and PG are assigned independently one to the other.

A given PI corresponds to a P_L in the PICH burst of a PICH block at sub-frame number "n", according to the following rule:

$$p = PI \text{ mod } N_{PI};$$

$$n = PI \text{ div } N_{PI};$$

As in the high chip rate TDD, the Page Indicator P_L is mapped to two bit strings, where the first bit string consists of the bits ($b_{LPI,0}, \dots, b_{LPI,p-1}$) and the second bit string consists of the bits ($b_{NPID,2+LPI,0}, \dots, b_{NPID,2+LPI,p-1}$) within that burst. This mapping scheme allows for an equal distribution of all PIs within the PICH burst.

[Rationale:]

PICH physical channel allows to improve the DRX mode at the UE, saving power consumption. The benefit of this channel have already been evaluated for the high chip rate TDD and FDD mode where it is now included; therefore it is recommended for its inclusion in the low chip rate TDD option as well.

[Differences:]

While no difference exists in principle between high chip rate TDD and low chip rate TDD PICH physical channel, there are differences in the burst structure coming from the different burst formats and the different number of supporting resource units in the respective TDD options.

7.2.4 Beacon function of physical channels

[Description:]

For the purpose of measurements, a beacon function shall be provided by ~~particular~~ physical channels at particular locations (time slot, code). Considering about the physical character requirement of the beacon function, ~~DwPTS and the~~ P-CCPCH in low chip rate TDD ~~satisfy~~ satisfies this requirement.

[Rationale:]

For the purpose of measurements, a beacon function is provided by ~~the P-CCPCH~~ physical channels at particular locations, ~~and the DwPTS~~.

7.2.4.1 Location of physical channels with beacon function

~~The beacon function shall be provided by the physical channels that are allocated to channelisation code $C_{Q^{?16}}^{(k?1)}$ and $C_{Q^{?16}}^{(k?2)}$ in Timeslot#0.~~

~~Note that by this definition the P-CCPCH always has beacon characteristics. The DwPTS and the P-CCPCH provides the beacon function in low chip rate TDD.~~

7.2.4.2 Physical characteristics of the beacon function

The physical channels providing the beacon function:

- are transmitted with reference power;

- are transmitted without beamforming

use midambles $m^{(1)}$ and $m^{(2)}$ exclusively in this time slot ~~when P-CCPCH provide the beacon function~~

[Explanation difference:]

~~— In high chip rate TDD, a beacon function has to be defined for channels other than the P-CCPCH, because there are two cases of synchronisation and the possibility of multiframes for the P-CCPCH. The location of beacon channels is fixed in low chip rate TDD.~~

~~In the low chip rate option, only the P-CCPCH and the DwPTS provides the beacon function.~~

7.2.5 Midamble Allocation for Physical Channels

'Common with the high chip rate TDD mode'

7.3 Mapping of transport channels to physical channels

[Description:]

This clause describes the way in which transport channels are mapped onto physical resources.

[Rational:]

| Transport channels | Physical channels |
|--------------------|---|
| DCH | Dedicated Physical Channel (DPCH) |
| BCH | Primary Common Control Physical Channels (P-CCPCH) |
| PCH | Primary Common Control Physical Channels (P-CCPCH) Secondary Common Control Physical Channels (S-CCPCH) |
| FACH | Primary Common Control Physical Channels (P-CCPCH) Secondary Common Control Physical Channels (S-CCPCH) |
| RACH | Physical Random Access Channel (PRACH) |
| USCH | Physical Uplink Shared Channel (PUSCH) |
| DSCH | Physical Downlink Shared Channel (PDSCH) |
| | Downlink Pilot Time Slot Channel (DwPTS DwPCH) |
| | Uplink Pilot Time Slot Channel (UpPTS UpPCH) |
| | PICH |
| | FPACH |

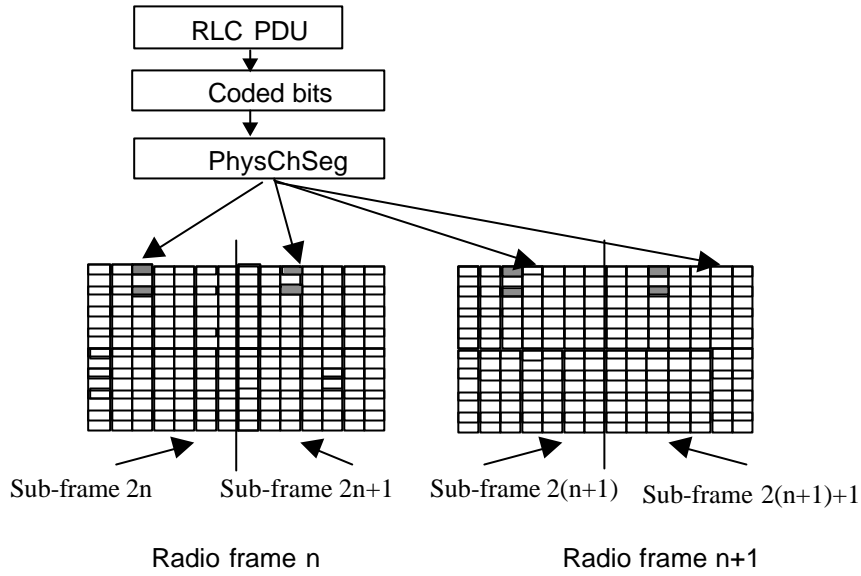
Transport channel to physical channel mapping

[Explanation difference:]

The PCH and FACH can be mapped on ~~P-CCPCHs and the~~ S-CCPCHs in low chip rate TDD option and the BCH ~~will only~~ is mapped ~~into onto the~~ P-CCPCHs. The ~~dedicated~~ physical channels ~~of~~ DwPTS ~~DwPCH~~ and UpPTS ~~UpPCH~~ are used for downlink and uplink pilots. The physical channel FPACH is used to answer the UE and to ~~request an~~ adjustment of the timing and synchronization shift of the UE. These three channels are used for synchronization operation. For a detailed description, see subclause 7.3.2 of 25.928.

7.3.1 Dedicated Transport Channels

Figure : Mapping of PDU onto the physical bearer(TTI= 20ms)



[Description:]

The figure shows the mapping of PDU onto physical bearer.

[Explanation difference:]

The mapping of PDU into dedicated channel is different from that of high chip rate TDD option according to the different frame structure. See separate sections (clause 8.1.11) for further explanation of the segmentation into sub-frames.

7.3.2 Common Transport Channels

[Description:]

The following figure shows the mapping of BCH, FACH and PCH transport channels onto the P-CCPCHs :

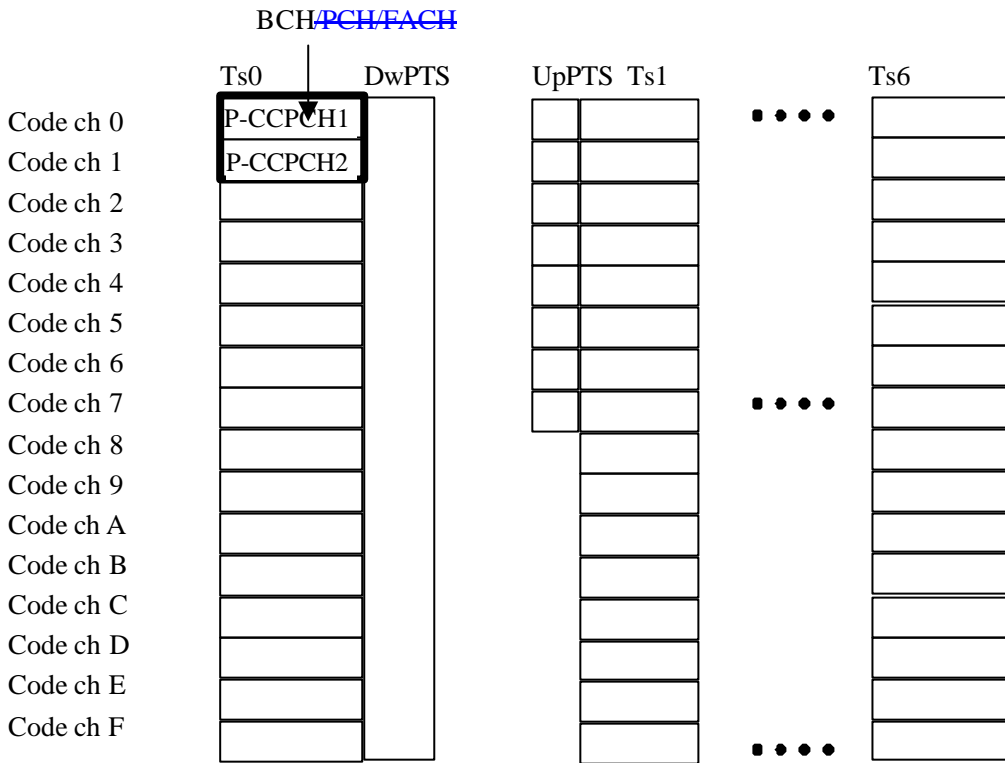


Figure Transport channels mapping onto the physical channels

In low chip rate option, There are two P-CCPCH, P-CCPCH 1 and P-CCPCH 2 which are mapped onto channelisation codes $c_{Q?16}^{(k?1)}$ and $c_{Q?16}^{(k?2)}$ (spreading factor 16). A cell should always contain P-CCPCH 1 and P-CCPCH 2. The transport channels mapped onto the P-CCPCH shall effectively be mapped onto P-CCPCH 1 and P-CCPCH 2 using the multi-code function in the channel coding and multiplexing (See physical channel segmentation in 25.222). As far as the S-CCPCH is concerned, two cases can be considered. Either there are as well two S-CCPCH, S-CCPCH 1 and S-CCPCH 2, mapped onto two codes of spreading factor 16 ~~or there is a single SCCPCH corresponding to a single code of spreading factor 8.~~ The S-CCPCHs may be mapped on any DL time slot. (as show in the figure above). More details are giving as following:

The BCH is mapped on a pre-defined number of RUs/physical channels, so that the UE can unambiguously decode it. As it is for the TDD high chip rate option and for FDD mode, the low chip rate option as well foresees for one P-CCPCH only. ~~On the combined P-CCPCH1+P-CCPCH2, different logical channels can be mapped according to the multi-frame structure.~~

[Rational:]

7.3.2.1 The Broadcast Channel (BCH)

The BCH is always mapped on the P-CCPCH1+P-CCPCH2. Due to the adoption of smart antenna, in order to provide the coverage of the whole cell, the P-CCPCHs must have in general higher transmission power level with omni-directional or sectorial pattern (without adaptive beamforming) compared with the other physical channels which can be adaptively beamformed. ~~The BCH is time multiplexed with other channels in the multi-frame.~~

The UE can find the beginning of each block which is delivered on the P-CCPCHs; that is the beginning of the interleaving period, through the DwPTS sequence and its relative phase with respect to the P-CCPCHs

midamble sequences. Each DwPTS can have 4 different phases [with respect to the MA of the P-CCPCH](#) and can be independently assigned by the Node B. ~~Several continues different phase DwPTSs's combination can indicate the BCH's position in the multi-frame and the start position of the interleaving period. Also the beginning of the control multiframe can be detected from phase relations. To ensure correct decisions, an additional bit coded together with a BCH block, allows the UE to know the BCH interleaving block in P-CCPCHs.~~

7.3.2.2 The Paging Channel (PCH)

The PCH is a special broadcast channel used to page UEs from RNC. ~~As mentioned above, it can also be mapped onto the P-CCPCHs time multiplexed with the BCH, FACH(see figure above) , and, therefore, transmitted with the same power level and antenna pattern as those of the BCH. PCH, FACH and BCH will occupy their own blocks in the multi-frame structure. And this is the preferred way, in some condition, the PCH can is be mapped onto a different physical channel (S-CCPCH or SCCPCH1+SCCPCH2, on any DL time slot but not on the codes used for the P-CCPCHs.) , the location of PCH is indicated on the BCH.(This gives more flexibility to the system.)~~[S-CCPCH.](#)

7.3.2.2 The Forward Channel (FACH)

[The FACH is mapped onto one or several S-CCPCHs. The location of the FACH is indicated on the BCH and both capacity and location can be changed, if required. FACH may or may not be power controlled.](#)

~~The FACH is used to carry control information to a mobile station when the system knows the location cell of the mobile station. The FACH may also carry short user packets. The FACH can be mapped onto the P-CCPCHs time multiplexed with the BCH and PCH, and, therefore, transmitted with the same power level and antenna pattern as those of the BCH. PCH, FACH and BCH will occupy their own blocks in the multi-frame structure. And this is the preferred way, in some condition, the FACH can be mapped onto a different physical channel (S-CCPCH or SCCPCH1+SCCPCH2 , on any DL time slot but not on the codes used for the P-CCPCHs.) , the location of FACH is indicated on the BCH.(This gives more flexibility to the system.)~~

[Explanation difference:]

[As In the high chip rate option, the BCH is always mapped onto P-CCPCH and the PCH/FACH onto the S-CCPCH. The P-CCPCH always contains only the BCH . The secondary SCH indicates in which timeslot a mobile can find the PCCPCH containing BCH. And the location of PCH is indicated on the BCH.](#)

~~In low chip rate option, the BCH is mapped only onto the P-CCPCHs (Primary Common Control Physical CHannel). The P-CCPCHs can also contain the PCH and FACH as well as the BCH. The P-CCPCHs are mapped onto the DL time slot preceding the DwPTS using two codes of that time slot (as shown in the figure 1) as described above. According the frame structure, P-CCPCHs carrying the BCH is followed by DwPTS, so when the UE detects the SYNC word, it can immediately find the BCH. [The beginning of the TTI for the P-CCPCH can be derived from the modulation of the DwPTS.](#)~~

7.3.2.3 The Random Access Channel (RACH)

[Description:]

[The RACH has intraslot interleaving only and is mapped onto PRACH. More than one slot per frame may be administered for the PRACH. The location of slots allocated to PRACH is broadcast on the BCH. The uplink sync codes \(SYNC-UL sequences\) used by the UEs for UL synchronisation have a well known association with the P-RACHs, as broadcast by the BCH. On the P-RACH, both power control and uplink synchronisation control are used. The burst type used on the P-RACH is the same as that for a dedicated physical channel.](#)

~~The RACH is mapped onto the P-RACH physical channel. The P-RACH configuration (time slot number and assigned spreading codes) is broadcast through the BCH information.~~

[Rationale:]

The RACH is mapped onto the P-RACH physical channel. The P-RACH can be configured by the network operator.

The P-RACHs can use either any spreading factor 16 RU or any spreading factor 8 RU in any UL time slot of the sub-frame or 4. The spreading codes and time slots assigned to the P-RACHs are broadcast by the cell from the BCH. The capability of mapping RACH onto any UL time slot offers more flexibility to the system. The interference handling is then configurable. As the RACH is different from the other traffic it may be advantageous to distribute the RACH resources on several time slots.

The uplink sync codes (SYNC1 SYNC-UL sequences) used by the UEs for UL synchronisation have a well known association to the P-RACHs, as broadcast by the BCH.

On the P-RACH, both power control and uplink synchronisation control is used.

The burst type used on the P-RACH is the same as for a traffic channel.

[Explanation difference:]

In low chip rate TDD option the random access procedure has two-step approach. The PRACH uses the close loop power control algorithm which is similar with the traffic channel..

In high chip rate TDD option the PRACH uses open loop power control. The details of the employed open loop power control algorithm may be different from the corresponding algorithm on other channels.

In low chip rate TDD option the burst type used on the P-RACH is the same as for a traffic channel while in high chip rate TDD option the burst type of the PRACH is a little different from the traffic channel.

7.3.2.4 The Uplink Shared Channel (USCH)

'Common with the high chip rate TDD mode'

7.3.2.5 The Downlink Shared Channel (DSCH)

'Common with the high chip rate TDD mode'

Annex A (Normative): Basic Midamble Codes

A.1 Basic Midamble Codes for Burst Type 1 and PRACH Burst Type

Table: Basic Midamble Codes

| <u>Code ID</u> | <u>Basic Midamble Codes of length 128</u> |
|----------------|---|
| <u>0</u> | <u>B2AC420F7C8DEBFA69505981BCD028C3</u> |
| <u>1</u> | <u>0C2E988E0DBA046643F57B0EA6A435E2</u> |
| <u>2</u> | <u>D5CEC680C36A4454135F86DD37043962</u> |
| <u>3</u> | <u>E150D08CAC2A00FF9B32592A631CF85B</u> |
| <u>4</u> | <u>E0A9C3A8F6E40329B2F2943246003D44</u> |
| <u>5</u> | <u>FE22658100A3A683EA759018739BD690</u> |
| <u>6</u> | <u>B46062F89BB2A1139D76A1EF32450DA0</u> |
| <u>7</u> | <u>EE63D75CC099092579400D956A90C3E0</u> |

| | |
|-----------|---|
| <u>8</u> | <u>D9C0E040756D427A2611DAA35E6CD614</u> |
| <u>9</u> | <u>EB56D03A498EC4FEC98AE220BC390450</u> |
| <u>10</u> | <u>F598703DB0838112ED0BABB98642B665</u> |
| <u>11</u> | <u>A0BC26A992D4558B9918986C14861EFF</u> |
| <u>12</u> | <u>541350D109F1DD68099796637B824F88</u> |
| <u>13</u> | <u>892D344A962314662F01F9455F7BC302</u> |
| <u>14</u> | <u>49F270E29CCD742A40480DD4215E1632</u> |
| <u>15</u> | <u>6A5C0410C6C39AA04E77423C355926DE</u> |
| <u>16</u> | <u>7976615538203103D4DBCC219B16A9E1</u> |
| <u>17</u> | <u>A6C3C3175845400BD2B738C43EE2645F</u> |
| <u>18</u> | <u>A0FD56258D228642C6F641851C3751ED</u> |
| <u>19</u> | <u>EFA48C3FC84AC625783C6C9510A2269A</u> |
| <u>20</u> | <u>62A8EB1A420334B23396E8D76BC19740</u> |
| <u>21</u> | <u>9E96235699D5D41C9816C921023BC741</u> |
| <u>22</u> | <u>4362AE4CAE0DCC32D60A3FED1341A848</u> |
| <u>23</u> | <u>454C068E6C4F190942E0904B95D61DFB</u> |
| <u>24</u> | <u>607FEEA6E2E99206718A49C0D6A25034</u> |
| <u>25</u> | <u>E1D1BCDA39A09095B5C81645103A077C</u> |
| <u>26</u> | <u>994B445E558344DE211C8286DDD3D1A3</u> |
| <u>27</u> | <u>C15233273581417638906ADB61FDCA3C</u> |
| <u>28</u> | <u>8B79A274D542F096FB1388098230F8A1</u> |
| <u>29</u> | <u>DF58AC1C5F44B2A40266385CE1DA5640</u> |
| <u>30</u> | <u>B5949A1CC69962C464401D05FF5C1A7A</u> |
| <u>31</u> | <u>85AC489841ED3EAA2D83BBB0039CC707</u> |
| <u>32</u> | <u>AE371CC144BC95923CA8108D8B49FE82</u> |
| <u>33</u> | <u>7F188484A649D1C22BDA1F09D49B5117</u> |
| <u>34</u> | <u>ADAA3C657089DEF7C0284903A491C9B0</u> |
| <u>35</u> | <u>C3F96893C7504DC3B51488604AF64F4C</u> |
| <u>36</u> | <u>B4002F5AE0CE8623AC979D368E9148C1</u> |
| <u>37</u> | <u>0EEBCC0C795C02A106C24ABB36D08C6E</u> |
| <u>38</u> | <u>4B0F537E384A893F58971580D9894433</u> |
| <u>39</u> | <u>08E0035AB29B7ECC53C15DAA0687CC8F</u> |

| | |
|-----------|---|
| <u>40</u> | <u>8611ACBC4C82781D77654EE862506D60</u> |
| <u>41</u> | <u>63315261A8F1CB02549802DBFD197C07</u> |
| <u>42</u> | <u>9A2609A434F43E7DCADC0E22B2EF4012</u> |
| <u>43</u> | <u>F4C9F0A127A88461209ABF8C69CE4D00</u> |
| <u>44</u> | <u>C79124EE3FFC28C5C4524D2B01670D42</u> |
| <u>45</u> | <u>C91985C4FED53D09361914354BA80E79</u> |
| <u>46</u> | <u>82AA517260779ECFF26212C1A10BDC29</u> |
| <u>47</u> | <u>561DE2040ACB458E0DBD354E43E111D9</u> |
| <u>48</u> | <u>2E58C7202D17392BC1235782CEFABB09</u> |
| <u>49</u> | <u>C4FAA121C698047650F6503126A577C1</u> |
| <u>50</u> | <u>E7B75206A9B410E44346E0DAE842A23C</u> |
| <u>51</u> | <u>3F8B1C32682B28D098D3805ED130EA7F</u> |
| <u>52</u> | <u>8D5FC2C1C6715F824B401434C8D4BB82</u> |
| <u>53</u> | <u>0B2A43453ACC028FE6EB6E1CB0740B59</u> |
| <u>54</u> | <u>BC56948FC700BA4883262EE73E12D82A</u> |
| <u>55</u> | <u>558D136710272912FA4F183D1189A7FD</u> |
| <u>56</u> | <u>5709E7F82DC6500B7B12A3072D182645</u> |
| <u>57</u> | <u>86D4F161C844AE5E20EE39FD5493B044</u> |
| <u>58</u> | <u>8729B6EDC382B152185885F013DAE222</u> |
| <u>59</u> | <u>154C45B50720F4C362C14C77FE8335A1</u> |
| <u>60</u> | <u>C6A0962890351F4EB802DE43A7662C9E</u> |
| <u>61</u> | <u>D19D69D6B380B4B22457CB80033519F0</u> |
| <u>62</u> | <u>C7D89509FB0DAE9255998E0A00C2B262</u> |
| <u>63</u> | <u>DFD481C652C0C905D61D66F1732C4AA2</u> |
| <u>64</u> | <u>06C848619AF1D6C910A8EAC4B622FC06</u> |
| <u>65</u> | <u>0635E29D4E7AC8ABC189890241F45ECA</u> |
| <u>66</u> | <u>B272B020586AAD7B093AC2F459076638</u> |
| <u>67</u> | <u>B608ACE46E1A6BC96181EEDD88B54140</u> |
| <u>68</u> | <u>0A516092B3ED7849B168AFE223B8670E</u> |
| <u>69</u> | <u>D1A658C5009E04D0D7D5E9205EE663E8</u> |
| <u>70</u> | <u>AC316DC39B91EB60B1AABD8280740432</u> |
| <u>71</u> | <u>E3F06825476A026CD287625E514519FC</u> |

| | |
|------------|---|
| <u>72</u> | <u>A56D092080DDE8994F387C175CC56833</u> |
| <u>73</u> | <u>15EA799DE587C506D0CD99A408217B05</u> |
| <u>74</u> | <u>A59C020BAB9AF6D3F813C391CA244CD2</u> |
| <u>75</u> | <u>74B0101EB9F3167434B94BABC8378882</u> |
| <u>76</u> | <u>CE752975C8DA9B0100386DB82A8C3D20</u> |
| <u>77</u> | <u>BBB38DCDB1E9118570AC147DC05241A4</u> |
| <u>78</u> | <u>944ABBF0866098101F6971731AB2E986</u> |
| <u>79</u> | <u>2BB147B2A30C68B4853F90481A166EB6</u> |
| <u>80</u> | <u>444840ACCF3F23C45B56D7704BF18283</u> |
| <u>81</u> | <u>87604F7450D1AD188C452981A5C7FC9B</u> |
| <u>82</u> | <u>8C3842EBC948A65BC4C8B387F11B7090</u> |
| <u>83</u> | <u>10B4767D071CF5DB2288E4029576135A</u> |
| <u>84</u> | <u>6F07AAB697CD0089572C6B062E2018E4</u> |
| <u>85</u> | <u>D3D65B442057E613A8655060C8D29E27</u> |
| <u>86</u> | <u>5EDA330514C604BF4E0894E09EC57A74</u> |
| <u>87</u> | <u>B0899CD094060724DED82AE85F18A43A</u> |
| <u>88</u> | <u>B2D999B86DF902BC25015CAE3A0823C4</u> |
| <u>89</u> | <u>C23CD40F04242B92D46EED82CD9A9A18</u> |
| <u>90</u> | <u>D22DDCC5CB82960125DD24655F3C8788</u> |
| <u>91</u> | <u>54987218FBD99AE4340FD4C9458E9850</u> |
| <u>92</u> | <u>BE4341822997A7B11EA1E8A1A2767005</u> |
| <u>93</u> | <u>255200FBA6EE48E6DE0A82B0461B8D0F</u> |
| <u>94</u> | <u>6FBD58A663932423503690CF9C171701</u> |
| <u>95</u> | <u>D215033A4AA87EC1C232BAC7EDA09370</u> |
| <u>96</u> | <u>CA0959B01AE48E80204F1E4A3F29CE55</u> |
| <u>97</u> | <u>582043413B9B825903E3A3545ED59463</u> |
| <u>98</u> | <u>5016541922971C703D16E284CBDF633B</u> |
| <u>99</u> | <u>7347EF160A1733CA98D43608A83A920B</u> |
| <u>100</u> | <u>908B22AD433CCA00B3FD47C691F1A290</u> |
| <u>101</u> | <u>BB22A272FC6923DF1B43BA4118806570</u> |
| <u>102</u> | <u>0FA75C87474836B47DC7624D61193802</u> |
| <u>103</u> | <u>A22EBA0658A4D0FF1E9CA5030A65CC06</u> |

| | |
|------------|---|
| <u>104</u> | <u>6C9C51CA15F1F4981F4C46180A6A6697</u> |
| <u>105</u> | <u>4C847ACF8BC15359C405322851C9BDE2</u> |
| <u>106</u> | <u>C1D29499C0082C9DE473ED15B14D63E0</u> |
| <u>107</u> | <u>7E85ECC98AC761005076C5572869A431</u> |
| <u>108</u> | <u>D8F11121595B8F49F78A7039E44126A0</u> |
| <u>109</u> | <u>1A0BC814445FD71C8E5B1A9163ED2059</u> |
| <u>110</u> | <u>A7591F27F8B0C00C68CC41697954FA04</u> |
| <u>111</u> | <u>6CA2CE595E7406D79C4840183D41B9D0</u> |
| <u>112</u> | <u>C093D3CC701FC20E66F5AB22516C5460</u> |
| <u>113</u> | <u>D0E0CDE9B595546B96C4F8066B469020</u> |
| <u>114</u> | <u>E99F743A451431C8B427054A4E6F2007</u> |
| <u>115</u> | <u>C0D21A344A2C07DF2A6EBE6250C7B91E</u> |
| <u>116</u> | <u>F031223E282CF7A4D8EF174A908668AE</u> |
| <u>117</u> | <u>E4BD244AC16C55C7137FB068FD44280C</u> |
| <u>118</u> | <u>C44920DE2028F19FC2AAB36A0DCFDAD0</u> |
| <u>119</u> | <u>3FA7054E77135250699E6C8A11600742</u> |
| <u>120</u> | <u>D5740B4D8870C1C5B5A214C4266FC537</u> |
| <u>121</u> | <u>F0B7942D43BB6F38446442EB8126AB80</u> |
| <u>122</u> | <u>83DB9534EAD6238FA8968798CDF04848</u> |
| <u>123</u> | <u>EB9663CDDC2B291690703125BABCB800</u> |
| <u>124</u> | <u>84D547225D4BBD20DEF1A583240C6E0F</u> |
| <u>125</u> | <u>B51F6A771838BE934724AEA6A2669802</u> |
| <u>126</u> | <u>D92AC05E10496794BBDC115233B1C068</u> |
| <u>127</u> | <u>D3ACF0078EDA9856BBB0AF8651132103</u> |

~~A.2 Basic Midamble Codes for Burst Type 2~~

~~A.3-2 Association between Midambles and Channelisation Codes~~

~~The following mapping schemes apply for the association between midambles and channelisation codes if no midamble is allocated by higher layers. Secondary channelisation codes are marked with (*). These associations apply for both UL and DL.~~

~~The following mapping schemes apply for the association between midambles and channelisation codes if no midamble is allocated by higher layers. These associations apply both for UL and DL.~~

A.3.2.1 Association for K=16 Midambles

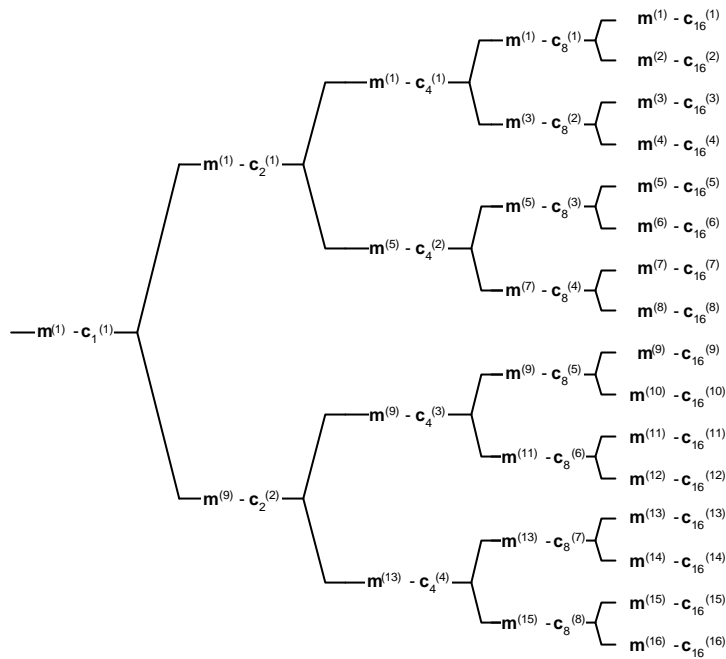
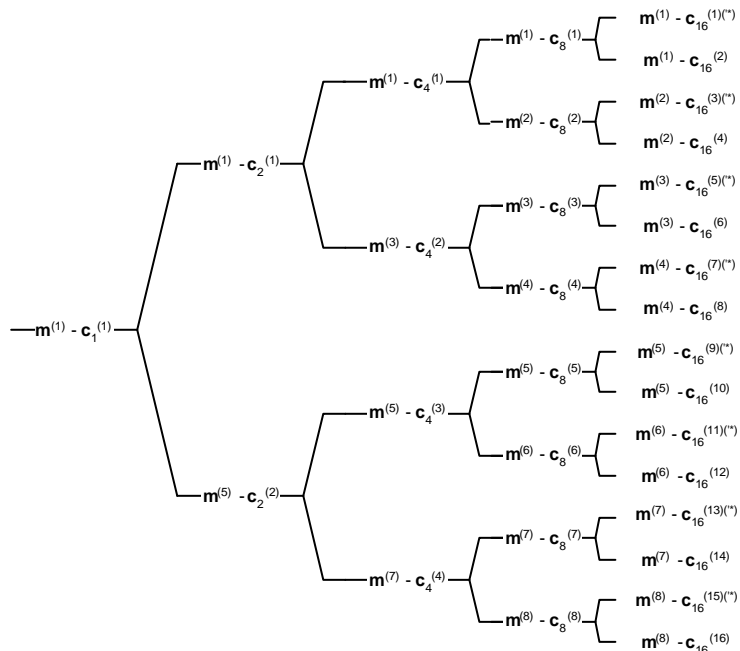


Figure A-1: Association of Midambles to Spreading Codes for K=16

A.3.2.2 Association for K=8 Midambles



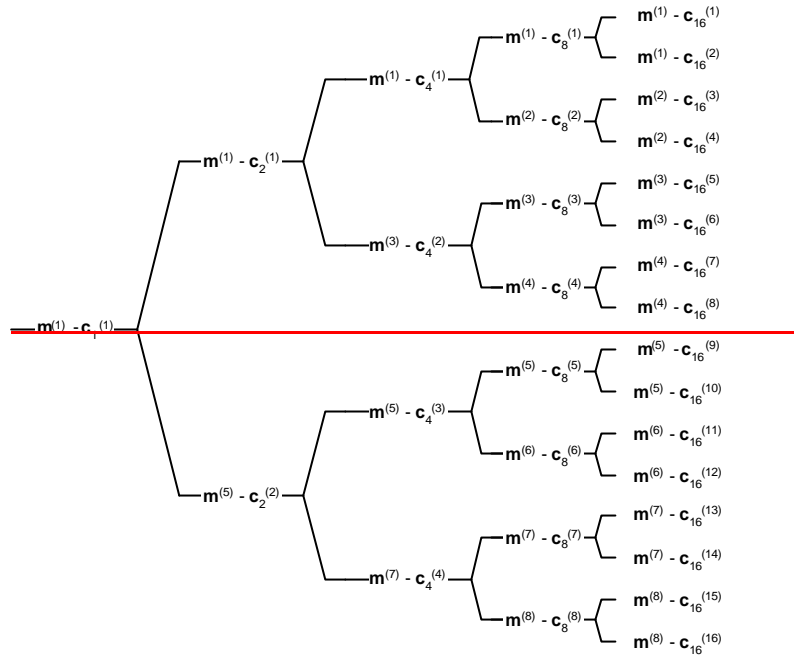
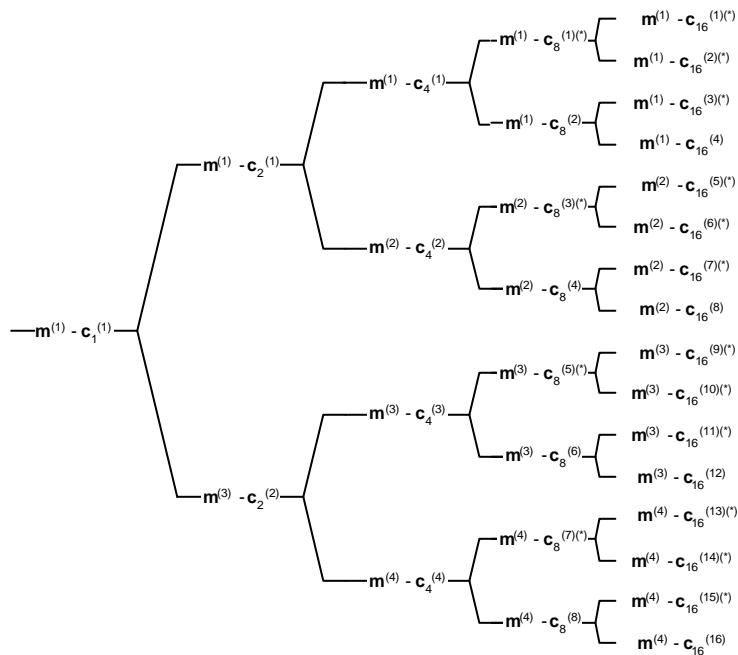


Figure A-2: Association of Midambles to Spreading Codes for K=8

A.3.2.3 Association for K=4 Midambles



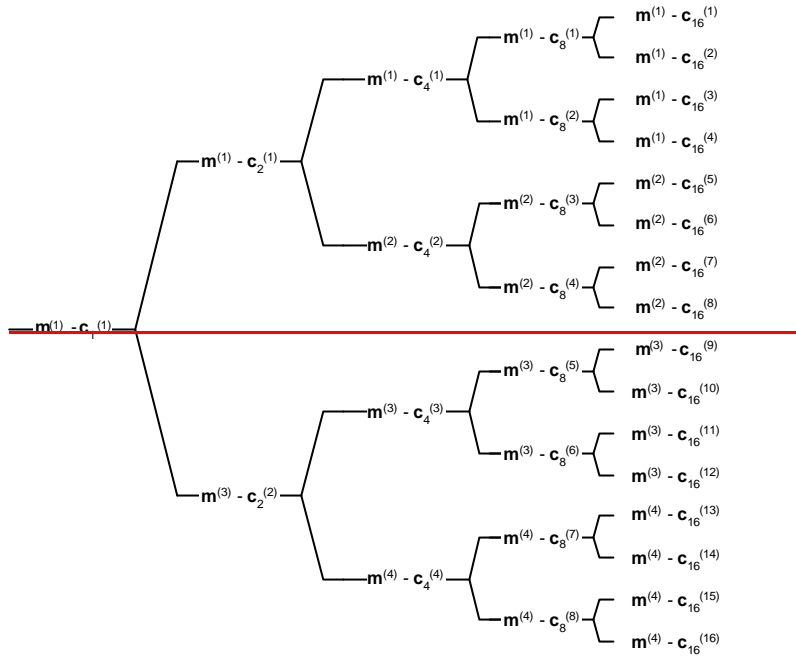
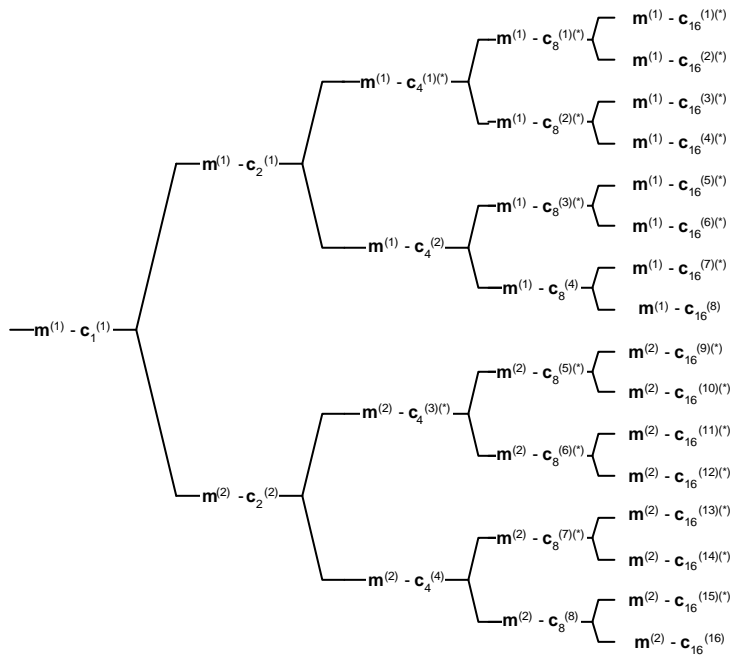


Figure A-3: Association of Midambles to Spreading Codes for K=4

A.3.2.4 Association for K=2 Midambles



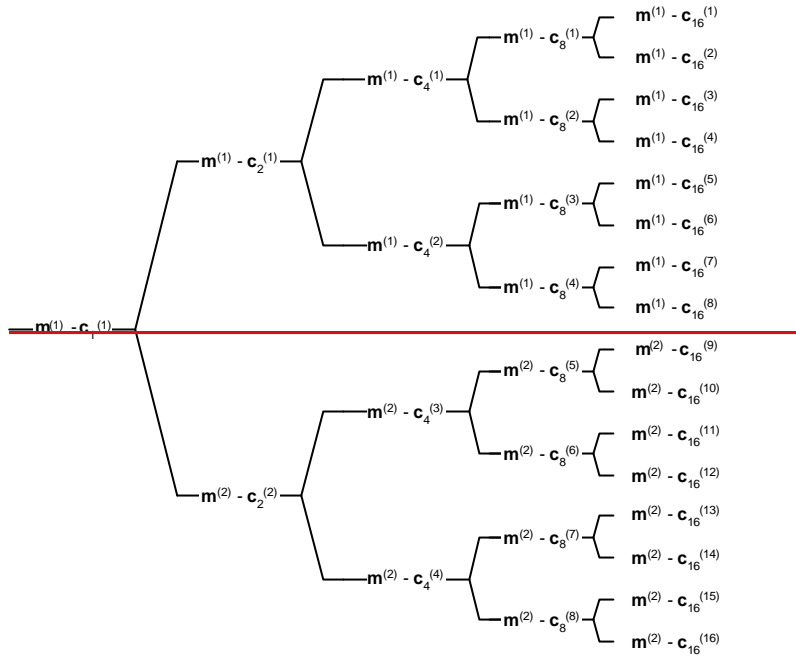
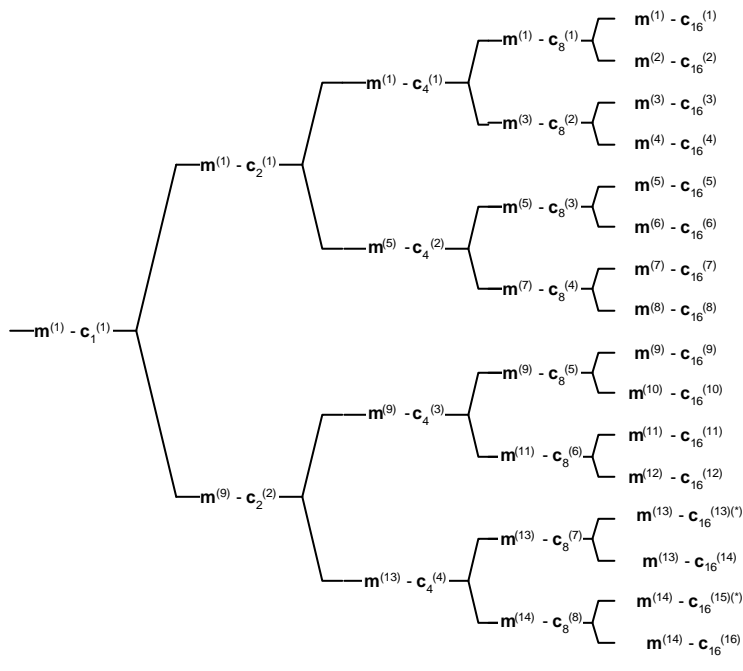


Figure A-4: Association of Midambles to Spreading Codes for K=2

A.3.2.5 Association for K=14 Midambles



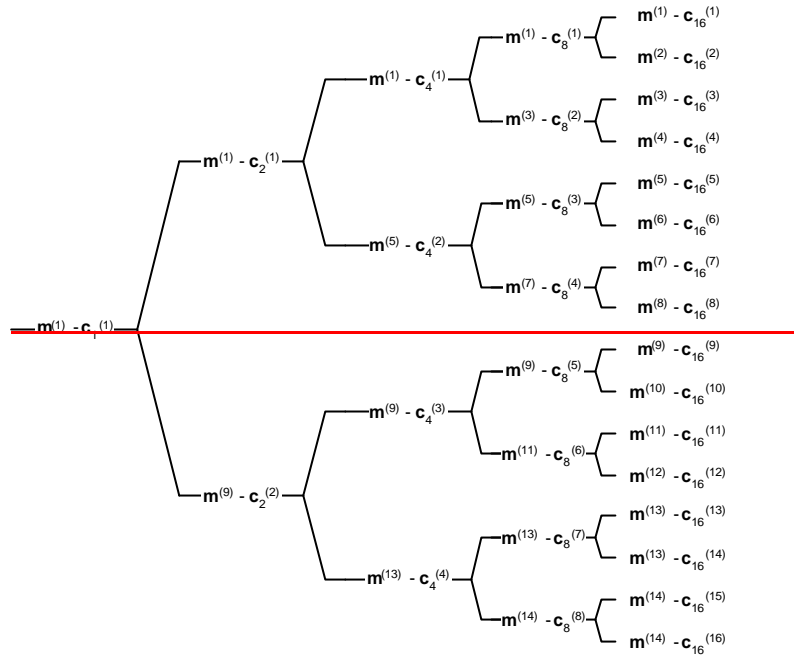
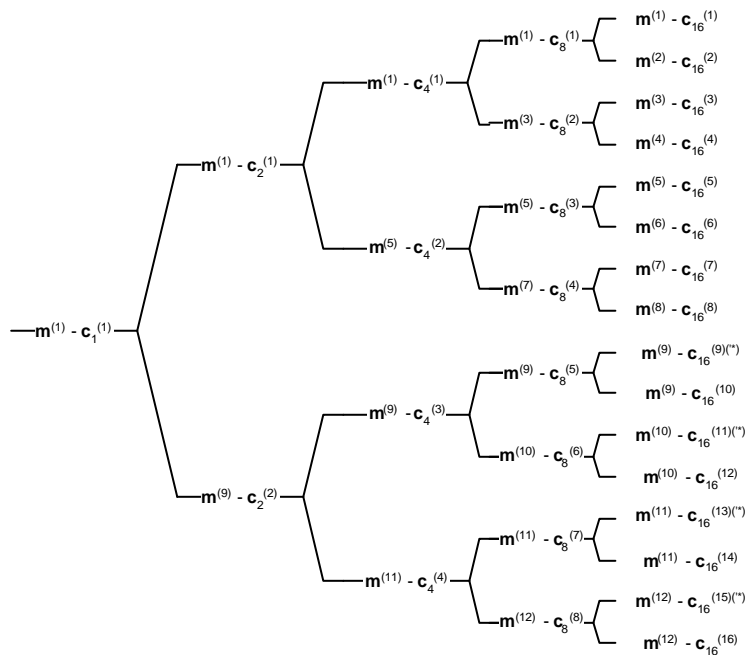


Figure A-5: Association of Midambles to Spreading Codes for K=14

A.3.2.6 Association for K=12 Midambles



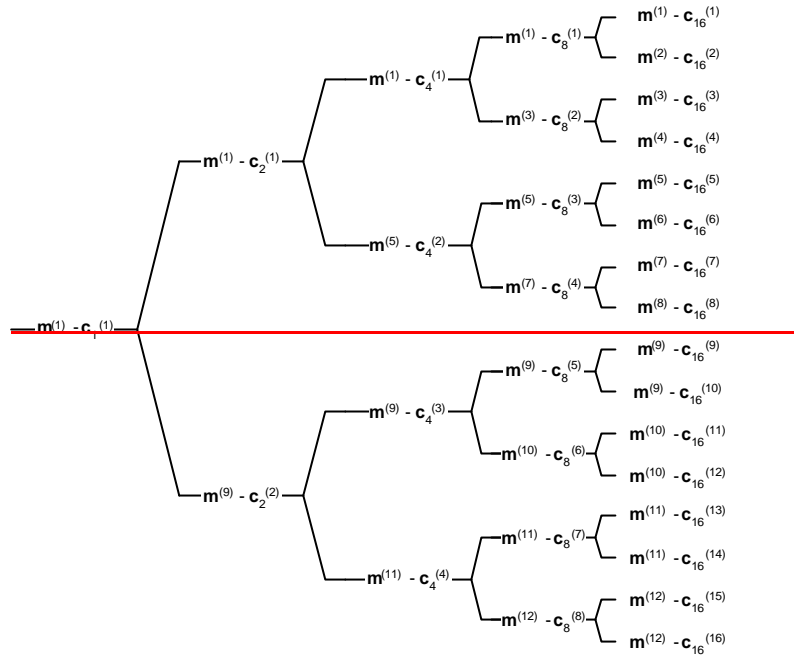
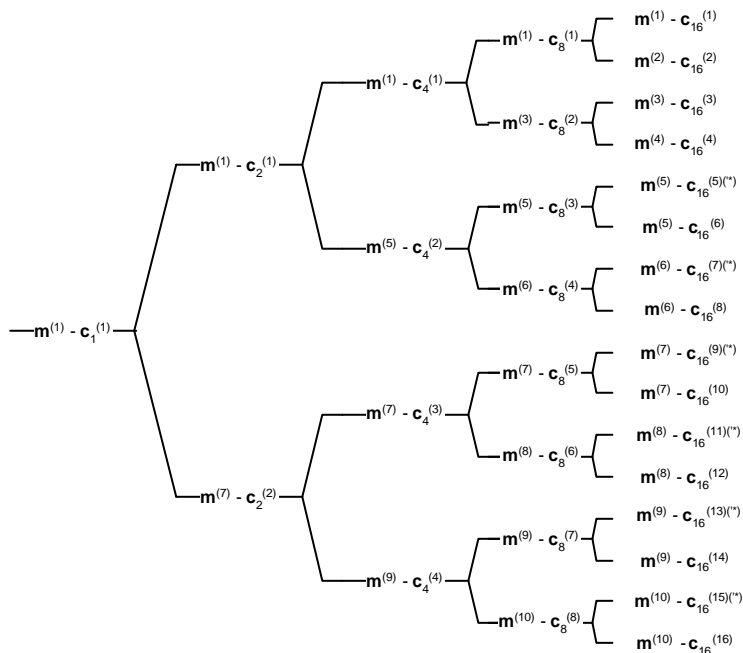


Figure A-6: Association of Midambles to Spreading Codes for K=12

A.32.7 Association for K=10 Midambles



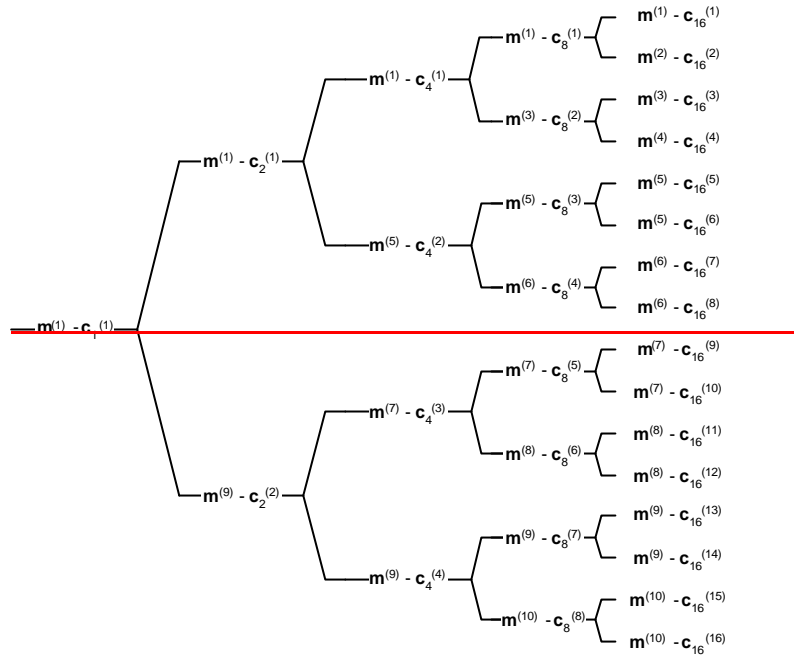
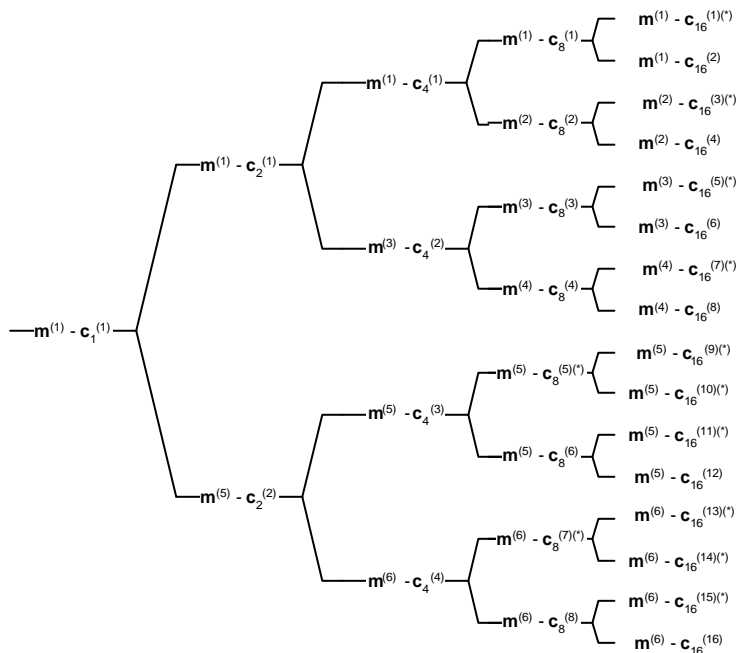


Figure A-7: Association of Midambles to Spreading Codes for K=10

A.32.8 Association for K=6 Midambles



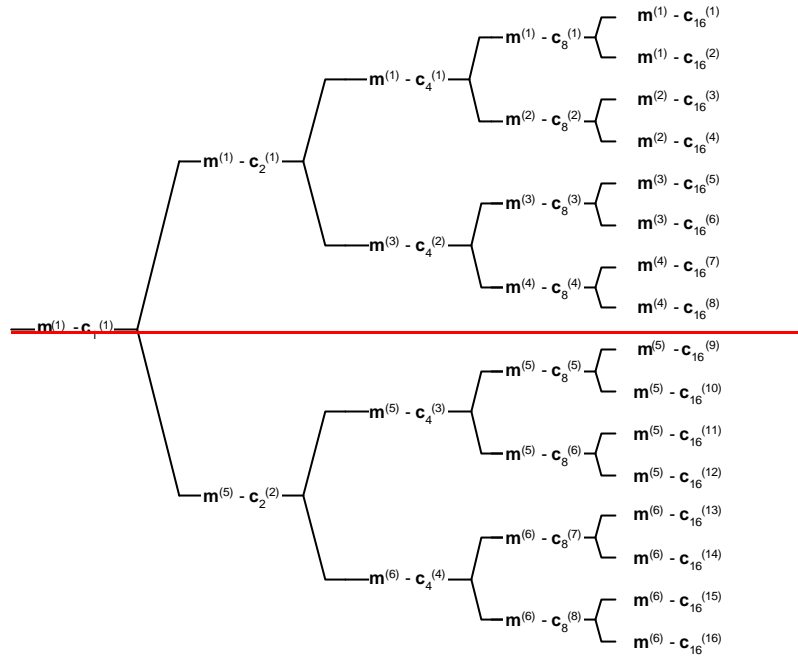


Figure A-8: Association of Midambles to Spreading Codes for K=6

Annex B (Informative): CCPCH Multiframe Structure

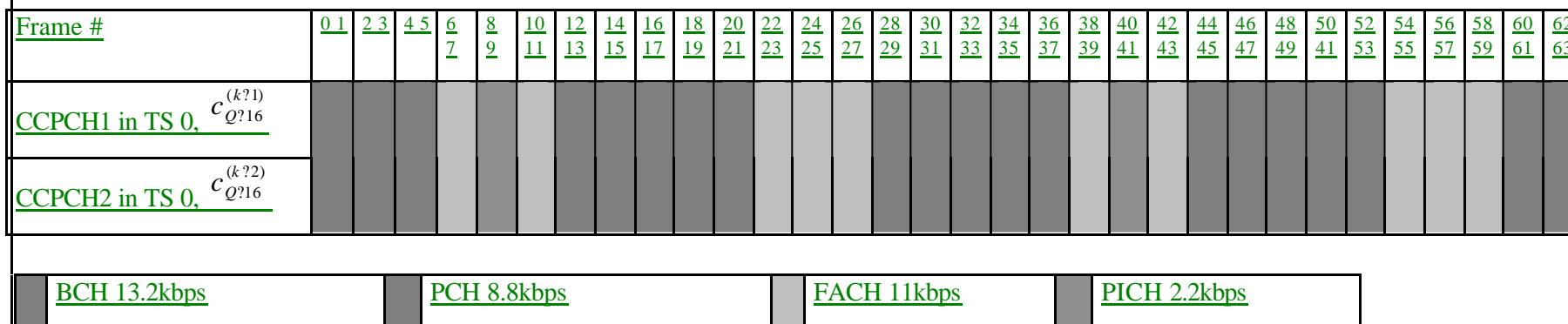


Figure B.1: Example for a multiframe structure for CCPCHs and PICH that is repeated every 64th frame (128 sub-frame)

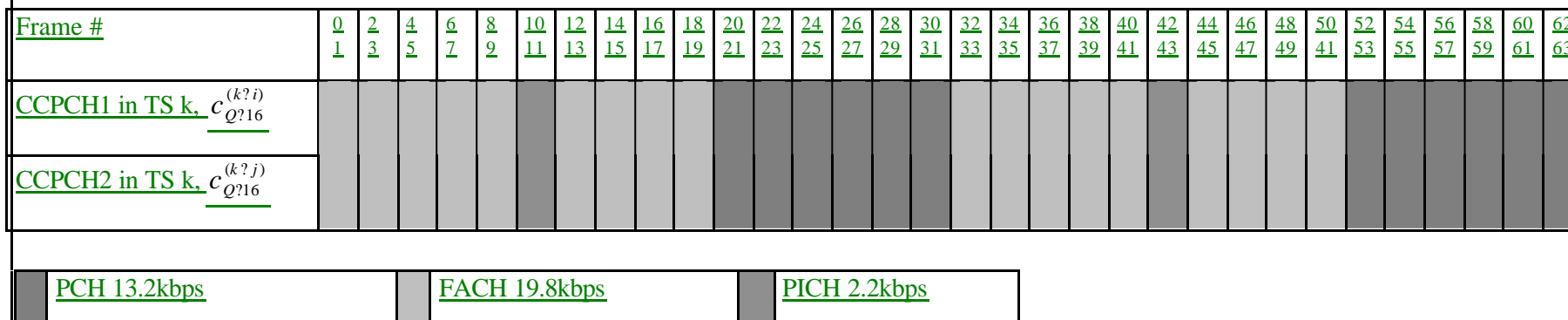


Figure B.2: Example for a multiframe structure for S-CCPCHs and PICH that is repeated every 64th frame, $i, j = 1, \dots, 16$ ($i \neq j$), $k = 0, 1$ (128 sub-frame)

| Frame # | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | 71 |
|---------|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |



Figure B.1: Example for a multiframe structure for P-CCPCHs that is repeated every 72th frame (144 sub-frame)

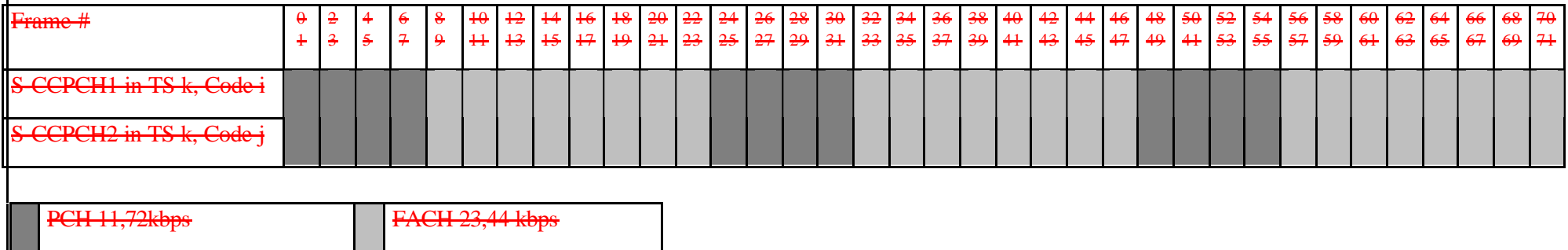


Figure B.2: Example for a multiframe structure for S-CCPCHs that is repeated every 72th frame, i,j=1-16 (144 sub-frame)

The two codes at SF 16 which define the two P-(S)CCPCHs, are jointly used to deliver the same higher layer message! this means that it not possible to send contemporarily two different messages (e.g. BCH and PCH) onto the two different codes of the P-(S)CCPCH

Annex C (Informative): Examples of the association of DL TPC commands to UL uplink time slots for 1.28 Mcps TDD

Table C.1 Two examples of the association of DL TPC commands to UL uplink time slots with $N_{ULslot}=3$

Case 1: $N_{UL_TPCSymbols}=2$; Case 2: $N_{UL_TPCSymbols}=4$

| Sub-Frame Number | Case 1 (2 UL TPC symbols) | | The order of the served UL time slot and CCTrCH pairs (UL time slot and CCTrCH number) | Case 2 (4 UL TPC symbols) | |
|------------------|--|---|--|------------------------------|--|
| | The order of UL TPC symbols | | | The order of UL TPC symbols | |
| <u>SFN'=0</u> | <u>(1st UL_{pos}=0)</u> | 0 | 0 (TS3) | 0 | <u>(1st UL_{pos}=0)</u> |
| | | 1 | 1 (TS4) | 1 | |
| | | | 2 (TS5) | 2 | |
| | | | 0 (TS3) | 3 | |
| <u>SFN'=1</u> | <u>(1st UL_{pos}=2)</u> | 0 | 0 (TS3) | 0 | <u>(1st UL_{pos}=1)</u> |
| | | 1 | 1 (TS4) | 1 | |
| | | | 2 (TS5) | 2 | |
| | | | 0 (TS3) | 3 | |
| | | | 1 (TS4) | | |
| <u>SFN'=2</u> | <u>(1st UL_{pos}=1)</u> | 0 | 0 (TS3) | 0 | <u>(1st UL_{pos}=2)</u> |
| | | 1 | 1 (TS4) | 1 | |
| | | | 2 (TS5) | 2 | |
| | | | 0 (TS3) | 3 | |
| | | | 1 (TS4) | | |
| | | | 2 (TS5) | | |
| . | . | . | . | . | . |
| . | . | . | . | . | . |
| . | . | . | . | . | . |

Annex D (Informative): Examples of the association of DL SS commands to UL uplink time slots

In the following two examples of the association of DL SS commands to UL uplink time slots are shown (see 6.2.2.3):

Table D.1 Two examples of the association of DL SS commands to UL uplink time slots with $N_{ULslot}=3$

Case 1: $N_{SSsymbols}=2$; Case 2: $N_{SSsymbols}=4$

| Sub-Frame Number | Case 1 (2 DL SS symbols) | | The order of the served UL time slot (UL time slot number) | Case 2 (4 DL SS symbols) | |
|------------------|--|---|--|-----------------------------|--|
| | The order of DL SS symbols | | | The order of DL SS symbols | |
| <u>SFN'=0</u> | <u>(1st UL_{pos}=0)</u> | 0 | 0 (TS3) 1 (TS4) 2 (TS5) 0 (TS3) | 0 | <u>(1st UL_{pos}=0)</u> |
| | | 1 | | 1 | |
| | | | | 2 | |
| | | | | 3 | |
| <u>SFN'=1</u> | <u>(1st UL_{pos}=2)</u> | 0 | 0 (TS3) 1 (TS4) 2 (TS5) 0 (TS3) 1 (TS4) | 0 | <u>(1st UL_{pos}=1)</u> |
| | | 1 | | 1 | |
| | | | | 2 | |
| | | | | 3 | |
| | | | | | |
| <u>SFN'=2</u> | <u>(1st UL_{pos}=1)</u> | 0 | 0 (TS3) 1 (TS4) 2 (TS5) 0 (TS3) 1 (TS4) 2 (TS5) | 0 | <u>(1st UL_{pos}=2)</u> |
| | | 1 | | 1 | |
| | | | | 2 | |
| | | | | 3 | |
| | | | | | |
| | | | | | |
| . | . | . | . | . | . |
| . | . | . | . | . | . |
| . | . | . | . | . | . |

8 Multiplexing and channel coding

8.1 Transport channel coding/multiplexing

8.1.1 Error detection

'Common with the high chip rate TDD mode'

8.1.2 Transport block concatenation and code block segmentation

'Common with the high chip rate TDD mode'

8.1.3 Channel coding

[Description:]

Usage of coding scheme and coding rate for the different types of TrCH is shown in table 1. In low chip rate TDD option, the coding scheme and coding rate of most type of TrCH are common with the high chip rate TDD.. Only BCH/PCH is a little different , it is mapped onto two code channels of the DL time slot. Rate 1/3 Convolutional coding is used for BCH and PCH.

[Rational:]

Usage of coding scheme and coding rate for the different types of TrCH is shown in table below. In low chip rate TDD option, BCH/PCH is mapped onto two physical channels of the DL time slot. If the usage of coding scheme and coding rate is 1/2 Convolutional coding, repeating as rate matching would be needed. So, it is used 1/3 Conv. coding as the coding scheme, this will lead to a better performance.

Table: Usage of channel coding scheme and coding rate

| Type of TrCH | Coding scheme | Coding rate |
|-----------------------|----------------------|-------------|
| BCH | Convolutional coding | 1/3 |
| PCH | | 1/3, 1/2 |
| RACH | | 1/2 |
| DCH, DSCH, FACH, USCH | Turbo coding | 1/3, 1/2 |
| | No coding | 1/3 |

| Type of TrCH | Coding scheme | Coding rate |
|-----------------------|----------------------|-------------|
| BCH, PCH | Convolutional coding | 1/3 |
| RACH | Convolutional coding | 1/2 |
| | | 1/3, 1/2 |
| DCH, DSCH, FACH, USCH | Turbo coding | 1/3 |
| | No coding | |

—The coding scheme and coding rate of other TrCH are common with high chip rate TDD and the following subclauses can be mentioned as “common with high rate TDD”:

8.1.3.1 Convolutional Coding

8.1.3.2 Turbo coding

8.1.3.2.1 Turbo coder

8.1.3.2.2 Trellis termination in turbo code

8.1.3.2.3 Turbo code internal interleaver

[Explanation difference:]

In high chip rate option, the coding scheme and coding rate of BCH/PCH is 1/2 Conv. coding. While in the low chip rate option, it is used 1/3 Conv. coding as the coding scheme and coding rate of BCH and PCH in low chip rate TDD option.

8.1.4 Radio frame size equalisation

'Common with the high chip rate TDD mode'

8.1.5 1st interleaving

'Common with the high chip rate TDD mode'

8.1.6 Radio frame segmentation

'Common with the high chip rate TDD mode'

8.1.7 Sub-frame segmentation

[Description:]

In the low chip rate option the radio frame which has a duration of 10 ms is subdivided into 2 subframes of 5ms each. The basic operated unit is a subframe. The bit streams in CCTrCH are mapped onto code channels of time slots in subframes. So, in low chip rate TDD option, it is needed to add the subframe segmentation unit between 2nd interleaving unit and physical channel mapping unit.

[Rational:]

In low chip rate option the radio frame which has a duration of 10 ms is subdivided into 2 subframes of 5ms each. The basic operated unit is a subframe. The bit streams in CCTrCH are mapped onto code channels of time slots in subframes. So, in low chip rate TDD option, it is needed to add subframe segmentation unit between 2nd interleaving unit and physical channel mapping unit. The operation of rate-matching guarantees that the bit streams is a even number and can be subdivided into 2 subframes. The transport channel multiplexing structure for uplink and downlink is shown in figure below.

The input bit sequence is denoted by $x_{i1}, x_{i2}, x_{i3}, \dots, x_{iX_i}$ where i is the TrCH number and X_i is the number bits. The two output bit sequences per radio frame are denoted by $y_{i,n_1}, y_{i,n_2}, y_{i,n_3}, \dots, y_{i,n_i}$ where n_i is the subframe number in current radio frame and Y_i is the number of bits per radio frame for TrCH i . The output sequences are defined as follows:

$$y_{i,n_k} = x_{i, \lfloor \frac{Y_i}{n_i} \rfloor + (n_i - 1) \cdot k}, \quad n_i = 1 \text{ or } 2, \quad k = 1 \dots Y_i$$

where

$Y_i = (X_i / 2)$ is the number of bits per subframe,

x_{ik} is the k^{th} bit of the input bit sequence and

$y_{i,n,k}$ is the k^{th} bit of the output bit sequence corresponding to the n^{th} subframe

The input bit sequence to the radio frame segmentation is denoted by $v_{(t)1}, v_{(t)2}, \dots, v_{(t)U_{(t)}}$, $x_{ik} = v_{(t)k}$ and $X_i = U_{(t)}$.

The output bit sequence corresponding subframe n_i is denoted by $g_{p1}, g_{p2}, \dots, g_{pU_p}$, where p is the PhCH number and U_p is the number of bits in one subframe for the respective PhCH. Hence, $g_{pk} = y_{i,n,k}$ and $U_p = Y_i$.

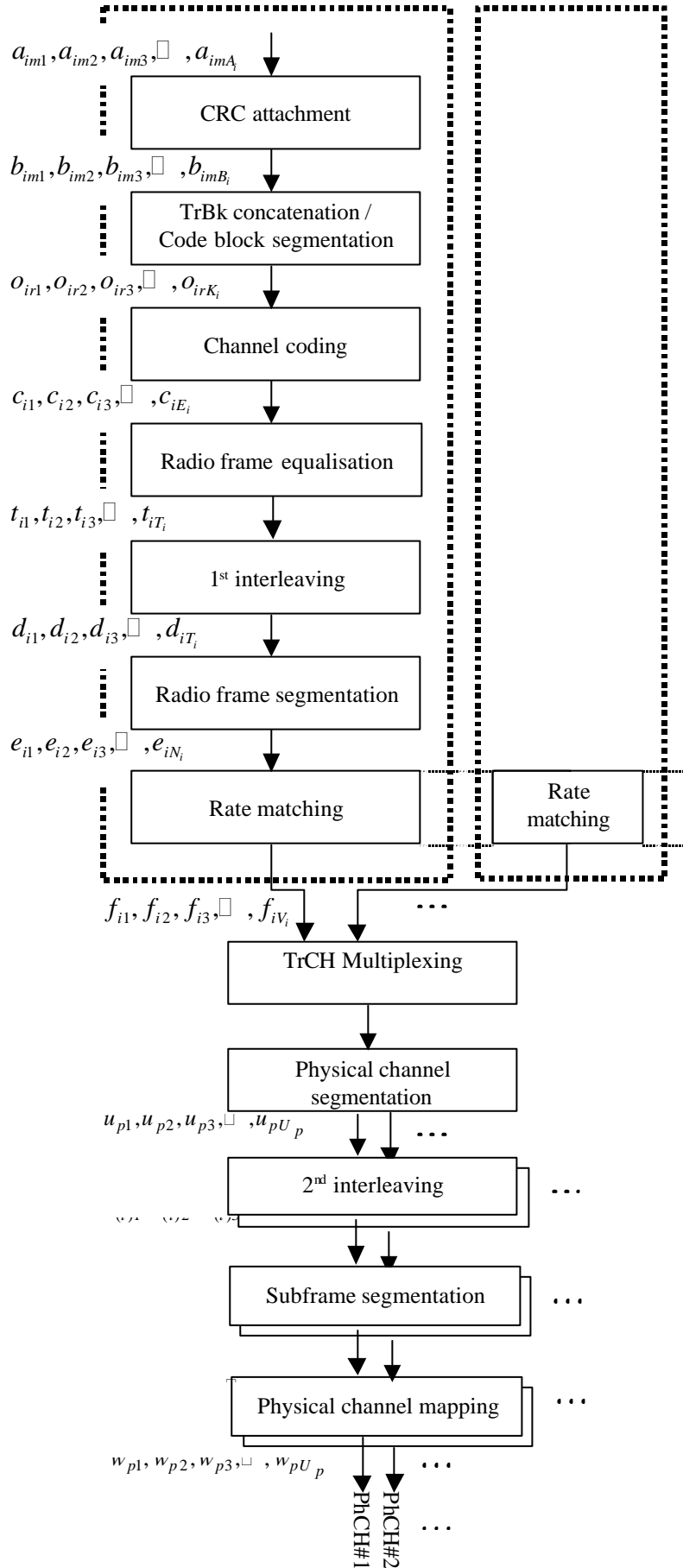


Figure : Transport channel multiplexing structure for uplink and downlink

[Explanation difference:]

In low chip rate option the radio frame which has a duration of 10 ms is subdivided into 2 subframes of 5ms each. The bit streams in CCTrCH are mapped onto code channels of time slots in subframes. So, in low chip rate TDD option, it is needed to add subframe segmentation unit between 2nd interleaving unit and physical channel mapping unit. While in high chip rate TDD option it is not included.

8.1.8 Rate matching

'Common with the high chip rate TDD mode'

8.1.9 TrCH multiplexing

'Common with the high chip rate TDD mode'

8.1.10 Physical channel segmentation

'Common with the high chip rate TDD mode'

8.1.11 2nd interleaving

'Common with the high chip rate TDD mode'

8.1.11.1 Frame related 2nd interleaving

8.1.11.2 Timeslot related 2nd interleaving

8.1.12 Physical channel mapping

[Description:]

In the low chip rate option the radio frame which has a duration of 10 ms is subdivided into 2 subframes of 5ms each. The basic operated unit is a subframe. So the bit streams from the subframe segmentation unit are mapped onto code channels of time slots in subframes in the low chip rate option.

[Rational:]

In the low chip rate option the radio frame which has a duration of 10 ms is subdivided into 2 subframes of 5ms each. The basic operated unit is a subframe. So the bit streams from the subframe segmentation unit are mapped onto code channels of time slots in subframes in the low chip rate option.

The PhCH for both uplink and downlink is defined in subclause 7.2. The bits after physical channel mapping are denoted by $w_{p1}, w_{p2}, \dots, w_{pU_p}$, where p is the PhCH number and U_p is the number of bits in one subframe for the respective PhCH. The bits w_{pk} are mapped to the PhCHs so that the bits for each PhCH are transmitted over the air in ascending order with respect to k .

The mapping of the bits $g_{p1}, g_{p2}, \dots, g_{pU_p}$ is performed like block interleaving, writing the bits into columns, but a PhCH with an odd number is filled in forward order, were as a PhCH with an even number is filled in reverse order.

The mapping scheme, as described in the following subclause, shall be applied individually for each timeslot t used in the current subframe. Therefore, the bits $g_{p1}, g_{p2}, \dots, g_{pU_p}$ are assigned to the bits of the physical channels $w_{t1,1...U_{t1}}, w_{t2,1...U_{t2}}, \dots, w_{tP,1...U_{tP}}$ in each timeslot.

In uplink there are at most two codes allocated (P?2). If there is only one code, the same mapping as for downlink is applied. Denote SF1 and SF2 the spreading factors used for code 1 and 2, respectively. For the number of consecutive bits to assign per code bs_k the following rule is applied:

if

SF1 >= SF2 then $bs_1 = 1$; $bs_2 = SF1/SF2$;

else

SF2 > SF1 then $bs_1 = SF2/SF1$; $bs_2 = 1$;

end if

In the downlink case bs_p is 1 for all physical channels.

8.1.12.1 Mapping scheme

Notation used in this subclause:

P_t : number of physical channels for timeslot t , $P_t = 1..2$ for uplink ; $P_t = 1...16$ for downlink

U_p : capacity in bits for the physical channel p in timeslot t

U_t : total number of bits to be assigned for timeslot t

bs_p : number of consecutive bits to assign per code

for downlink all $bs_p = 1$

for uplink if SF1 >= SF2 then $bs_1 = 1$; $bs_2 = SF1/SF2$;

if SF2 > SF1 then $bs_1 = SF2/SF1$; $bs_2 = 1$;

fb_p : number of already written bits for each code

pos: intermediate calculation variable

for p=1 to P_t -- reset number of already written bits for every physical channel

$fb_p = 0$

end for

p = 1 -- start with PhCH #1

for k=1 to U_t

do while ($fb_p == U_p$) -- physical channel filled up already ?

~~$p = ((p + 1) \bmod (P_t + 1)) + 1 - (p \bmod P_t) + 1$;~~

end do

if (p mod 2) == 0

pos = $U_p - fb_p$ -- reverse order

else

pos = $fb_p + 1$ -- forward order

endif

$W_{p,pos} = g_{t,k}$ -- assignment

$fb_p = fb_p + 1$ -- Increment number of already written bits

if $(fb_p \bmod bs_p) == 0$ -- Conditional change to the next physical channel

$p = \underline{(p \bmod P_i) + 1} + ((p + 1) \bmod (P_i + 1)) - 1$;

end if

end for

[Explanation difference:]

In the high chip rate TDD option, the bit streams from the 2nd interleaving unit are mapped onto code channels of timeslots in radio frames. While in the low chip rate option the radio frame which has a duration of 10 ms is subdivided into 2 subframes of 5ms each. The basic operated unit is a subframe. So the bit streams from the subframe segmentation unit are mapped onto code channels of time slots in subframes in the low chip rate option.

8.1.13 Multiplexing of different transport channels onto one CCTrCH, and mapping of one CCTrCH onto physical channels

'Common with the high chip rate TDD mode'

8.1.13.1 Allowed CCTrCH combinations for one UE

8.1.13.1.1 Allowed CCTrCH combinations on the uplink

8.1.13.1.2 Allowed CCTrCH combinations on the downlink

8.1.14 Transport format detection

'Common with the high chip rate TDD mode'

8.2 Coding for layer 1 control

8.2.1 Coding of transport format combination indicator (TFCI)

[Description:]

Encoding of the TFCI bits depends on the number of them and the mode of modulation applied. When the modulation of QPSK is deployed, encoding of the TFCI bits is the same as it in the high chip rate option. When the modulation of 8PSK is applied, the encoding of the TFCI bits is a little different from it in high chip rate option.

[Rationale:]

Encoding of the TFCI bits depends on the number of them and the mode of modulation applied. When the modulation of QPSK is deployed, encoding of the TFCI bits is the same as it in the high chip rate option. That is to say, if there are 6-10 bits of TFCI, the TFCI bits are encoded using a (32,10) sub-code of the second order Reed-Muller code. If the number of TFCI bits is in the range 3 to 5, the TFCI bits are encoded using a (16, 5) bi-orthogonal (or first order Reed-Muller) code. If the number of TFCI bits is 1 or 2, then repetition will be used for coding. In this case each bit is repeated to a total of 4 times giving 4-bit transmission ($N_{\text{TFCI}}=4$) for a single TFCI bit and 8-bit transmission ($N_{\text{TFCI}}=8$) for 2 TFCI bits. When 8PSK service is transmitted, the modulation of 8PSK is applied in low chip rate option. ~~In this case of 8PSK service, the odd bits of the encoded TFCI bits from the TFCI coder are repeated (e.g. the input is b0, b1, b2, b3, b4... the output will be b0, b1, b1, b2, b3, b3, b4...).~~ Thus the amount of encoded bits of TFCI in this case will be 48, 24, 12, 6 respectively for the 6-10, 3-5, 2, 1 TFCI bits. The same TFCI lengths like in WB-TDD are supported (0, 4, 8, 16, 32).

~~Other TFCI coding scheme for 8PSK is also considered.~~

8.2.1.1 Coding of transport format combination indicator (TFCI) for 8PSK

Encoding of TFCI bits depends on the number of them and the modulation in use. When 2 Mcps service is transmitted, 8PSK modulation is applied in 1.28 Mcps TDD option. The coding scheme for TFCI when the number of bits are 6 – 10, and less than 6 are described in section 4.4.2.1 and 4.4.2.2, respectively.

8.2.1.1.1 Coding of long TFCI lengths

When the number of TFCI bits are 6 – 10, the TFCI bits are encoded by using a (64,10) sub-code of the second order Reed-Muller code, then 16 bits out of 64 bits are punctured (Puncturing positions are 0, 4, 8, 13, 16, 20, 27, 31, 34, 38, 41, 44, 50, 54, 57, 61st bits). The coding procedure is shown in Figure [F1].

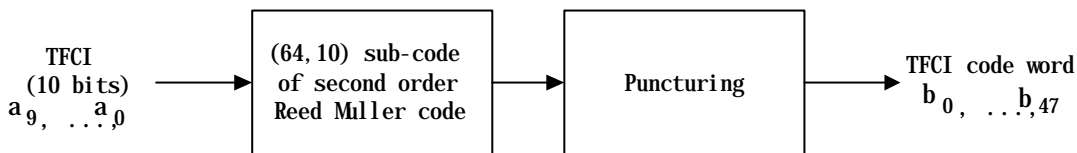


Figure [F1]: Channel coding of long TFCI bits for 8PSK

The code words of the punctured (48,10) sub-code of the second order Reed-Muller codes are linear combination of 10 basis sequences. The basis sequences are shown in Table [T1].

Table [T1]: Basis sequences for (48,10) TFCI code

| <u>l</u> | <u>M_{l,0}</u> | <u>M_{l,1}</u> | <u>M_{l,2}</u> | <u>M_{l,3}</u> | <u>M_{l,4}</u> | <u>M_{l,5}</u> | <u>M_{l,6}</u> | <u>M_{l,7}</u> | <u>M_{l,8}</u> | <u>M_{l,9}</u> |
|-----------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| <u>0</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> |
| <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>0</u> |
| <u>2</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> |
| <u>3</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> |
| <u>4</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> |
| <u>5</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> |
| <u>6</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> |
| <u>7</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> |
| <u>8</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> |
| <u>9</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>0</u> |
| <u>10</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> |
| <u>11</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> |
| <u>12</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> |
| <u>13</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> |
| <u>14</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> |
| <u>15</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> |
| <u>16</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>0</u> |
| <u>17</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> |
| <u>18</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> |
| <u>19</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> |
| <u>20</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> |
| <u>21</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> |
| <u>22</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> |
| <u>23</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> |
| <u>24</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> |
| <u>25</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> |
| <u>26</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> |
| <u>27</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> |
| <u>28</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> |
| <u>29</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> |
| <u>30</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> |
| <u>31</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> |
| <u>32</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> |
| <u>33</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> |
| <u>34</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> |
| <u>35</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> |
| <u>36</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> |
| <u>37</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> |
| <u>38</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> |
| <u>39</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>0</u> |
| <u>40</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>0</u> |
| <u>41</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> |
| <u>42</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> |
| <u>43</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> |
| <u>44</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> |
| <u>45</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> |
| <u>46</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> |
| <u>47</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>0</u> |

Let's define the TFCI bits as $a_0, a_1, a_2, a_3, a_4, a_5, a_6, a_7, a_8, a_9$, where a_0 is the LSB and a_9 is the MSB. The TFCI bits shall correspond to the TFC index (expressed in unsigned binary form) defined by the RRC layer to reference the TFC of the CCTrCH in the associated DPCH radio frame.

The output code word bits b_i are given by:

$$b_i = \sum_{n=0}^9 (a_n \cdot M_{i,n}) \text{ mod } 2$$

where $i=0 \dots 47$, $N_{\text{TFCI}}=48$.

8.2.1.1.2 Coding of short TFCI lengths

8.2.1.1.2.1 Coding very short TFCIs by repetition

When the number of TFCI bits is 1 or 2, then repetition will be used for the coding. In this case, each bit is repeated to a total of 6 times giving 6-bit transmission ($N_{\text{TFCI}} = 6$) for a single TFCI bit and 12-bit transmission ($N_{\text{TFCI}} = 12$) for 2 TFCI bits. For a single TFCI bit b_0 , the TFCI code word shall be $\{b_0, b_0, b_0, b_0, b_0, b_0\}$. For TFCI bits b_0 and b_1 , the TFCI code word shall be $\{b_0, b_1, b_0, b_1, b_0, b_1, b_0, b_1, b_0, b_1, b_0, b_1\}$.

8.2.1.1.2.2 Coding short TFCIs using bi-orthogonal codes

If the number of TFCI bits is in the range of 3 to 5, the TFCI bits are encoded using a (32,5) first order Reed-Muller code, then 8 bits out of 32 bits are punctured (Puncturing positions are 0, 1, 2, 3, 4, 5, 6, 7th bits). The coding procedure is shown in Figure [F2].

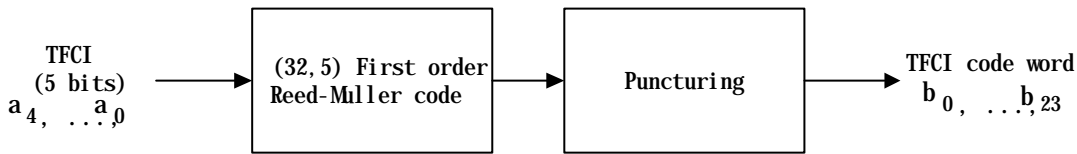


Figure [F2]: Channel coding of short TFCI bits for 8PSK

The code words of the punctured (32,5) first order Reed-Muller codes are linear combination of 5 basis sequences shown in Table [T2].

Table [T2]: Basis sequences for (24,5) TFCI code

| <u>l</u> | <u>M_{l,0}</u> | <u>M_{l,1}</u> | <u>M_{l,2}</u> | <u>M_{l,3}</u> | <u>M_{l,4}</u> |
|-----------|------------------------|------------------------|------------------------|------------------------|------------------------|
| <u>0</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>0</u> |
| <u>1</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>0</u> |
| <u>2</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> |
| <u>3</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> |
| <u>4</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>0</u> |
| <u>5</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>0</u> |
| <u>6</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> |
| <u>7</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> |
| <u>8</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>1</u> |
| <u>9</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>1</u> |
| <u>10</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> |
| <u>11</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> |
| <u>12</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> |
| <u>13</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> |
| <u>14</u> | <u>0</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> |
| <u>15</u> | <u>1</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> |
| <u>16</u> | <u>0</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> |
| <u>17</u> | <u>1</u> | <u>0</u> | <u>0</u> | <u>1</u> | <u>1</u> |
| <u>18</u> | <u>0</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> |
| <u>19</u> | <u>1</u> | <u>1</u> | <u>0</u> | <u>1</u> | <u>1</u> |

| | | | | | |
|----|---|---|---|---|---|
| 20 | 0 | 0 | 1 | 1 | 1 |
| 21 | 1 | 0 | 1 | 1 | 1 |
| 22 | 0 | 1 | 1 | 1 | 1 |
| 23 | 1 | 1 | 1 | 1 | 1 |

Let's define the TFCI bits as a_0, a_1, a_2, a_3, a_4 , where a_0 is the LSB and a_4 is the MSB. The TFCI bits shall correspond to the TFC index (expressed in unsigned binary form) defined by the RRC layer to reference the TFC of the CCTrCH in the associated DPCH radio frame.

The output code word bits b_i are given by:

$$b_i = \sum_{n=0}^4 (a_n \cdot M_{i,n}) \text{ mod } 2$$

where $i=0 \dots 23$, $N_{\text{TFCI}}=24$.

8.2.1.1.3 Mapping of TFCI code word

Denote the number of bits in the TFCI code word by N_{TFCI} , and denote the TFCI code word bits by b_k , where $k=0, \dots, N_{\text{TFCI}}-1$.

When the number of bits in the TFCI code word is 12, 24, or 48, the mapping of the TFCI code word to the TFCI bit positions in a time slot shall be as follows.

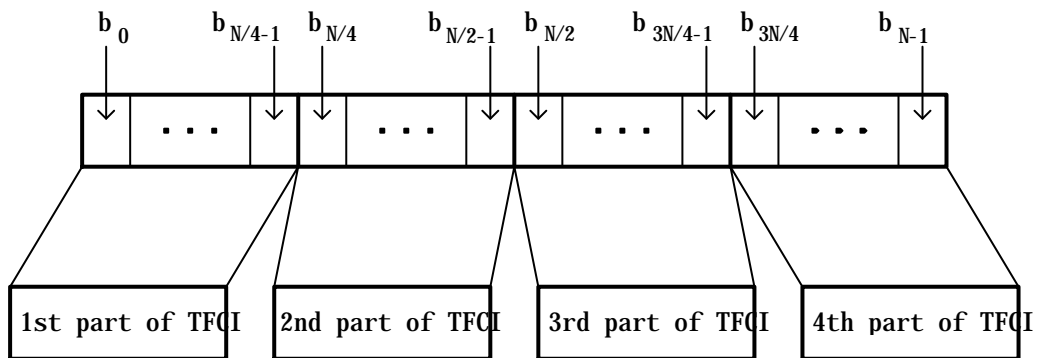


Figure [F3]: Mapping of TFCI code word bits to timeslot in 1.28 Mcps TDD option, where $N = N_{\text{TFCI}}$.

When the number of bits in the TFCI code word is 6, the TFCI code word is equally divided into two parts for the consecutive two sub-frames and mapped onto the first data field in each of the consecutive sub-frames. The mapping of the TFCI code word to the TFCI bit positions in a time slot shall be as shown in figure [F4].

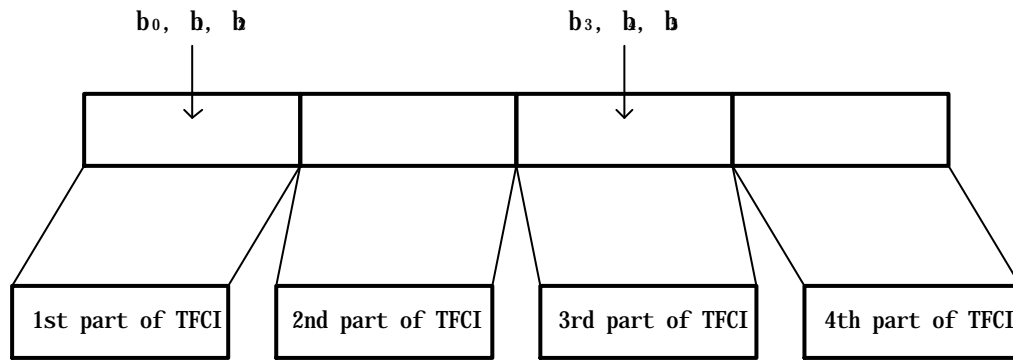


Figure [F4]: Mapping of TFCI code word bits to timeslot in 1.28 Mcps TDD option when $N_{\text{TFCI}} = 6$.

The location of the 1st to 4th parts of TFCI in the timeslot is defined in [7].

[Explanation difference:]

In high chip rate option, encoding of the TFCI bits depends on the number of them. 1-10 bits of TFCI are supported. Thus, the amount of encoded bits of TFCI is 32, 16, 8, 4 respectively for the 6-10, 3-5, 2, 1 TFCI bits.

In the low chip rate option, encoding of the TFCI bits depends on the ~~number of them and the mode of modulation applied~~ applied mode of modulation. ~~When the modulation of QPSK is deployed~~ applied, encoding of the TFCI bits is the same as it in the high chip rate option. ~~In this case of 8PSK service, the odd bits of the encoded TFCI bits from the TFCI coder are repeated, thus the amount of encoded bits of TFCI in this case will be 48, 24, 12, 6 respectively for the 6-10, 3-5, 2, 1 of TFCI bits. The repetition of TFCI odd bits is necessary to guarantee the same number of symbols.~~

~~Note: Details of the TFCI coding with 8PSK are for further study and proposals are under consideration.~~

8.2.2 Coding of Synchronisation Shift

[Description:]

The SS command, one kind of L1 control signals, is an identifier sent in downlink, to instruct a timing adjustment each M frames. The length of the SS command is 1 symbol.

[Rational:]

The SS command is sent in every sub-frame (in case allocated). The command may be updated only after every M sub-frames. I. The coding of the SS command is shown in table below. M (1-8) and k (1-8) can be adjusted during call setup or readjusted during the call by higher layer.

Table: Coding of the SS

| <u>SS</u> | <u>SS Bits</u> | <u>Meaning</u> |
|---------------------|----------------|---|
| <u>'Down'</u> | <u>00</u> | <u>Decrease synchronisation shift by k/8 Tc</u> |
| <u>'Up'</u> | <u>11</u> | <u>Increase synchronisation shift by k/8 Tc</u> |
| <u>'Do nothing'</u> | <u>01</u> | <u>No change</u> |

| <u>SS-Bits</u> | <u>Meaning</u> |
|----------------|--|
| <u>11</u> | <u>Increase timing advance by k/8 Tc</u> |
| <u>00</u> | <u>Decrease timing advance by k/8 Tc</u> |

~~* Note: other methods like e.g. definition of 'do nothing' are under consideration~~

In case of 8PSK service, the numbers of the SS bits is 3. The specific coding of SS for the case of 8PSK ~~service~~ is shown in table below.

Table : Coding of the SS (special for in case of 8PSK)

| <u>SS</u> | <u>SS Bits</u> | <u>Meaning</u> |
|--------------|----------------|---|
| 'Down' | 000 | Decrease synchronisation shift by $k/8 T_c$ |
| 'Up' | 110 | Increase synchronisation shift by $k/8 T_c$ |
| 'Do nothing' | 011 | No change |

| <u>SS Bits</u> | <u>Meaning</u> |
|----------------|-----------------------------------|
| 111 | Increase timing advance $k/8 T_c$ |
| 001 | Decrease timing advance $k/8 T_c$ |

* Note: other methods like e.g. definition of 'do-nothing' are under consideration

[Explanation difference:]

In high chip rate TDD option, SS information is not transmitted as L1 signal on each frame. Because of uplink synchronisation in the low chip rate TDD option, SS information is transmitted, as one of L1 signals, once per 5ms subframe.

The SS command is an identifier sent in downlink, to instruct a timing adjustment each M frames. The length of the SS command is 1 symbol. ~~There are the three possibilities: "up", "down" or "do nothing". The SS bits "11" mean increasing timing advance $k/8 T_c$ and "00" mean decreasing the timing advance by $k/8 T_c$. The modulation of 8PSK is applied, e.g. in case of 2Mbps service. In this case, the numbers of the SS bits is 3. The specific coding of SS for the case of 8PSK service is shown in table above.~~

8.2.3 Coding of Transmit Power Control (TPC)

[Description:]

The TPC command, one kind of L1 control signals, is an identifier sent both in up- and downlink, to instruct a power level adjustment which is increase or decrease. The coding of the TPC command is shown.

[Rationale:]

The TPC command is an identifier sent both in up- and downlink, to instruct a power level adjustment which is increase or decrease. The length of the TPC command is one symbol. The coding of the TPC command is shown in table 1.

Table: Coding of the TPC

| TPC | TPC Bits | Meaning |
|--------|----------|-------------------|
| 'Up' | 11 | Increase Tx Power |
| 'Down' | 00 | Decrease Tx Power |

* Note: other methods like e.g. definition of 'do-nothing' are under consideration

When 8PSK modulation is applied, the length of the coded TPC command remains one symbol and therefore the number of TPC Bits is 3. The specific coding of TPC for the case of ~~2Mbps 8PSK service~~ is shown in table 2.

Table: Coding of the TPC (Special for 8PSK)

| TPC | TPC Bits | Meaning |
|-----|----------|---------|
|-----|----------|---------|

| | | |
|--------|--------|-------------------|
| 'Up' | 111110 | Increase TX power |
| 'Down' | 001000 | Decrease TX power |

* ~~Note1: other methods like e.g. definition of 'do nothing' is under consideration~~

* ~~Note2~~Note1: the TPC coding for 8PSK refer to 9.1.2

[Explanation difference:]

In high chip rate option, the TPC command is sent in uplink transmission only, to instruct the NodeB whether Tx power has to be increased or decreased. The length of the TPC command is one symbol.

In the low chip rate option, the TPC command is an identifier sent both in up- and downlink, to instruct a power level adjustment which is increase or decrease. When 8PSK modulation is applied the length of the coded TPC command remains one symbol and therefore the number of TPC Bits is 3. The specific coding of TPC for the case of 8PSK is shown in table above. ~~Other methods like e.g. to define the command of 'do nothing' is under consideration.~~

8.2.4 Coding of the Paging Indicator

Common with the high chip rate TDD option

9 Spreading and Modulation

9.1 Data modulation

[Description:]

This document is described the difference of modulation and spreading in low chip rate TDD. The main difference is the mapping of bits onto signal point constellation, synchronization codes and code Allocation.

[Rational:]

9.1.2 Mapping of bits onto signal point constellation

9.1.2.1 QPSK modulation

'Common with high chip rate TDD'

9.1.2.2 8PSK modulation

The data modulation is performed to the bits from the output of the physical channel mapping procedure for 8PSK service 3 consecutive binary bits to a complex valued data symbol. Each user burst has two data carrying parts, termed data blocks:

$$\underline{d}^{(k,i)} = (d_1^{(k,i)}, d_2^{(k,i)}, \dots, d_{N_k}^{(k,i)})^T \quad i = 1, 2; k = 1, \dots, K. \quad (14)$$

N_k is the number of symbols per data field for the user k . This number is linked to the spreading factor Q_k .

Data block $\underline{d}^{(k,1)}$ is transmitted before the midamble and data block $\underline{d}^{(k,2)}$ after the midamble. Each of the N_k data symbols $d_n^{(k,i)}$; $i = 1, 2; k = 1, \dots, K; n = 1, \dots, N_k$ of equation 1 has the symbol duration $T_s^{(k)} = Q_k T_c$ as already given.

The data modulation is 8PSK, thus the data symbols $d_n^{(k,i)}$ are generated from 3 consecutive data bits from the output of the physical channel mapping procedure:

using the following mapping to complex symbols:

| Consecutive binary bit pattern | complex symbol |
|---|--|
| $b_{1,n}^{(k,i)} b_{2,n}^{(k,i)} b_{3,n}^{(k,i)}$ | $d_n^{(k,i)}$ |
| 000 | $\text{Cos}(11\pi/8) + j\sin(11\pi/8)$ |
| 001 | $\text{Cos}(9\pi/8) + j\sin(9\pi/8)$ |
| 010 | $\text{Cos}(5\pi/8) + j\sin(5\pi/8)$ |
| 011 | $\text{Cos}(7\pi/8) + j\sin(7\pi/8)j$ |
| 100 | $\text{Cos}(13\pi/8) + j\sin(13\pi/8)$ |
| 101 | $\text{Cos}(15\pi/8) + j\sin(15\pi/8)$ |
| 110 | $\text{Cos}(3\pi/8) + j\sin(3\pi/8)$ |
| 111 | $\text{Cos}(\pi/8) + j\sin(\pi/8)$ |

The mapping corresponds to a 8PSK modulation of the interleaved and encoded data bits $b_{l,n}^{(k,i)}$ of the table above and $d_n^{(k,i)}$ of equation 14.

~~The use of shifted 8PSK is under consideration.~~

9.1.3 Symbol rate

'Common with the high chip rate TDD mode'

9.2 Spreading modulation

9.2.1 Basic spreading parameters

'Common with the high chip rate TDD mode'

9.2.2 Spreading codes

'Common with the high chip rate TDD mode'

9.2.3 Scrambling codes

'Common with the high chip rate TDD mode'

9.2.4 Spread and scrambled signal of data symbols and data blocks

'Common with the high chip rate TDD mode'

9.3 Synchronisation codes

DwPTS code

The DwPTS is composed of 64 chips (4 symbols) of SYNC-DL and 32 chips (2 symbols) of guard period as shown in Figure below. SYNC-DL code is not scrambled. There should be 32 different basic SYNC-DL codes for the whole system.

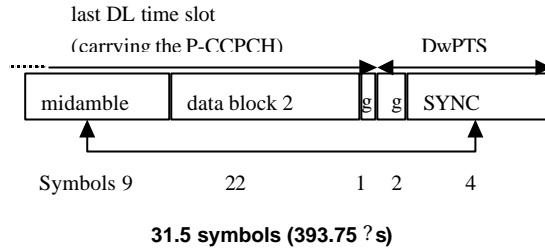


Figure : The frame structure around DwPTS

The phase of the whole DwPTS is used to signal the P-CCPCH multi-frame. As QPSK is used for the modulation of the DwPTS, the phases 45, 135, 225, 315° is used to signal. Indication of starting point of the phase quadruple and the position of the BCH is realised by means of direct signalling. In this method the phase of 45° is reserved for the beginning of each phase quadruple. For the other sub-frames of the phase quadruple, the phase 135°, 225° and 315° are used only to detect the position of the BCH as shown Table 1.

The sequence of the phases is chosen, that the position of the BCH can also be detected by using differential demodulation of the consecutive phases of the DwPTS.

Table Sequence for the phase modulation for the DwPTS

| Phase quadruple | # 225 | (SFN/2) mod 8 |
|-------------------|-------|----------------------------|
| 45, 225, 225, 225 | 3 | 0 (the BCH should be here) |
| 45, 135, 135, 225 | 4 | 1 |
| 45, 135, 225, 135 | 4 | 2 |
| 45, 315, 225, 315 | 4 | 3 |
| 45, 225, 135, 315 | 4 | 4 |
| 45, 225, 315, 315 | 4 | 5 |
| 45, 225, 225, 135 | 2 | 6 |
| 45, 225, 225, 315 | 2 | 7 |
| | | |
| | | |
| | | |
| | | |
| Others | - | Error |

For the generation of the complex valued SYNC-DL codes of length 64, the basic binary SYNC-DL codes

s_1, s_2, \dots, s_{64} of length 64 shown in Table A are used. The relation between the elements s_i and s_j is given by:

$$s_j = (j - i) \cdot s_i \quad s_i = \pm 1, \pm j \quad i = 1, \dots, 64 \quad (1)$$

Hence, the elements s_i of the complex SYNC-DL code S are alternating real and imaginary.

The SYNC-DL is QPSK modulated and the phase of the SYNC-DL is used to signal the presence of the P-CCPCH in the multi-frame of the resource units of code $c_{Q^{216}}^{(k,1)}$ and $c_{Q^{216}}^{(k,2)}$ in time slot #0.

The SYNC-DL sequences are modulated with respect to the midamble ($m^{(1)}$) in time slot #0.

Four consecutive phases (phase quadruple) of the SYNC-DL are used to indicate the presence of the P-CCPCH in the following 4 sub-frames. In case the presence of a P-CCPCH is indicated, the next following sub-frame is the first sub-frame of the interleaving period. As QPSK is used for the modulation of the SYNC-DL, the phases 45, 135, 225, and 315° are used.

The total number of different phase quadruples is 2 (S1 and S2). A quadruple always starts with an even system frame number ((SFN mod 2) = 0). Table X is showing the quadruples and their meaning.

Table X Sequences for the phase modulation for the SYNC-DL

| Name | Phase quadruple | Meaning |
|------|-------------------|--|
| S1 | 135, 45, 225, 135 | There is a P-CCPCH in the next 4 sub-frames |
| S2 | 315, 225, 315, 45 | There is no P-CCPCH in the next 4 sub-frames |

There should be 32 different SYNC codes (see Table A) for the whole system. That the $(SFN/2) \bmod 8 = 0$ is always used for BCH. Other position can also be configured to transmit the BCH.

9.3.1 UpPTS code

Synchronisation sequences for the UpPTS (SYNC1 SYNC-UL)

SYNC1 SYNC-UL code is not scrambled.

The time slot is composed of 128chips of SYNC1 SYNC-UL and 32chips of GP as shown in Figure 2.

There should be 256 different SYNC1 SYNC-UL codes (see Table B) for the whole system.

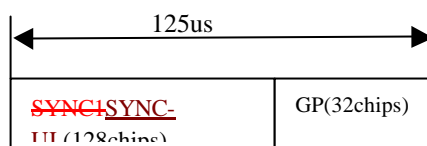


Figure Burst structure of UpPTS

The possible restriction to the network planning from parameter grouping is to be verified.

9.3.2 Code Allocation

Relationship between the SYNC-DL and SYNC-UL sequences, the scrambling codes and the midamble codes

| Code Group | Associated Codes | | | |
|------------|------------------|------------------------------|--------------------------------------|--|
| | SYNC-DL ID | SYNC-UL ID (coding criteria) | Scrambling Code ID (coding criteria) | Basic Midamble Code ID (coding criteria) |
| Group 1 | 0 | 0~7 (000~111) | 0 (00) | 0 (00) |
| | | | 1 (01) | 1 (01) |
| | | | 2 (10) | 2 (10) |
| | | | 3 (11) | 3 (11) |
| Group 2 | 1 | 8~15 (000~111) | 4 (00) | 4 (00) |
| | | | 5 (01) | 5 (01) |
| | | | 6 (10) | 6 (10) |
| | | | 7 (11) | 7 (11) |
| Group 32 | 31 | 248~255 (000~111) | 124 (00) | 124 (00) |
| | | | 125 (01) | 125 (01) |
| | | | 126 (10) | 126 (10) |
| | | | 127 (11) | 127 (11) |

Table A

Basic SYNC-DL Codes

| Code ID | SYNC-DL Codes of length 64 |
|---------|----------------------------|
| 0 | B3A7CC05A98688E4 |
| 1 | 9D559BD290606791 |
| 2 | 2CE7BA12A017C3A2 |
| 3 | 34511D20672F4712 |

| | |
|----|------------------|
| 4 | 9A772841474603F2 |
| 5 | 9109B1A5CE01F228 |
| 6 | 8FD429B3594501C0 |
| 7 | 25251354AA3F8C19 |
| 8 | C9A3B8E0C043EA56 |
| 9 | BA04B888E5BC1802 |
| 10 | A735354299370207 |
| 11 | 74C3C8DA4415AE51 |
| 12 | F4FD0458A0124663 |
| 13 | A011D4E16C3D6064 |
| 14 | BDA0661B0CAA8C68 |
| 15 | 8E31123F28928698 |
| 16 | F095C1632E2906AB |
| 17 | B60B4A8A664071CF |
| 18 | AA094DCCE91E041A |
| 19 | C0C31CDA8A256807 |
| 20 | D516964FB18C1890 |
| 21 | 30DE01834F4AACCE |
| 22 | 8F700323BA5CAD34 |
| 23 | 1B50F4DEE0C1380C |
| 24 | 443382164F56F2D1 |
| 25 | E1E4005D49B846B4 |
| 26 | 040A97165330BFAA |
| 27 | C48E26881693AD78 |
| 28 | D4354B2FE02361CC |
| 29 | 5383AB6C8A10CE84 |
| 30 | D417A730F2F12244 |
| 31 | ABF0A0D905A939C4 |

Table B

Basic SYNC1 SYNC-UL Codes

| Code ID | SYNC-UL SYNC-UL Codes of length 128 |
|---------|--|
| 0 | C11C20F0D1807DB8859175B798EC094A |
| 1 | 91278068081EC8E74543DBC1C9AD4235 |
| 2 | 38F5AEE2E513DB12A663BA04160103E5 |
| 3 | 7AA8A0A210F12A1E4332F2EDD33011FC |
| 4 | C180EA3B9BA1774EB9611BD249C4A508 |
| 5 | B072A2C839489D496B98CE9D0132FBC9 |
| 6 | B2723EAC6EB01667F2B33961C8074234 |
| 7 | C4144AD060F0EC095E227B92CF7C8280 |
| 8 | 653036A10D3054146FCF815986C63A14 |
| 9 | F899CA61435D64DC07FDF04C4A0C053A |
| 10 | B56F2D6893A8051407F4C341D88DC7DC |
| 11 | DC0BE838242142EDE6413A72C88D74AA |
| 12 | 22A2FD86E4086C70A4860B13C76E579F |
| 13 | A3CBC21322C97D2A02728E7875F39588 |
| 14 | D4EC4F694A082CB38E3B1558A0FCC89F |
| 15 | CC891141C4E216D235C15CF5D3F9B002 |
| 16 | A1993114C50B77CB0C0725D1E22FD016 |
| 17 | 24F73A979DE52F82E8800CCB93842A59 |
| 18 | 8F878FA04659842E294D8DEAB20BA2FD |
| 19 | AC90B0442D70662B028CF76A6BECDF09 |
| 20 | D94A284DF64D7B0102F0E084C29C88C8 |
| 21 | 8603200C7596F24E865FD3815693358D |
| 22 | B466B12CF433642BD8B08F1F452E0550 |
| 23 | 86A3A1772C1C99FCA7DBBA0C312E34A0 |
| 24 | 622A1889F72A9A2C042D46F08EFEE1AC |
| 25 | BF220A362BC0D3B0D7CE400954C6CFAE |
| 26 | D28D73C52E89CF57905C502244F63616 |
| 27 | AD4E1C2103697D64D8B9D4C035D90548 |
| 28 | 8F081A9BA12B6C6BD024531AA984D21C |
| 29 | E4092429BE82988E1E3585BF6A6AE550 |
| 30 | 08BD36E0A9C061782CB38B35B335CA56 |

| | |
|----|-----------------------------------|
| 31 | 1CDFF3CC2685D1C44F4A1059AB03F40A |
| 32 | 506ED4E88FB1CECE3243F2A27A0221A4 |
| 33 | 846CF58A7AB613C83A24130B5778C0E2 |
| 34 | A2711A99E26A0C75AC026F4CFAECE893 |
| 35 | D846EEEEBA2432AC05A01043C62579DCF |
| 36 | 6B16B4E851CAF2121FC4CF88820C89E7 |
| 37 | AA4889A78207674A74E10C6F2BE11D48 |
| 38 | 8534CF8145BC991052814ED5C72709EE |
| 39 | 01AEF15D2290A84A607425746D9963C7 |
| 40 | 999188F758245D5164FE16D852942C71 |
| 41 | CF71C008599287E446E30745BD56E2D2 |
| 42 | 248414BA0DF8CDC4711FE7C8707ED0AD |
| 43 | EB2E263EC016191C81AB714BFE4D2B30 |
| 44 | 862082A7482FAC1C499793A0D8CED670 |
| 45 | DE2C22B2783AB75A7342608DE413840A |
| 46 | E31AA60B727F2CA2A78DAAC10665011D |
| 47 | CEF6CD06509870AC9E0177ACD550921D |
| 48 | E52C84D499FFCDC287581691471540F2 |
| 49 | B33BF6551A4322504BEE0930BCA1EC68 |
| 50 | 555BE6886D0FC43D72315E6C6D384148 |
| 51 | 8444F67451EE23CE1240C90F0B52A492 |
| 52 | 5C290D28E84060E69D09788A261B10FF |
| 53 | 337E0C35E83CD38CCC5D45804241F952 |
| 54 | A7879F0D31A8982A01EE6AC4952984DC |
| 55 | A37F506508928C70A83D69A2373781B9 |
| 56 | 42F55208EE12909803A7CBEB19B5419E |
| 57 | 57E5E268A328FCC9ED04B9E5420AC702 |
| 58 | EB033AD1222F84D8642C4E3FAAD28206 |
| 59 | 98EE1415F026AC0E862C520451697DD0 |
| 60 | 6A0528AEA4B7CD6702660D81F8821E19 |
| 61 | 763D626A87C603BCB09E1A4C800A378F |
| 62 | EEA61897879289340C23F669D6A03762 |

| | |
|----|----------------------------------|
| 63 | A6571B3CC2D0E04F017ACC808B92DCE7 |
| 64 | DDF88B52EA1831D293A803CF23C8C471 |
| 65 | 6CA4D333A2684140475DAB491F61C17A |
| 66 | A7D2AD23043989A13289F7C3E135580A |
| 67 | B1C752FA66B41C81904EDE27EA000E2E |
| 68 | 8694BE3CC1CB36BE2A095F89CC619080 |
| 69 | 9C20334E1BBC596B25E151180BF99940 |
| 70 | 484256214F81070DD9C49A2B05A43DCE |
| 71 | 401A20BCBE29B7438A7AEE44635A9E23 |
| 72 | 8858585C3239CBF628033FA0DF189378 |
| 73 | EFA36404C1BA5118CC5F9052FD28D9C3 |
| 74 | 155609873D8A042D496E6477B747C4F8 |
| 75 | 8446077883A6D7D2549CC9742E3FD023 |
| 76 | E630142B189AA209371A6F0FFDBC30A7 |
| 77 | C46060535AC6DBB2095F1D7826D0CD5C |
| 78 | E00D19E48797148B28DEDA9D429362E2 |
| 79 | 645DE447E938485489416CAFCC1C571F |
| 80 | DA10AFBF2AE61C593A1D88584DE30598 |
| 81 | BB248AEA5FD3FE210CD48FC401E1A686 |
| 82 | A89F146BD9191F445301C081CB6F5625 |
| 83 | 15BBF04F247C59150208949EB6B9CC58 |
| 84 | 08F48BFA7804B5B2CC2E96510232E062 |
| 85 | 9AA2BE74005A3679C626B209580B8D03 |
| 86 | 9D40664A2C808F2F293E255398B37E6A |
| 87 | 6869C98A8AAD81CAE41A23C83FF9EEA0 |
| 88 | 576E8948E61BD0927C4140C3C04C4CF3 |
| 89 | 0F942C67A1137B6EAA058C2A74872C73 |
| 90 | 9D058E27ED546C10632684BBC84E5BC1 |
| 91 | 79D4B840E20148B134F90B51164BCBD0 |
| 92 | 0E35E1D8D1214C05FAC790B69B239150 |
| 93 | FFA1BB0232CD71480BE5CA1C2A269F89 |
| 94 | B2956F5F4E270446F9211584792628DB |

| | |
|-----|----------------------------------|
| 95 | F56CCA23421C8EC8F8A41F7DA4A41EA2 |
| 96 | 0B5ECA04F1789A7148C80C39D57D05F6 |
| 97 | A10B538E8A8CFC8F8925C485F2A88660 |
| 98 | 9925C2C715001D9FC78ACCC51DA1AF34 |
| 99 | 0DAC9CFDEA40429A8B12C7D320D60F70 |
| 100 | 377FC9A097017958440914E83118E39D |
| 101 | 8421096FA8B47E4E943B6473671955CC |
| 102 | 574086183477C4F68540CB7E858263B1 |
| 103 | 895B6A8980C6703C779F49F40C5CFC19 |
| 104 | D0D253E157BC19262150CEA668679E71 |
| 105 | B8889C60EBA812BD7F0B6498823296D2 |
| 106 | A13FB9F3A08528E44B13C12CF0D461AA |
| 107 | 8D4DCFBE43D6E2024B1F8470224AA330 |
| 108 | 536D159E119E0893838657B12A074E64 |
| 109 | DCFD49C504AD3A2F049A0CB70238EC8A |
| 110 | D363DB4C46C11757FA8FB18139789102 |
| 111 | 424A1E8A1D4DA256E4CA3BC8C2201BE3 |
| 112 | 417B619ED30FEB0A847CC3A191A20398 |
| 113 | 843FBBC95453C61786D1332612B45B4D |
| 114 | F26CACC0732CF8ED0C5BC1462B1620B4 |
| 115 | 88E0FE440C70E9249A92A7AF94638880 |
| 116 | 99A52B7D8C950308057E0661D7459960 |
| 117 | A5C28218BF5D16E63E42698A0A6B0896 |
| 118 | B2763BEEC784A12E8C50778536921806 |
| 119 | 987B2B6A3A77A059B30A082457AB84E0 |
| 120 | 820DB500F1B206358D7A7F210AB85AA8 |
| 121 | 97760A5CFC5E03EB439C914590045938 |
| 122 | 896A720E8857C8708A59F8C94DE0841E |
| 123 | 2D101F0CF95263843412577340DEBB11 |
| 124 | E8E5214B4DCF5D11A245B0149D49C87C |
| 125 | 51224EAA10099ACDE384834A5ADF03D8 |
| 126 | 64E51253554A230C186FDE4E8781BC09 |

| | |
|-----|----------------------------------|
| 127 | A499E391E69ED08890AC1A82A6115BEC |
| 128 | EE54C6E1834210D3EC1B07A456B92AA8 |
| 129 | 949DB5CA82420B54C1E0BCC111E704D9 |
| 130 | 9439EE9A9E4C447D1AA350926495047F |
| 131 | AD095CC0E7438AECE38D60980B3F2D00 |
| 132 | 83089C254C5EE9788072BC3D9282F798 |
| 133 | A27DC1A457BC5A56563D8A9B11203615 |
| 134 | 713053A9C0B1B08B14705FF5A7244DB4 |
| 135 | D36D4B9F4007354E0EC1B0CA8C8C7124 |
| 136 | 82E7C990612114F1CCE1BD9509FD4386 |
| 137 | C8D83FF0B48B14830D2015D53F8C0672 |
| 138 | 08AF223C869A36B169148FDDABB7D120 |
| 139 | B6C284C600AD0A99F86C449F8F4C53A6 |
| 140 | DC741B320C07682AF92AC4DBDE0C28C2 |
| 141 | 89B8D84FA902265850C0FA6FF0EB2C4F |
| 142 | A69445B3A52201DB984BC03D1956D7F3 |
| 143 | 0FE0F7224B7AD72E4D4530D0223F590C |
| 144 | 1B8C06F051434048EB925133AD3BD3F9 |
| 145 | E133D4C3C942726A351300C37E55D0DF |
| 146 | 9E09481D1881A66F562D8B453BC83AB2 |
| 147 | 2397B04B60A3C5700907BDBBA4E818C8 |
| 148 | 8F81F7A08CC6C8DA3D692AD34F50C012 |
| 149 | 9AB325352981BCCFA072F8FDE3009221 |
| 150 | 4FA88B7F1F8A620C31B0D486C52AC2F6 |
| 151 | 097AF0ADD16D7D39851049F0130EE444 |
| 152 | A5027732DACFF11C388D5820A4A9BA49 |
| 153 | 1CD981EA2EDB46218A407C7E20D4BE84 |
| 154 | D0FD94279FA67EC61A3904C0AD8ACA04 |
| 155 | EA73A9415EC2004D49E9D0F645961C75 |
| 156 | 005AF0614A7552041194DEECBF8DD016 |
| 157 | B514481533DA0A731705B93CF634E40D |
| 158 | 983054521841A6E4FF34B2C07B5684FE |

| | |
|-----|----------------------------------|
| 159 | C46D927D0FD2B2F509550025677C6871 |
| 160 | 2AD85C08127487C87ECE014D65169102 |
| 161 | 0F617852FA3930AA7EE74B400B2CC831 |
| 162 | AE9D395004C6E27540C378625D36E0D6 |
| 163 | DC4FA55750F10B0636248F12C212FFE4 |
| 164 | D3602B8D6CBF1809C88B827185631ECF |
| 165 | A94825850708E7723EA8F22C44BF78B2 |
| 166 | A62D231C16AEEFE0B0026B306662945A |
| 167 | 9C7BE810A86465A50551F89125D93B12 |
| 168 | 9712D9338B9CC60485C10172F50F121F |
| 169 | A3902CE0E0B9912591FF28C695728257 |
| 170 | 4167057891AB29473A9E0F67F3658921 |
| 171 | B3368B91EC12A284BC414C8F0D7F8D20 |
| 172 | EE21888101ABF06C1175828CB58B598D |
| 173 | E43923A00ECC32CCC2D162A4A44BD7F4 |
| 174 | CC9E30B8538AD51703EEB6F70801AB22 |
| 175 | B908AD2F1501DA1C156811736CD798CD |
| 176 | 2B46302ACCC2F808797FC648A614326D |
| 177 | 8A54494F1BE27235B8764023AA0FBCFA |
| 178 | BC1041E6F636421E89277DC154439103 |
| 179 | 275B39A63029B974E3561AE0A8FC8032 |
| 180 | 9283F6FE819B80492A22B85CE5CE5DC4 |
| 181 | 4CCB52C0CE058A78022C22DF5788CBCC |
| 182 | B0DF9608DE549A6F6C581516919A81E6 |
| 183 | 2CA185163CC36060D1E85BB0A7FBB988 |
| 184 | 66101D2846155CAC986FC790D2124EFC |
| 185 | 8016E3904644D2093579B83BD7AB5071 |
| 186 | 531CAB7085BEC14257439658023647CF |
| 187 | DF2910165AA5051E41F6EB198E4D491C |
| 188 | BA32052042B0FB2188DE7857DA1B6788 |
| 189 | 9E6D075AFF0EA4153615E140BF380666 |
| 190 | 9ACC5A037902534642A3BE391AA40F9B |

| | |
|-----|----------------------------------|
| 191 | 4D741A3B4499843010D7E5FA8988DC80 |
| 192 | FA1421C96EDC6092726154560B1C2FC8 |
| 193 | 882946076223CAE0B0BFE3EDA59826D5 |
| 194 | CEBB288C28B7472A0D3917012276C034 |
| 195 | BD35A6E00C9528DB38289CF823C34F30 |
| 196 | E2C93618B6B2800D51171A5F85746A55 |
| 197 | B43EF39A1A64F0E220AF740F9494291B |
| 198 | AC537817C2612744A58132A8AFBC44A3 |
| 199 | 98A321249A821DDBF81C38235A371A14 |
| 200 | AE1D46069090D81BB6B08FED9E687285 |
| 201 | 7EAE2415DC2CD60AE083249A33B56E05 |
| 202 | 3D942AAA9BC9F27289421CE0B301FB98 |
| 203 | 1548BA6D08530727AC6D059C005C6C42 |
| 204 | FF47C21142C65B502DA70647BAE831D1 |
| 205 | C83AA7FEAC5E51A08091E10DB0C233D9 |
| 206 | E86EDD2EC2DAA3104229EDC43471A16A |
| 207 | 22FAFB9C184B78B56EE91B6602C03244 |
| 208 | E45631DC509B1290C08D2C1A1F15DBFE |
| 209 | D203C51207092B56568FDAD9E2D44473 |
| 210 | 2AA87F31A7D1AB1C90024F936006C4A5 |
| 211 | 913136153593DEABC7305BF0C5A62180 |
| 212 | D8DA5FE401F2758642A082C53A6A5CB8 |
| 213 | 23C2295213147F324DE8EC1C103BAE88 |
| 214 | 883AF097FCDE82B366A1844245E0D727 |
| 215 | 79E5E9F8C933159ACADC22A06F900A70 |
| 216 | FE40502B44A9E44B2C336250D47538CC |
| 217 | 670452E19172C843176F1278FE41D584 |
| 218 | B7EAA436078E6886A3024F593AD57580 |
| 219 | 1044D4CDD7230E7B1953AD1232DF07E2 |
| 220 | 4D821ECAC3D845A2E1011695624576FF |
| 221 | 96622ED2FBD44D1B859D70601999F438 |
| 222 | CCC31C3D6D5B41B8D82FF4522A4C0146 |

| | |
|-----|----------------------------------|
| 223 | 4A84F7CD62E0C712980E6A0C89BF394F |
| 224 | 10E56751F000927284DBE174E68ECC4C |
| 225 | A3DE70921356F026E084CFE302A210A9 |
| 226 | B12DA0621B343A8C3FE941A32EA5D571 |
| 227 | D653135DE825A74B743E275C19020C71 |
| 228 | 5CAD301BF846B2EE921D33A3D4BB1220 |
| 229 | 1292445ACBB548C668FC3853578474E6 |
| 230 | B94B4B89C0654688C9E007D9061DF5FE |
| 231 | 75A2C91E76061A8680884E8BFD14A64A |
| 232 | 83726F3070B47ECE21504A5065D74A36 |
| 233 | 964A471444A270840919F7FE07382D14 |
| 234 | A582701EBFCA899B8497088C3560F300 |
| 235 | 64FCB63E21CAC63002D1E09FD1543274 |
| 236 | B1E1C83F689ADF422C865F98D288838A |
| 237 | A06A0D822165D3F3416B47419ECCB547 |
| 238 | 1D2068039A32B7EF728914ECE07CB416 |
| 239 | 64C0CF81F78E8823ECC8661A5295422A |
| 240 | 902A7243F593F2180E5A306A8438E6A9 |
| 241 | A4CCED356D56BF1B41C28E1504301FE8 |
| 242 | 82AE90E2F76B3055A2E3A966025CC01A |
| 243 | 8B90D5A62364E18574145C5895CEFF60 |
| 244 | 43F7EA1AB0D19032551AD9DE21307353 |
| 245 | DD5D8424AC60360B1C14E65815C9B15E |
| 246 | C632A67382ECB2681DFB8525140E2878 |
| 247 | 3A6ACF212B6F8B9C53FF224C2E00C16C |
| 248 | 86A90C267B1171093F362FE5CB14E3A0 |
| 249 | EA262EC36E6589C3BB005426AF2590F4 |
| 250 | 200F03126C5B0D7B901128E7757C5F70 |
| 251 | 68FC090C2221AA98BF0D24E85066EFC2 |
| 252 | 9E26CEC67832FC42A87E92FA1015212E |
| 253 | ACD889634F79506F2582EA03240F2A07 |
| 254 | AA65407E1F4A33BF9A62860A3D6A4CC0 |

| | |
|-----|----------------------------------|
| 255 | B1B950AC76A608AA32D04B03C7FF24D3 |
|-----|----------------------------------|

[Explanation difference:]

For low chip rate have different frame structure. It has the special time slot DwPTS and UpPTS to estimate the UL-synchronization and Cell search. So the ~~Sync~~ SYNC-DL and ~~Sync1~~ SYNC-UL code is needed in low chip rate TDD.

10 Physical layer procedures

10.1 Transmitter Power Control

[Description:]

The basic purpose of power control is to limit the interference level within the system thus reducing the intercell interference level and to reduce the power consumption in the UE.

[Rationale:]

General Parameters

The main characteristics of power control are summarized in the following table.

Table: Transmit Power Control characteristics

| | Uplink | Downlink |
|---------------------------|--|---|
| Power control rate | Variable Closed loop: 0-200 cycles/sec. Open loop: (about 200us – 3575us delay) | Variable closed loop: 0-200 cycles/sec. |
| Step size | 1,2,3 dB (closed loop) | 1,2,3 dB (closed loop) |
| Remarks | All figures are without processing and measurement times | within one timeslot the powers of all active codes may be balanced to within a range of [20] dB |

Note:

All codes within one timeslot allocated to the same CCTrCH use the same transmission power in case they have the same Spreading Factor. Gainfactors are applied to consider different spreading factors. ~~In case of different spreading factors in the uplink for the same CCTrCH are used, the power levels of the parallel codes portion are under further study.~~

10.1.2 Uplink Control

Open loop power control for the UpPTS

The transmit power level by a UE on the UpPTS shall be calculated based on the following equation:

$$P_{\text{UpPTS}} = L_{\text{P-CCPCH}} + \text{PRX}_{\text{UpPTS,des}}$$

where, P_{UpPTS} : transmit power level in dBm,

$L_{\text{P-CCPCH}}$: measured path loss in dB (P-CCPCH reference transmit power level is broadcast on BCH),

$\text{PRX}_{\text{UpPTS,des}}$: desired RX power level at cell's receiver in dBm, which is broadcast on BCH.

The interference power on the UpPTS (I_{UpPTS}) measured by the Node B is reported to the RNC on a regular basis to allow the RNC to make a decision for new control parameters.

The network signals (on BCH) a power increment that is applied only for the access procedure. At each new transmission of a ~~SYNC1~~ SYNC-UL burst during the access procedure, the transmit power level can be increased by this power increment.

10.1.2.2 Common Physical Channel

In low chip rate TDD option system, the F-PACH brings the answer to the ~~SYNC1~~ SYNC-UL burst of the UE. The answer, a one burst long message, shall bring besides the acknowledgment to the received ~~SYNC1~~ SYNC-UL burst, the timing and power level indications to prepare the transmission of the RACH burst.

The transmit power level on the PRACH is calculated by the following equation:

$$P_{\text{PRACH}} = L_{\text{P-CCPCH}} + \text{PRX}_{\text{PRACH,des}}$$

Where, P_{PRACH} is the UE transmit power level on the PRACH;

$\text{PRX}_{\text{PRACH,des}}$ is the desired receive power level on the PRACH, as signalled by the network on the F-PACH

The network computes the $\text{PRX}_{\text{PRACH,des}}$ by measuring the interference on the PRACH timeslot which has to be averaged over an configurable (by O&M) number of frames (N).

10.1.2.3 Dedicated Physical Channel

The closed loop power control makes uses of layer 1 symbol in the DPCH. The power control step can take the values 1,2,3 dB within the overall dynamic range 80dB. The initial transmission power of the uplink Dedicated Physical Channel is signalled by the UTRAN.

Closed-loop TPC is based on SIR, and the TPC processing procedures are described in this section. During this power control process, the node B periodically makes a comparison between the received SIR measured value and the target SIR value. When the measured value is higher than the target SIR value, TPC command = 'down'. When this is lower than the target SIR value, TPC command = 'up'. At the UE, soft decision on the TPC bits is performed, and when it is judged as 'down', the mobile transmit power shall be reduced by one power control step, whereas if it is judged as 'up', the mobile transmit power shall be raised by one power control step. A higher layer outer loop adjusts the target SIR. This scheme allows quality based power control.

When the TPC bit cannot be received due to out-of-synchronisation, the transmission power value shall be kept at a constant value. When SIR measurement cannot be performed for being out-of-synchronisation, the TPC command shall always be set to = 'up' during the period of being out-of-synchronisation.

10.1.3 Downlink Control

10.1.3.1 Common Physical Channel

The power of the P-CCPCH

The primary CCPCH transmit power is set by high layer signalling and can be changed based on network determination. The reference power of P-CCPCH is signalled on the BCCH on a periodic basis.

The power value for the F-PACH is set by the network.

The relative transmit power of the S-CCPCH (for FACH) and PICH compared to the P-CCPCH transmit power is set by higher layers.

~~It is set by the network and can take into account both the received power level on the PRACH from the addressed UE and the transmit power level as signalled by the UE.~~

~~The power of the S-CCPCH(for PCH)~~

~~This condition is the same as P-CCPCH.~~

10.1.3.2 Dedicated Physical Channel

The initial transmission power of the downlink Dedicated Physical Channel is set by the network until the first UL DPCH arrives. After the initial transmission, the node B transits into SIR-based closed-loop TPC.

The measurement of received SIR shall be carried out periodically at the UE. When the measured value is higher than the target SIR value, TPC command = 'down'. When this is lower than the target SIR value, TPC command = 'up'. At the Node B, soft decision on the TPC bits is performed, and when it is judged as 'down', the transmission power shall be reduced by one power control step, whereas if judged as 'up', the transmission power shall be raised by one power control step.

When the TPC bit cannot be received due to out-of-synchronisation, the transmission power value shall be kept at a constant value.

When SIR measurement cannot be performed due to out-of-synchronisation, the TPC command shall always be = 'up' during the period of being out-of-synchronisation.

[Explanation difference:]

In low chip rate TDD option, for uplink, the power control update of PRACH can be calculated according to the received power of UpPTS. The power control of the DPCH is closed loop transmitter power control. Closed loop power control in uplink is used because of beamforming. Open loop power control is under consideration if there is no beamforming. For the downlink the transmit power control adjustment of the S-CCPCH_(for FACH) can be calculated according to the transmit power level signaled in the RACH.

In high chip rate TDD option, for uplink, the power controls of the PRACH and DPCH are open loop transmitter power control. For downlink, the initial transmission power of DPCH is set by the network.

Operation of multiple CCH is under studying.

10.2 UL Synchronisation Timing Advance

~~10.2.1 With UL Synchronization~~

[Description:]

This section describes the detail description on the UL synchronization including the establishment of UL synchronization and maintenance of the UL synchronization.

[Rationale:]

10.2.1 General Description

Support of UL synchronization is mandatory for the UE.

10.2.1.1 Preparation of uplink synchronization (downlink synchronization)

When a UE is powered on, it first needs to establish the downlink synchronisation with the cell. Only after the UE has established the downlink synchronisation, it shall start the uplink synchronisation procedure.

10.2.1.2 Establishment of uplink synchronization

The establishment of uplink synchronization is done during the random access procedure and involves the UpPCH and the PRACH.

Although the UE can receive the downlink signal from the Node B, the distance to Node B is still uncertain. This would lead to unsynchronised uplink transmission. Therefore, the first transmission in the uplink direction is performed in a special time-slot UpPTS to reduce interference in the traffic time-slots.

The timing used for the UpPCH is set e.g. according to the received power level of DwPCH and/or P-CCPCH.

After the detection of the SYNC_UL sequence in the searching window, the Node B will evaluate the timing, and reply by sending the adjustment information to the UE to modify its timing for next transmission. This is done with the FPACH within the following 4 sub-frames. After sending the PRACH the uplink synchronization is established. The uplink synchronisation procedure shall also be used for the re-establishment of the uplink synchronisation when uplink is out of synchronisation.

10.2.1.3 Maintenance of uplink synchronisation

Uplink synchronization is maintained in 1.28Mcps TDD by sending the uplink advanced in time with respect to the timing of the received downlink.

For the maintenance of the uplink synchronization, the midamble field of each uplink burst can be used.

In each uplink time slot the midamble for each UE is different. The Node B may estimate the timing by evaluating the channel impulse response of each UE in the same time slot. Then, in the next available downlink time slot, the Node B will signal Synchronisation Shift (SS) commands to enable the UE to properly adjust its Tx timing.

10.2.2 UpPCH

Open loop uplink synchronisation control is used for UpPCH.

The UE may estimate the propagation delay t_p based upon the path loss using the received P-CCPCH and/or DwPCH power.

The UpPCH is sent to the Node B advanced in time according to the timing of the received DwPCH. The time of the beginning of the UpPCH $T_{TX-UPPCH}$ is given by:

$$T_{TX-UPPCH} = T_{RX-DwPCH} - 2t_p + 12 \cdot 16 T_C$$

in multiple of 1/8 chips, where

$T_{TX-UPPCH}$ is the beginning time of UpPCH transmission with the UE's timing,

$T_{RX-DwPCH}$ is the received beginning time of DwPCH with the UE's timing,

$2t_p$ is the timing advance of the UpPCH ($UpPCH_{ADV}$).

10.2.3 PRACH

The Node B shall measure the received SYNC UL timing deviation $UpPCH_{POS}$. $UpPCH_{POS}$ is sent in the FPACH and is represented as an 11 bit number (0-2047) being the multiple of 1/8 chips which is nearest to received position of the $UpPCH$.

Time of the beginning of the PRACH $T_{TX-PRACH}$ is given by:

$$T_{TX-PRACH} = T_{RX-PRACH} - (UpPCH_{ADV} + UpPCH_{POS} - 8 * 16 T_C)$$

in multiple of 1/8 chips, where

$T_{TX-PRACH}$ is the beginning time of PRACH transmission with the UE's timing,

$T_{RX-PRACH}$ is the beginning time of PRACH reception with the UE's timing if the PRACH was a DL channel.

10.2.4 DPCCH and PUSCH

The closed loop uplink synchronisation control uses layer 1 symbols (SS commands) for DPCCH and PUSCH. After establishment of the uplink synchronisation, NodeB and UE start to use the closed loop UL synchronisation control procedure. This procedure is continuous during connected mode.

The Node B will continuously measure the timing of the UE and send the necessary synchronisation shift commands in each sub-frame. On receipt of these synchronisation shift commands the UE shall adjust the timing of its transmissions accordingly, in steps of $\pm k/8$ chips or do nothing, each M sub-frames.

The default value of M (1-8) and k (1-8) is broadcast in the BCH. The value of M and k can also be adjusted during call setup or readjusted during the call.

During a 1.28 Mcps TDD to 1.28 Mcps TDD hand-over the UE shall transmit in the new cell with timing advance TA adjusted by the relative timing difference Δt between the new and the old cell:

$$TA_{new} = TA_{old} + \Delta t$$

10.2.4.1 Out of synchronization handling

Same as that of 3.84 Mcps TDD, cf. [4.2.2.3.3 Out of synchronisation handling.]

~~10.2.1.1 The establishment of uplink synchronization~~

~~10.2.1.1.1 Preparation of uplink synchronization (downlink synchronization)~~

~~When a UE is powered on, it first needs to establish the downlink synchronisation with the cell as describe in paper about cell search procedure. Only after the UE can establish and maintain the downlink synchronisation, it can start the uplink synchronisation procedure.~~

~~10.2.1.1.2 Establishment uplink synchronization~~

~~Although the UE can receive the downlink synchronization signal from the Node B, the distance to Node B is still uncertain which would lead unsynchronised uplink transmission. Therefore, the first transmission in uplink direction is performed in a special time slot $UpPTS$ to reduce interference in traffic time slots.~~

~~The timing used for the SYNC1 SYNC_UL burst are set e.g. according to the received power level of $DwPTS$ and/or $P-CCPCH$.~~

~~At the detection of the SYNC1 SYNC_UL sequence in the searching window, the Node B will evaluate the received power levels and timing, and reply by sending the adjustment information to UE to modify its timing and power level for next transmission and for establishment of the uplink synchronisation procedure. Within the next 4 sub-frames, the Node B will send the adjustment information to the UE (in a single subframe message in the FPACH). The uplink synchronisation procedure, normally used for a random access to the~~

~~system, can also be used for the re-establishment of the uplink synchronisation when uplink is out of synchronisation.~~

~~10.2.1.2. Maintenance of uplink synchronisation~~

~~For the maintenance of the uplink synchronization, the midamble field of each uplink burst can be used.~~

~~In each uplink time slot the midamble in each UE is different. The Node B can estimate the power level and timing shift by measuring the midamble field of each UE in the same time slot. Then, in the next available downlink time slot, the Node B will signal the Synchronisation Shift (SS) and the Power Control (PC) commands to enable the UE to properly adjust respectively its Tx timing and Tx power level.~~

~~These procedures guarantee the reliability of the uplink synchronisation. The uplink synchronization can be checked once per TDD sub-frame. The step size in uplink synchronization is configurable and re-configurable and can be adapted from 1/8 chip to 1 chip duration. The following updates for UL synchronization are possible: 1 step up; 1 step down; no update.~~

~~[Explanation difference:]~~

~~For high chip rate option, uplink synchronisation is mentioned in 4.3 of TS25.224. But the implementation method is a little different with the low chip rate option. For low chip rate option, the establishment of the UL synchronization is done by using the UpPTS and the FPACH.~~

~~It allocates a unique time slot UpPTS for UE to establish uplink synchronisation in the access procedure. The benefit of this method is when the UE wants to do random access, the P-RACH will have minimum interference to other traffic channel. Vice-versa, it will also reduce the interference from traffic channels to P-RACH.~~

10.3 Synchronisation and Cell Search Procedures

10.3.1 Cell Search

[Description:]

In this section, a 4step cell search procedure for low chip rate TDD option is described which is a slightly different with the current 3 step cell search procedure for high chip rate TDD option.

[Rational:]

During the initial cell search, the UE searches for a cell. It then determines the DwPTS synchronization, scrambling and basic midamble code identification, control multi-frame synchronisation and then reads the contents in BCH. This initial cell search is carried out in 4 steps:

Step 1: Search for DwPTS

During the first step of the initial cell search procedure, the UE uses the ~~SYNC~~SYNC-DL (in DwPTS) to acquire DwPTS synchronization to a cell. This is typically done with one or more matched filters (or any similar device) matched to the received ~~SYNC~~SYNC-DL which is chosen from PN sequences set. A single or more matched filter (or any similar device) is used for this purpose. During this procedure, the UE needs to identify which of the 32 possible ~~SYNC~~SYNC-DL sequences is used.

Step 2: Scrambling and basic midamble code identification

During the second step of the initial cell search procedure, the UE receives the midamble of the P-CCPCH. The P-CCPCH is followed by the DwPTS. In the current low chip rate TDD option each DwPTS code corresponds to a group of 4 different basic midamble code. Therefore there are total 128 midamble codes and these codes are not overlapping with each other. Basic midamble code number divided by 4 gives the ~~SYNC~~SYNC-DL code number. Since the ~~SYNC~~SYNC-DL and the group of basic midamble codes of the P-CCPCH are related one by one (that is, once the ~~SYNC~~SYNC-DL is detected, the 4 midamble codes can be determined), the UE knows which 4 basic midamble codes is used. Then the UE can determine the used basic midamble code using a try

and error technique. The same basic midamble code will be used throughout the frame. As each basic midamble code is associated with a scrambling code, the scrambling code is also known by that time. According to the result of the search for the right midamble code, UE may go to next step or go back to step 1.

Step 3: Control multi-frame synchronisation

During the third step of the initial cell search procedure, the UE searches for the head of multi-frame indicated by QPSK phase modulation of the DwPTS with respect to the P-CCPCH midamble. The control multi-frame is positioned by a sequence of QPSK symbols modulated on the DwPTS. [n]consecutive DwPTS are sufficient for detecting the current position in the control multi-frame. To ensure correct decisions, an additional bit coded together with a BCH block, allows the UE to know the BCH interleaving block in P-CCPCH. According to the result of the control multi-frame synchronisation for the right midamble code, UE may go to next step or go back to step 2.

Step 4: Read the BCH

The (complete) broadcast information of the found cell in one or several BCHs is read. According to the result the UE may move back to previous steps or the initial cell search is finished.

[Explanation difference:]

The initial cell search procedure is optimized considering the frame structure that is needed to enable UL synchronization and other specific features and properties for low chip rate option .

For high chip rate option , the three steps are : slot synchronisation, frame synchronisation and code-group identification, scrambling code identification.

For low chip rate option , the four steps are : search for DwPTS , scrambling and basic midamble code identification, control multi-frame synchronisation and the read of BCH information.

10.4 Discontinuous transmission (DTX) of Radio Frames

'Common with the high chip rate TDD mode'

[Description:]

The different downlink transmit diversity schemes for different channel has been considered in low chip rate TDD option.

[Rationale:]

10.5 Downlink Transmit Diversity

10.5.1 Transmit Diversity for DPCH

'Common with the high chip rate TDD'

Difference: Time Switched Transmit Diversity (TSTD) may also be employed as transmit diversity scheme for downlink DPCH.

10.5.1.1 TSTD for DPCH

TSTD can be employed as transmit diversity scheme for downlink DPCH. An example for the transmitter structure of the TSTD transmitter is shown in figure [6]. Channel coding, rate matching, interleaving, bit-to-symbol mapping, spreading, and scrambling are performed as in the non-diversity mode. Then the data is time multiplexed with the midamble sequence. Then, after pulse shaping, modulation and amplification, DPCH is transmitted from antenna 1 and antenna 2 alternately every sub-frame. Not all DPCH in the sub-frame need to be transmitted on the same antenna and not all DPCH within a sub-frame have to use TSTD. Figure [7] shows an example for the antenna switching pattern for the transmission of DPCH for the case that all physical channels are transmitted with TSTD and are using the same antenna in the sub-frame.

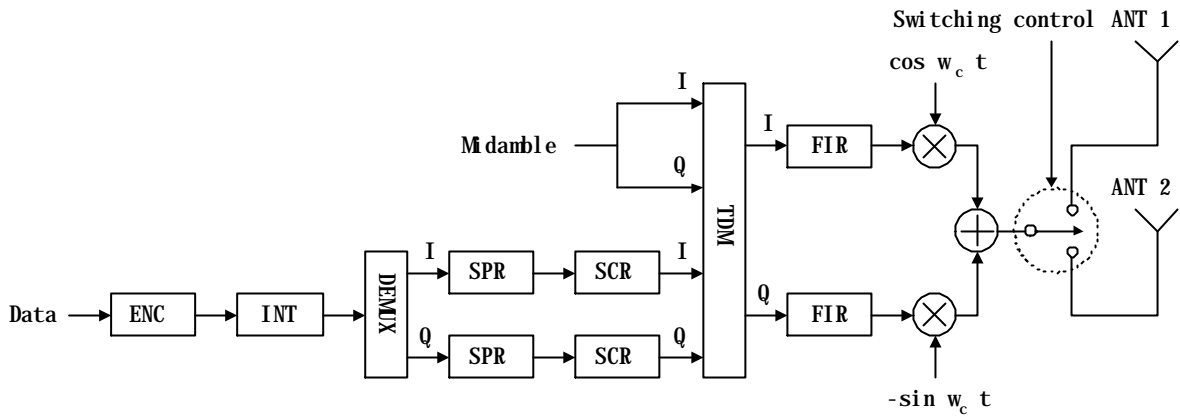


Figure [6]: Example for TSTD Transmitter structure for DPCH and P-CCPCH.

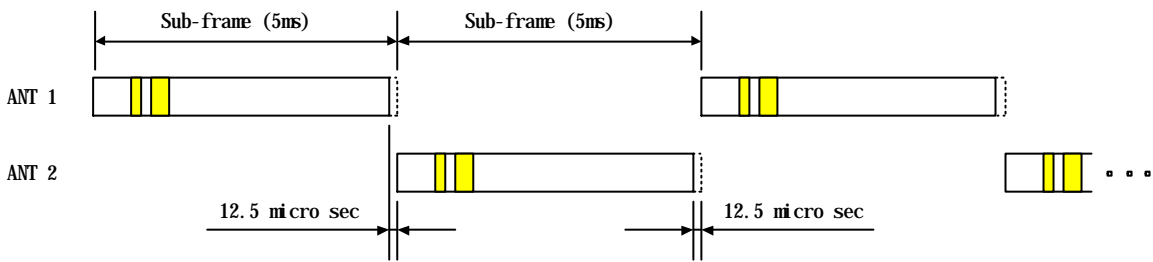


Figure [7]: Example for the antenna swithing pattern for TSTD transmission of DPCH and P-CCPCH: all physical channels are transmitted with TSTD and are using the same antenna in the sub-frame.

10.5.1.2 Closed Loop Tx Diversity for DPCH

The transmitter structure to support transmit diversity for DPCH transmission is shown in figure [8]. Channel coding, interleaving and spreading are done as in non-diversity mode. The spread complex valued signal is fed to both TX antenna branches, and weighted with antenna specific weight factors w_1 and w_2 . The weight factors are complex valued signals (i.e., $w_i = a_i + jb_i$), in general. These weight factors are calculated on a per slot and per user basis.

The weight factors are determined by the UTRAN.

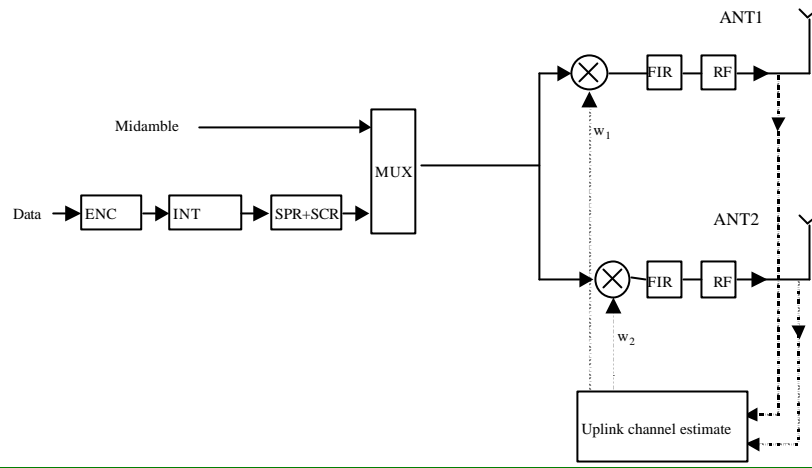


Figure [8]: Downlink transmitter structure to support Transmit Diversity for DPCH transmission (UTRAN Access Point) in 1.28Mcps TDD

10.5.2 Transmit Diversity for SCH/DwPCH

The SCH function in high chip rate TDD has been achieved by ~~DwPTS~~-DwPCH in low chip rate TDD and transmit diversity schemes for the DwPTS in low chip rate TDD is common with that for SCH in high chip rate TDD.

The transmitter structure to support transmit diversity for DwPCH transmission is shown in figure [9]. DwPCH is transmitted from antenna 1 and antenna 2 alternatively.

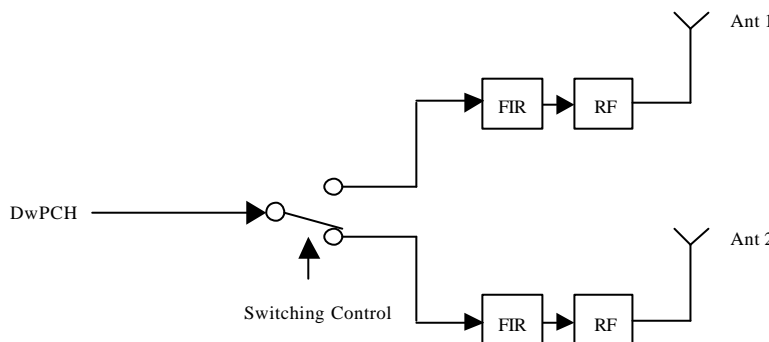


Figure [9]: Downlink transmitter structure to support Transmit Diversity for DwPCH transmission (UTRAN Access Point) in 1.28Mcps TDD

10.5.3 Transmit Diversity for P-CCPCH

TSTD or Block Space Time Transmit Diversity (Block STTD) can be employed as transmit diversity scheme for the Primary Common Control Physical Channel (P-CCPCH)

~~Transmit diversity for P-CCPCH as in the high chip rate option (i.e., Block STTD) is not supported in low chip rate TDD.~~

10.5.3.1 TSTD Transmission Scheme for P-CCPCH

A block diagram of an example of a TSTD transmitter is shown in figure [6]. Channel coding, rate matching, interleaving, bit-to-symbol mapping, spreading, and scrambling are performed as in the non-diversity mode. Then the data is time multiplexed with the midamble sequence. Then, after pulse shaping and modulation and amplification, P-CCPCH is

transmitted from antenna 1 and antenna 2 alternately every sub-frame. If there is a DPCH that uses TSTD, TSTD is also applied to P-CCPCH. An example of the antenna-switching pattern is shown in figure [7].

[Explanation difference:]

~~If both the uplink and downlink physical channels are work under the synchronization mode and if "smart antenna" method is used, the interference on P-CCPCH is thought to be very little in low chip rate TDD option. As a result, "Tx diversity" has not been considered currently to be applied in low chip rate TDD. As this may not hold in all cases, the Block STTD applied for P-CCPCH is to be studied. TSTD makes use of the subframe structure of 1.28Mcps TDD and is therefore also suited for 1.28Mcps TDD.~~

10.5.4 Transmit diversity for FPACH

~~The same scheme as for the DPCH can be used for the FPACH.~~

10.6 Random Access Procedure

[Description:]

The random access procedure and the collision problems for low chip rate option are described here. It include the preparation of random access, the random access procedure and the procedure for random access collision.

Note:

In this paper, the FPACH is just a physical channel used to carry one burst message responding to ~~SYNC1~~SYNC-UL during random access procedure. There is no mapping relationship between FACH and FPACH. The FPACH here is a little like the AICH in FDD.

[Rationale:]

10.6.1 Preparation of random access

When the UE is in Idle mode, it will keep the downlink synchronisation and read the cell broadcast information. From the used DwPTS, the UE will get the code set of 8 ~~SYNC1~~SYNC-UL codes (signatures) assigned to UpPTS physical channel for random access. There are total 256 different ~~SYNC1~~SYNC-UL sequences. ~~SYNC1~~SYNC-UL sequences number divided by 8 gives the DwPTS sequences number. From the cell broadcast information, the UE will get to know the used ~~SYNC1~~SYNC-UL sequences within the code set to be used; the description (codes, spreading factor, midambles, time slots) of the P-RACH channels, the description (codes, spreading factor, midambles, time slots) of the FPACH channels, and other information (if needed) related to random access.

In the BCH it is described what ~~SYNC1~~SYNC-UL sequences are associated with what FPACH resources; what FPACHs are associated with what P-RACH resources and what P-RACH resources are associated with what ~~(P/S)-S~~S-CCPCH (carrying the FACH logical channel) resources.

Thus, when sending a ~~SYNC1~~SYNC-UL sequence, the UE knows which FPACH resources, P-RACH resources and CCPCH resources will be used for the access.

10.6.2 Random access procedure

The physical random access procedure described below is invoked whenever a higher layer requests transmission of a message on the RACH. The physical random access procedure is controlled by primitives from RRC and MAC.

10.6.2.1 Definitions

$FPACH_i$: FPACH number i

L_i : Length of RACH message associated to $FPACH_i$ in sub-frames

N_{RACH_i} : The number of PRACHs associated to the i^{th} FPACH

n_{RACH_i} : The number of a PRACH associated to the i^{th} FPACH ranging from 0 to $N_{RACH_i}-1$

M : Maximum number transmissions in the UpPCH

WT : Maximum number of sub-frames to wait for the network acknowledgement to a sent signature

SFN' : The sub-frame number counting the sub-frames. At the beginning of the frame with the system frame number $SFN=0$ the sub-frame number is set to zero.

10.6.2.2 Preparation of random access

When the UE is in Idle mode, it will keep the downlink synchronisation and read the cell broadcast information. From the used SYNC-DL code in DwPCH, the UE will get the code set of 8 SYNC-UL codes (signatures) assigned to UpPCH for random access.

The description (codes, spreading factor, midambles, time slots) of the P-RACH, FPACH, and S-CCPCH (carrying the FACH logical channel) channel is broadcast on the BCH.

Thus, when sending a SYNC-UL sequence, the UE knows which FPACH resources, P-RACH resources and CCPCH resources will be used for the access.

The UE needs to decode the BCH information regarding the random access prior to transmission on the UpPCH.

The physical random access procedure described in this sub-clause is initiated upon request of a PHY-Data-REQ primitive from the MAC sub-layer (see [18] and [19]).

Before the physical random-access procedure can be initiated, Layer 1 shall receive the following information by a CPHY-TrCH-Config-REQ from the RRC layer:

- The association between which signatures and which FPACHs; which FPACHs and which PRACHs; which PRACHs and which CCPCHs: including the parameter values for each listed physical channel.
- The length L_i of a RACH message associated to $FPACH_i$ can be configured to be either 1 or 2 or 4 sub-frames corresponding to a length in time of either 5 ms or 10 ms or 20 ms.

NOTE 1: N_{RACH_i} PRACHs can be associated with to $FPACH_i$. The maximum allowed N_{RACH_i} is L_i .

- The available UpPCH sub-channels for each Access Service Class (ASC):

NOTE 2: An UpPCH sub-channel is defined by a (sub-set of) signature(s) and sub-frame numbers.

- The set of Transport Format parameters for the PRACH message;
- The "M" maximum number transmissions in the UpPCH;
- The "WT" maximum number of sub-frames to wait for the network acknowledgement to a sent signature: (1.4) the maximum value supported by Layer 1 is 4 sub-frames.
- The initial signature power "Signature Initial Power":

NOTE 2: The above parameters may be updated from higher layers before each physical random access procedure is initiated.

At each initiation of the physical random access procedure, Layer 1 shall receive the following information from the higher layers (MAC):

- The Transport Format to be used for the specific PRACH message;

- The ASC for the specific Random Access procedure with the timing and power level indication;
- The data to be transmitted (Transport Block Set).

10.6.2.3 Random access procedure

The physical random-access procedure shall be performed as follows:

UE side:

- 1 Set the Signature Re-Transmission Counter to M.
- 2 Set the Signature transmission power to Signature Initial Power.
- 3 Randomly select the UpPCH sub-channel from the available ones for the given ASC. The random function shall be such that each of the allowed selections is chosen with equal probability.
- 4 Transmit a signature using the selected UpPCH sub-channel at the signature transmission power.
- 5 After sending a signature, listen to the relevant FPACH for the next WT sub-frames to get the network acknowledgement. The UE will read the FPACH_i associated to the transmitted UpPCH only in the sub-frames fulfilling the following relation:

$$(SFN' \bmod L) = n_{RACHi}; n_{RACHi} = 0, \dots, N_{RACHi} - 1.$$

- 6 In case no valid answer is detected in the due time: decrease the Signature Re-transmission counter by one and if it is still greater than 0, then repeat from step 3; else report a random access failure to the MAC sub-layer.
- 7 In case a valid answer is detected in the due time
 - a) set the timing and power level values according to the indication received by the network in the FPACH_i;
 - b) send at the sub-frame coming 2 sub-frames after the one carrying the signature acknowledgement, the RACH message on the relevant PRACH. In case L_i is bigger than one and the sub-frame number of the acknowledgement is odd the UE will wait one more sub-frame. The relevant PRACH is the n_{RACHi}th PRACH associated to the FPACH_i if the following equation is fulfilled:

$$(SFN' \bmod L) = n_{RACHi};$$

Here SFN' is the sub-frame number of the arrival of the acknowledgement.

Both on the UpPCH and on the PRACH, the transmit power level shall never exceed the indicated value signalled by the network.

Network side:

- The node B will transmit the FPACH_i associated the transmitted UpPCH only in the sub-frames fulfilling the following relation:

$$(SFN' \bmod L) = n_{RACHi}; n_{RACHi} = 0, \dots, N_{RACHi} - 1.$$

- The Node B will not acknowledge UpPCHs transmitted more than WT sub-frames ago

At the reception of a valid signature:

- Measure the timing deviation with respect to the reference time T_{ref} of the received first path in time from the UpPCH and acknowledge the detected signature sending the FPACH burst on the relevant FPACH.

For examples on the random access procedure refer to Annex E.

10.6.2.3.1. The use and generation of the information fields transmitted in the FPACH

The Fast Physical Access CHannel (FPACH) is used by the Node B to carry, in a single burst, the acknowledgement of a detected signature with timing and power level adjustment indication to a user

equipment.

The length and coding of the information fields is explained in TS25.221 sub-clause 6.3.3.1.

10.6.2.3.1.1 Signature Reference Number

The Signature Reference Number field contains the number of the acknowledged signature. The user equipment shall use this information to verify whether it is the recipient of the FPACH message.

10.6.2.3.1.2 Relative Sub-Frame Number

The Relative Sub-Frame Number field indicates the current sub-frame number with respect to the sub-frame at which the acknowledged signature has been detected.

The user equipment shall use this information to verify whether it is the recipient of the FPACH message.

10.6.2.3.1.3 Received starting position of the UpPCH ($UpPCH_{POS}$)

The *received starting position of the UpPCH ($UpPCH_{POS}$)* field indirectly indicates to the user equipment the timing adjustment it has to implement for the following transmission to the network. The node B computes the proper value for this parameter according to the following rules: $UpPCH_{POS} = UpPTS_{R_{path}} - UpPTS_{TS}$

where

$UpPTS_{R_{path}}$: time of the reception in the Node B of the SYNC-UL to be used in the uplink synchronization process

$UpPTS_{TS}$: time instance two symbols prior to the end of the DwPCH according to the Node B internal timing

This information shall be used by the UE to adjust its timing when accessing the network as described in section 10.2. 'Uplink Synchronisation'

10.6.2.3.1.4 Transmit Power Level Command for the RACH message

This field indicates to the user equipment the power level to use for the RACH message transmission on the FPACH associated P-RACH.

The network may set this value based on the measured interference level (I) (in dBm) on the specific PRACH and on the desired signal to interference ratio (SIR) (in dB) on this channel as follows:

Transmit Power Level Command for the PRACH ($PRX_{PRACH,des}$)

$PRX_{PRACH,des}$ is the desired receive power level on the PRACH.

The UE shall add to this value the estimated path-loss to compute the power level to transmit for the PRACH.

10.6.2.4 Random access collision

When a collision is very likely or in bad propagation environment, the Node B does not transmit the FPACH or cannot receive the SYNC-UL. In this case, the UE will not get any response from the Node B. Thus the UE will have to adjust its Tx time and Tx power level based on a new measurement and send a SYNC-UL again after a random delay.

Note that at each (re-)transmission, the SYNC-UL sequence will be randomly selected again by the UE.

Note : Due to the two-step approach a collision most likely happens on the UpPCH. The RACH RUs are virtually collision free. This two-step approach will guarantee that the RACH RUs can be handled with conventional traffic on the same UL time slots.

~~The SYNC1 sequence in UpPTS following the guard time slot is used only for uplink synchronisation. The UE randomly selects one of the 1-8 possible signatures of the cell it wants to access to and sends it on the UpPTS physical channel.~~

~~Then the UE determines the timing and the Tx power level (open loop procedure) for the UpPTS and transmits the selected signature on the UpPTS.~~

~~Once the Node B detects the UpPTS transmission from an UE, the arrival time and the received power are known. The Node B determines the Tx power update and timing adjustment and sends them to the UE within the next four frames through the FPACH (in a single burst/sub-frame message). Note that the FPACH also~~

~~contains the signature reference and the relative frame number (number of frames passed after the reception of the acknowledged signature) for cross check with the UE.~~

~~Once the UE receives the above mentioned control signalling from the chosen FPACH (i.e. the FPACH which is associated to the selected signature), its UpPTS sequence has been accepted by the Node B. Then the UE will adjust its timing and power level and send the RACH (also as a single burst/sub-frame message) on the P-RACH channel corresponding to the FPACH exactly two frames later. In this step, the RACH sent to Node B by UE will have high synchronisation precision.~~

~~After that, the UE will receive a response from the network from the CCPCH associated to the P-RACH (by the FACH logical channel) indicating whether the UE random access has been accepted or not. In case it has been accepted the further signalling for establishing the link will take place on UL and DL dedicated channels assigned by the network through the FACH.~~

~~The UE can transmit a second UpPTS and wait for the response from the FPACH for a further power and SS update before transmitting on the assigned resources.~~

~~Note: Details of the random access procedure including the FPACH coding are for further study and proposals are under consideration.~~

10.6.3 Random access collision

When a collision is very likely or in bad propagation environment, the Node B does not transmit the FPACH or cannot receive the ~~SYNC1~~SYNC-UL. In this case, the UE will not get any response from the Node B. Thus the UE will have to adjust its Tx time and Tx power level based on a new measurement and send a ~~SYNC1~~SYNC-UL again after a random delay.

Note that at each (re-)transmission, the ~~SYNC1~~SYNC-UL burst will be randomly selected again by the UE.

Due to the two-step approach a collision most likely happens on the UpPTS. The RACH RUs are virtually collision free. This two-step approach will guarantee that the RACH RUs can be handled with conventional traffic on the same UL time slots.

[Explanation difference:]

Different from the high chip rate option, the random access procedure of low chip rate option has two-step approach. The ~~SYNC1~~SYNC-UL word is used to carry out uplink synchronisation and to resolve the access collision. This two-step procedure enables the RACH RUs to be handled with conventional traffic on the same UL time slots.

A.1 Example Implementation of Closed Loop Uplink Power Control in Node B for 1.28 Mcps TDD

The measurement of received SIR shall be carried out periodically at Node B. When the measured value is higher than the target SIR value, TPC command = "down". When the measurement is lower than or equal to the target SIR, TPC command = "up".

In case of an uplink transmission pause on DPCH, the initial uplink transmission power of DPCH after the pause can be determined by an open loop power control. After the initial transmission after the pause, a closed loop uplink power control procedure can resume.

A.2 Example Implementation of Downlink Power Control in UE for 1.28 Mcps TDD when TSTD is used

When TSTD is applied, the UE can use the consecutive measurements of SIR to calculate SIR_{AVG} :

$$SIR_{AVG}(i) = w_1 \cdot SIR(i-1) + w_2 \cdot SIR(i),$$

where, $w_1 + w_2 = 1$, $w_1 \geq 0$, $w_2 \geq 0$, and $SIR(i)$ is the measurement of SIR in sub-frame i and $SIR_{AVG}(i)$ is the measurement of SIR_{AVG} in sub-frame i . If SIR_{AVG} is greater than the target SIR value, TPC command = "down". If the SIR_{AVG} is smaller than the target SIR value, TPC command = "up".

In case of a downlink transmission pause on the DPCH, the example in Annex A.2 can be used for DL power control with $RSCP_{vir}(i)$ and $ISCP(i)$ replaced by $RSCP_{AVG}(i)$ and $ISCP_{AVG}(i)$, where

$$RSCP_{AVG}(i) = w_1 \cdot RSCP_{vir}(i-1) + w_2 \cdot RSCP_{vir}(i),$$

$$ISCP_{AVG}(i) = w_1 \cdot ISCP(i-1) + w_2 \cdot ISCP(i).$$

A.3 Example Implementation of open Loop Power Control for access procedure for 1.28 Mcps TDD

The higher layer signals (on BCH) a power increment that is applied only for the access procedure. At each new transmission of a SYNC UL burst during the access procedure, the transmit power level can be increased by this power increment.

A.4 Examples random access procedure for 1.28Mcps TDD

Figure E-1 Single burst RACH WT=4, L =1, SF4 PRACH

| | | | | | | | | | | | |
|----------------------------|---|---|---|---|---|---|---|---|---|---|----|
| Sub-frame Number | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
| Users sending on UpPCH | 1 | 3 | 5 | 7 | | | | | | | |
| | 2 | 4 | 6 | 8 | | | | | | | |
| Acknowledged user on FPACH | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | | | |
| User sending RACH 0 | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | |

User 8 is not granted because more than 5 frames would have passed since the UpPCH.

Figure E-2 Two burst RACH WT=4, L =2, SF8 RACH

| | | | | | | | | | | | | |
|----------------------------|---|---|---|---|---|---|---|---|---|---|----|----|
| Sub-frame Number | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
| Users sending on UpPCH | 1 | 3 | 5 | 7 | | | | | | | | |
| | 2 | 4 | 6 | 8 | | | | | | | | |
| Acknowledged user on FPACH | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | | | | |
| User sending RACH 0 | | | | | 2 | 2 | 4 | 4 | 6 | 6 | | |
| User sending RACH 1 | | | | | 1 | 1 | 3 | 3 | 5 | 5 | 7 | 7 |

User 8 is not granted because more than 5 frames would have passed since the UpPCH.

Figure E-3 four burst RACH WT=4, L =4, SF16 RACH

| | | | | | | | | | | | | | | |
|------------------|---|---|---|---|---|---|---|---|---|---|----|----|----|----|
| Sub-frame Number | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|------------------|---|---|---|---|---|---|---|---|---|---|----|----|----|----|

Figure E-4 four burst RACH WT=4, L =4, SF16 RACH

| Sub-frame Number | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|----------------------------|---|---|---|---|---|---|---|---|---|---|----|----|----|
| Users sending on UpPCH | 1 | 3 | 5 | 7 | | | | | | | | | |
| | 2 | 4 | 6 | 8 | | | | | | | | | |
| Acknowledged user on FPACH | X | 1 | | | 2 | 3 | | | X | X | | | |
| User sending RACH 0 | | | | | | | 2 | 2 | 2 | 2 | | | |
| User sending RACH 1 | | | | | 1 | 1 | 1 | 1 | 3 | 3 | 3 | 3 | |

The FPACH is used ONLY in sub-frames 0, 1, 4, 5, 8, 9... because they correspond to the used RACH resources.

The FPACH in sub-frame 0 is not used because no UpPCH is preceding.

The FPACH in sub-frames 8,9 is not used because no UpPCH is preceding in the last 4 sub-frames.

In contrast to the previous examples users 4,5,6,7 are not granted because they would no lead to a RACH anyway. In this example their grand would come too late.

User 8 is not granted because more than 4 frames would have passed since the UpPCH.

11 Physical layer measurements

All the sections of this chapter are marked as: 'Common with the high chip rate TDD mode'. The range/mapping values should be discussed in WG2/WG4.

11.1 Control of UE/UTRAN measurements

11.1.1 General measurement concept

'Common with the high chip rate TDD mode'

11.1.2 Measurements for cell selection/reselection

'Common with the high chip rate TDD mode'

11.1.3 Measurements for Handover

11.1.4 Measurements for DCA

'Common with the high chip rate TDD mode'

11.1.5 Measurements for timing advance

11.2 Measurement abilities for UTRA TDD

11.2.1 UE measurement abilities

11.2.1.1 PCCPCH RSCP

11.2.1.2 CPICH RSCP

11.2.1.3 RSCP

11.2.1.4 Timeslot ISCP

'Common with the high chip rate TDD mode'

11.2.1.5 UTRA carrier RSSI

11.2.1.6 GSM carrier RSSI

11.2.1.7 SIR

'Common with the high chip rate TDD mode'

11.2.1.8 CPICH Ec/No

11.2.1.9 Physical channel BER

11.2.1.10 Transport channel BLER

'Common with the high chip rate TDD mode'

11.2.1.11 UE transmitted power

'Common with the high chip rate TDD mode'

11.2.1.12 SFN-SFN observed time difference

11.2.1.13 Observed time difference to GSM cell

11.2.1.14 Timing Advance (T_{ADV}) for 1.28 Mcps TDD

| | |
|-------------------|---|
| Definition | The 'timing advance (T_{ADV})' is the time difference $T_{ADV} = T_{RX} - T_{TX}$ where T_{RX} : <u>calculated beginning time of a certain uplink time slot with the UE timing according to the reception of a certain downlink time slot (for the timing it is assumed that the time slots within a sub-frame are scheduled like given in the frame structure described in 25.221 chapter 6.1)</u> T_{TX} : <u>time of the beginning of the same uplink time slot by the UE (for the timing it is assumed that the time slots within a sub-frame are scheduled like given in the frame structure described in 25.221 chapter 6.1)</u> |
|-------------------|---|

Note: This measurement can be used for uplink synchronisation or location services.

11.2.2 UTRAN measurement abilities

11.2.2.1 RSCP

'Common with the high chip rate TDD mode'

11.2.2.2 Timeslot ISCP

'Common with the high chip rate TDD mode'

11.2.2.3 RSSI

11.2.2.4 SIR

'Common with the high chip rate TDD mode'

11.2.2.5 Physical channel BER

'Common with the high chip rate TDD mode'

11.2.2.6 Transport channel BLER

'Common with the high chip rate TDD mode'

11.2.2.7 Transmitted carrier power

'Common with the high chip rate TDD mode'

11.2.2.8 Transmitted code power

'Common with the high chip rate TDD mode'

11.2.2.9 RX Timing Deviation

[additional measurements for 1.28 Mcps TDD:](#)

11.2.2.9.1 Received SYNC-UL Timing Deviation for 1.28 Mcps TDD

| | |
|-------------------|--|
| Definition | <p>'Received SYNC-UL Timing Deviation' is the time difference</p> $UpPCH_{POS} = UpPTS_{Rxpath} - UpPTS_{TS}$ <p><u>Where</u> <u>UpPTS_{Rxpath}</u>: time of the reception in the Node B of the SYNC-UL to be used in the uplink synchronization process <u>UpPTS_{TS}</u>: time instance two symbols prior to the end of the DwPCH according to the Node B internal timing</p> <p>UE can calculate Round Trip Time (RTT) towards the UTRAN after the reception of the FPACH containing UpPCH_{POS} transmitted from the UTRAN.</p> <p>Round Trip Time RTT is defined by</p> $RTT = UpPCH_{ADV} + UpPCH_{POS} - 8 * 16 T_c$ <p><u>Where</u> <u>UpPCH_{ADV}</u>: the amount of time by which the transmission of UpPCH is advanced in time relative to the end of the guard period according to the UE Rx timing.</p> |
|-------------------|--|

Annex A (informative): Monitoring GSM from low chip rate TDD: Calculation Results

[Description:]

This paper gives some general description about how to monitor GSM from the low chip rate TDD.

[Rationale:]

A.1 Low data rate traffic using 1 uplink and 1 downlink slot

NOTE: The section evaluates the time to acquire the FCCH if all idle slots are devoted to the tracking of a FCCH burst, meaning that no power measurements is done concurrently. The derived figures are better than those for GSM. The section does not derive though any conclusion. A conclusion may be that the use of the idle slots is a valid option. An alternative conclusion may be that this is the only mode to be used, removing hence the use of the slotted frames for low data traffic or the need for a dual receiver, if we were to considering the monitoring of GSM cells only, rather than GSM, TDD and FDD.

If a single synthesiser UE uses only one uplink and one downlink slot, e.g. for speech communication, the UE is not in transmit or receive state during 5 slots in each frame. According to the timeslot numbers allocated to the traffic, this period can be split into two continuous idle intervals A and B as shown in the figure below.

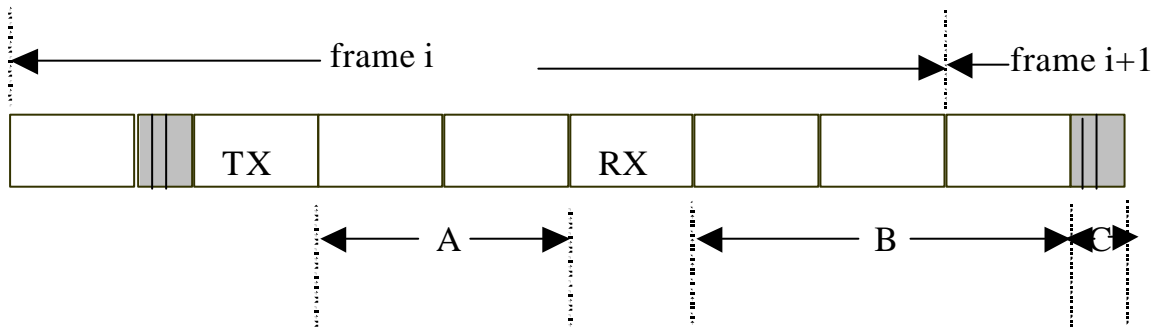


Figure A.1: Possible idle periods in a subframe with two occupied timeslots

A is defined as the number of idle slots between the Tx and Rx slots and B the number of idle slots between the Rx and Tx slots. It is clear that $A+B=5$ time slots and C is equal to the $DwPTS+GP+UpPTS$.

In the scope of low cost terminals, a [0.5] ms period is supposed to be required to perform a frequency jump from low chip rate TDD to GSM and vice versa. This lets possibly two free periods of $A*Ts-1$ ms and $B*Ts+C-1$ ms during which the mobile station can monitor GSM, Ts being the slot period.

Following table evaluates the average synchronisation time and maximum synchronisation time, where the announced synchronisation time corresponds to the time needed to find the FCCH. The FCCH is supposed to be perfectly detected which means that it is entirely present in the monitoring window. The FCCH being found the SCH location is unambiguously known from that point. All the 5 idle slots and the $DwPTS+GP+UpPTS$ are assumed to be devoted to FCCH tracking and the UL traffic is supposed to occupy the time slot 1.

Table A.1: example- of average and maximum synchronisation time with two busy timeslots per frame and with 0.5 ms switching time

| Downlink time slot number | Number of free TS in A | Number of free TS in B | Average synchronisation time (ms) | Maximum synchronisation time (ms) |
|---------------------------|------------------------|------------------------|-----------------------------------|-----------------------------------|
| 0 | 5 | 0 | 83 | 231 |
| 2 | 0 | 5 | 75 | 186 |
| 3 | 1 | 4 | 98 | 232 |
| 4 | 2 | 3 | 185 | 558 |
| 5 | 3 | 2 | 288 | 656 |
| 6 | 4 | 1 | 110 | 371 |

(*) All simulations have been performed with a random initial delay between GSM frames and low chip rate TDD subframes.

Each configuration of TS allocation described above allows a monitoring period sufficient to acquire synchronisation.

A.1.1 Higher data rate traffic using more than 1 uplink and/or 1 downlink TDD timeslot

The minimum idle time to detect a complete FCCH burst for all possible alignments between the GSM and the 1.28Mcps TDD frame structure (called 'guaranteed FCCH detection'), assuming that monitoring happens every sub-frame, can be calculated as follows ($t_{FCCH} =$ one GSM slot):

$$t_{\min, \text{ guaranteed}} = 2 \cdot t_{\text{synth}} + t_{FCCH} + \frac{5\text{ms}}{13} + 2 \cdot t_{\text{synth}} + \frac{25\text{ms}}{26}$$

- (e.g for $t_{\text{synth}}=0\text{ms}$: 2 1.28Mcps TDD **consecutive** idle timeslots needed, for $t_{\text{synth}}=0.3\text{ms}$: 3 slots (or 2 slots and the DwPTS+GP+UpPTS), for $t_{\text{synth}}=0.5\text{ms}$: 3 slots, for $t_{\text{synth}}=0.8\text{ms}$: 4 slots). Under this conditions the FCCH detection time can never exceed the time of 660ms.
- (For a more general consideration t_{synth} may be considered as a sum of all delays before starting monitoring is possible).
- For detecting SCH instead of FCCH (for a parallel search) the same equation applies.
- In the equation before the dual synthesiser UE is included if the synthesiser switching time is 0ms.

Table A.1.1: FCCH detection time for a single synthesizer UE monitoring GSM from 1.28Mcps TDD every sub-frame

| Occupied Slots | Cases | AVERAGE FCCH detection time in ms | MAXIMUM FCCH detection time in ms |
|----------------|-------|-----------------------------------|-----------------------------------|
| 2 | 21 | 136.625 | 660.785 |
| 3 | 35 | 188.451 | 660.785 |
| 4 | 35 | 231.115 | 660.785 |
| 5 | 21 | - | - |
| 6 | 7 | - | - |
| 7 | 1 | - | - |

The result in the above table is based on the following assumption:

- ?? A single synthesizer is used.
- ?? A [0.5] ms period is supposed to be required to perform a frequency jump from 1.28Mcps TDD to GSM and vice versa.
- ?? For a given number of occupied slots in the TDD mode all possible cases of distributions of these occupied TDD slots are considered (see 'cases'). For every case arbitrary alignments of the TDD and the GSM frame structure are taken into account for calculating the average FCCH detection time (only these cases are used which guarantee FCCH detection for all alignments; only the non-parallel FCCH search is reflected by the detection times in the above table).

The term 'occupied slots' means that the UE is not able to monitor in these TDD slots.

For a synthesiser switching time of one or one half TDD timeslot the number of needed consecutive idle TDD timeslots is summarized in the table below:

Table A.1.2: Link between the synthesiser performance and the number of free consecutive Timeslots for guaranteed FCCH detection, needed for GSM monitoring

| <u>One-way switching time for the synthesiser</u> | <u>Number of free consecutive 1.28Mcps TDD timeslots needed in the sub-frame for a guaranteed FCCH detection</u> |
|---|--|
| <u>1 Timeslot (=864 chips)</u> | <u>4</u> |
| <u>0.5 Timeslot (=432 chips)</u> | <u>3</u> |
| <u>0 (dual synthesiser)</u> | <u>2</u> |

The minimum idle time to detect a complete FCCH burst for all possible alignments between the GSM and the TDD frame structure (called 'guaranteed FCCH detection'), assuming that monitoring happens every TDD frame, can be calculated as follows (t_{FCCH} = one GSM slot):

— (e.g for t_{synth} = 0ms: 2 low chip rate TDD ~~consecutive~~ idle timeslots needed, for t_{synth} = 0.3ms: 3 slots (or 2 slots and the DwPTS+GP+UpPTS), for t_{synth} = 0.5ms: 3 slots, for t_{synth} = 0.8ms: 4 slots). Under this conditions the FCCH detection time can never exceed the time of 660ms.

— (For a more general consideration t_{synth} may be considered as a sum of all delays before starting monitoring is possible).

— For detecting SCH instead of FCCH (for a parallel search) the same equation applies.

— In the equation before the dual synthesiser UE is included if the synthesiser switching time is 0ms.

Considering about the frame structure of the low chip rate TDD, there are total 7 timeslot in each frame that can be used as data traffic. If more than 1 uplink and/or 1 downlink TDD timeslot are used for data traffic, that means it will occupy at least 3 time slot, equal to $0.675 \times 3 = 2.205$ ms. And more time slots for traffic data means more switching point are needed to switch between the GSM and the low chip rate TDD. As it was mentioned above, each switching will take 0.5ms. As a result, the idle time left for monitoring the GSM will be very little. So monitoring GSM from low chip rate TDD under this situation will be considered in the future. It will need more carefully calculation and simulation.

For a synthesiser switching time of one or one half TDD timeslot the number of needed consecutive idle TDD timeslots is summarized in the table below:

Table A.2: Link between the synthesiser performance and the number of free consecutive TSs for guaranteed FCCH detection, needed for GSM monitoring

| <u>One-way switching time for the synthesiser</u> | <u>Number of free consecutive TDD timeslots needed in the frame for a guaranteed FCCH detection</u> |
|---|---|
| | |

| | |
|---------------------------------|--------------|
| 1 TS (=864 chips) | 4 |
| 0.5 TS (=432 chips) | 3 |
| 0 (dual synthesiser) | 2 |

[Explanation difference:]

Due to the different operating bandwidth and the different frame structure, some measurement method about how to monitor GSM are different between the high and low chip rate TDD.

12 Performance analysis of the low chip rate

Simulation assumptions

~~Note: Some of the assumptions may need further clarifications. Other simulations may also be needed to clarify some of the special features of the low chip rate TDD.~~

Calculation of the E_b/N_0

Intercell interference is modeled as white Gaussian noise. In the following, bit error rates (BER) are given as a function of the average E_b/N_0 (or as a function of average C/I) in dB (E_b is the energy per bit and N_0 is the one-sided spectral noise density) with the intracell interference, i.e. the number K of active users per time slot as a parameter. The relation between the E_b/N_0 and the carrier to interference ratio C/I, with C denoting the carrier power per CDMA code and with I denoting the intercell interference power, is given by

$$\frac{C}{I} \approx \frac{E_b}{N_0} \frac{R_c}{B} \frac{\log_2 M}{Q T_c} \quad (1.1)$$

with

R_c the rate of the channel encoder (depends on the service),

M the size of the data symbol alphabet (4),

B the user bandwidth

Q the number of chips per symbol (16) and

T_c the chip duration (0.24444-78125 ?s).

The expression $\log_2 M$ is the number of bits per data symbol and $QxT_c/\log_2 M$ is the bit duration at the output of the encoder. One net information bit is transmitted in a duration of $QxT_c/(R_c \times \log_2 M)$. Therefore, (1.1) is equivalent to $C/I = (E_b/T_b)/(N_0 \times B)$, i.e., $C = E_b/T_b$ and $I = N_0 \times B$ with T_b the duration of a net information bit. The carrier to interference ratio per user is K_c times the carrier to interference ratio per CDMA code, with K_c denoting the number of CDMA codes per time slot per user.

The E_b/N_0 (as the C/I) is calculated at the antenna connector of the antenna elements.

Channel model

In case smart antennas are used the channel model is like the vehicular A model used for ITU and ETSI 30.03. The channel model has been adapted to the smart antenna environment such that the directions of arrival (DOA) for the multipaths are uniformly distributed.

Antenna array

Figure 1 shows the circular array used in smart antenna simulations. The circular array is suitable for omnidirectional cell design. Let the array be composed of N antenna elements, where the first (reference) antenna element is located at the position of $(R, 0)$, and the k -th element is located at the location of $(R \cos 2k\pi/N, R \sin 2k\pi/N)$ in circular array.

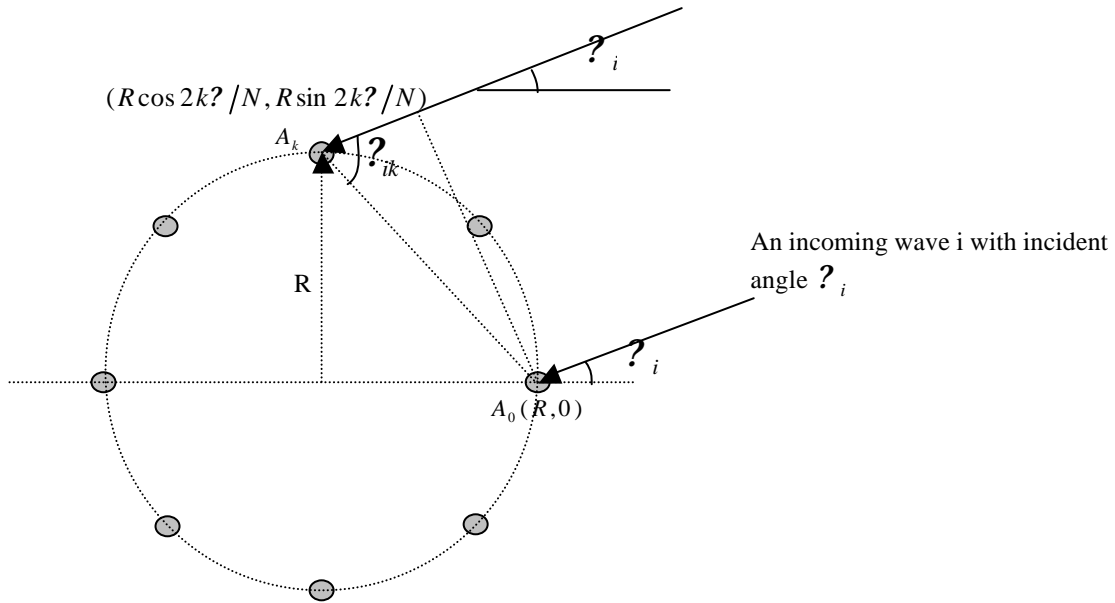


Figure . The geometric illustration for circular antenna array

Then, when an incoming wave i from the direction of θ_i , for circular array, the differential optical distance (D_{ik}) between the first and the k -th antenna element will be

$$D_{ik} = R \cos \theta_{ik} [2(1 - \cos 2k\pi/N)]^{1/2}$$

where R is the radius of the circular array;

$$k = 1, 2, \dots, N - 1;$$

N is the total number of antenna element.

The incident wave comes from the direction of θ_i as shown in Figure 1, and

$$\theta_{ik} = \theta_i - (1/2) \cdot k/N$$

Let's denote $S_{kj}(n)$ as the Rx signal at the k -th antenna element from the i -th path of the j -th UE, then

$$S_{kj}(n) = \sum_i a_{ji}(n) \exp[j(\theta_i - \theta_{kji})] \quad \text{for the } n\text{-th sampling}$$

where, $a_{ji}(n)$ is the amplitude of the i -th path from the j -th UE;

τ_{ji} is the time delay of the i -th path from the j -th UE;

ϕ_{kji} is the phase different between the k -th element and the reference element for the i -th path from the j -th UE:

$$\phi_{kji} = 2\pi D_{jik} / \lambda$$

and D_{jik} is the differential optical distance between the first and the k -th antenna element for the i -th path from the j -th UE;

ω is the angle frequency and λ is the wavelength.

Simulation results

Simulation for BCH

Simulation parameters:

Channel model: vehicular A (Speed 120km/h)

Coding: CC ,coding rate =1/3

Link: downlink

Power control: No

SF: 16

Number of timeslots: 1

Codes per slot: 2

L1 control signals: No

TFCI: No

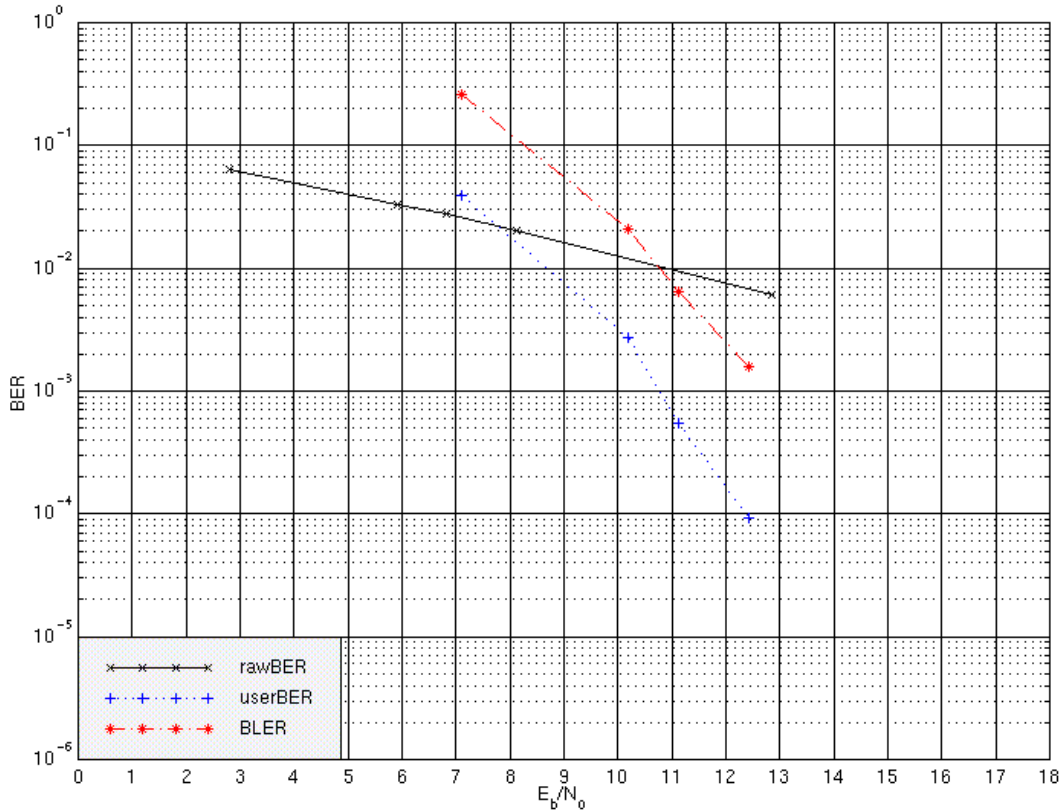


Figure : BER vs. Eb/N0 for BCH

Multiplexing of 12.2kbps data and 2.4kbps data

For 2.4kbps data path

Simulation parameters:

Channel model: vehicular A with Smart antenna (Speed 120km/h)

Coding:CC ,coding rate =1/2

Link: Uplink

Power control: No

SF:16

Number of users: 1

Number of time slot: 1

Codes per time slot: 3

L1 control signals: No

TFCI: No

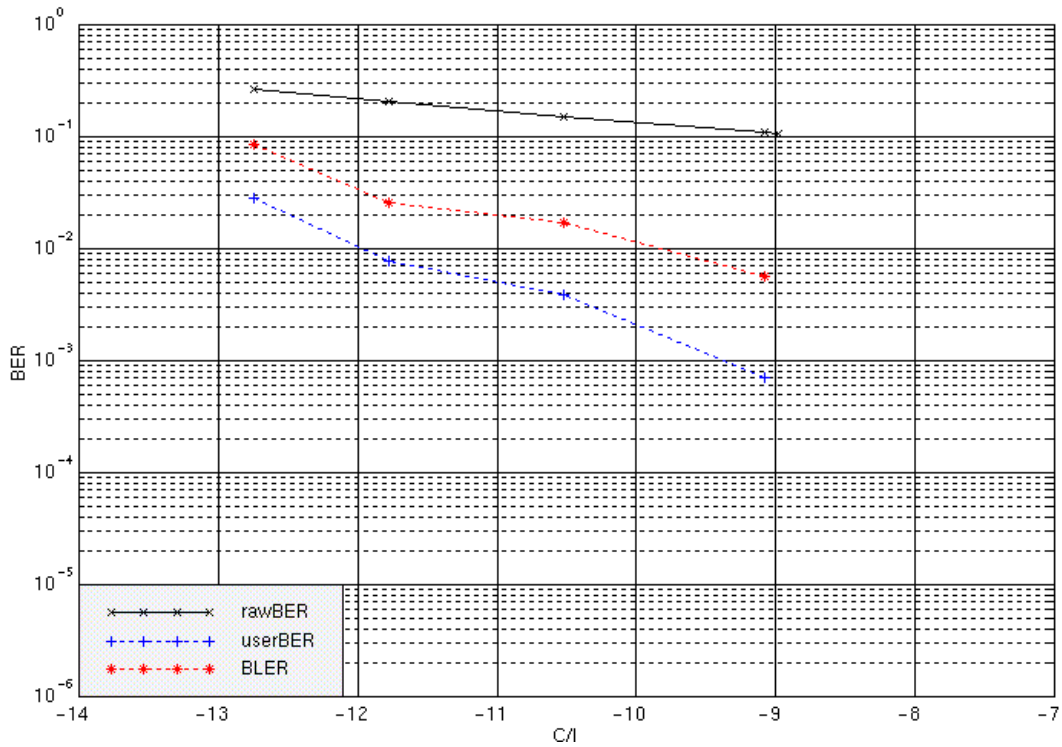


Figure : BER vs. C/I for 2.4kbps path

For 12.2kbps data path

Simulation parameters:

Channel model: vehicular A with Smart antenna (Speed 120km/h)

Coding: CC ,coding rate=1/2,class C

CC, coding rate=1/3,class A and B

Link: Uplink

Power control: No

SF:16

Number of users: 1

Number of time slot: 1

Codes per time slot: 3

L1 control singals: 4 bits.

TFCI: 16 bits(8 bits per subframe).

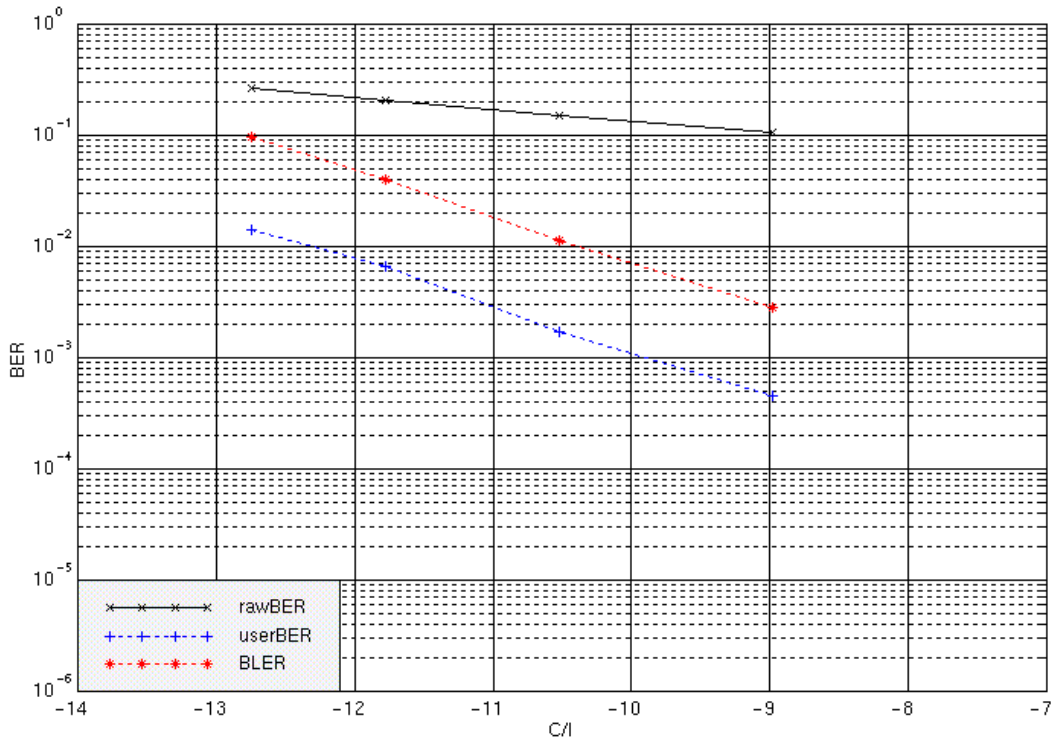


Figure : BER vs. C/I for 12.2kbps path

Simulation for 384kbps

Simulation parameters:

Channel model: vehicular A with Smart antenna (Speed 120km/h)

Coding: Turbo coding ,coding rate 1/3. Convolutional code with code rate 1/3 is optional for 384kbps packet data.

Link: Uplink

Power control: No

SF:16

Number of users: 1

Number of time slot: 4

Codes per time slot: 16

L1 control signals: 4 bits.

TFCI: 16 bits

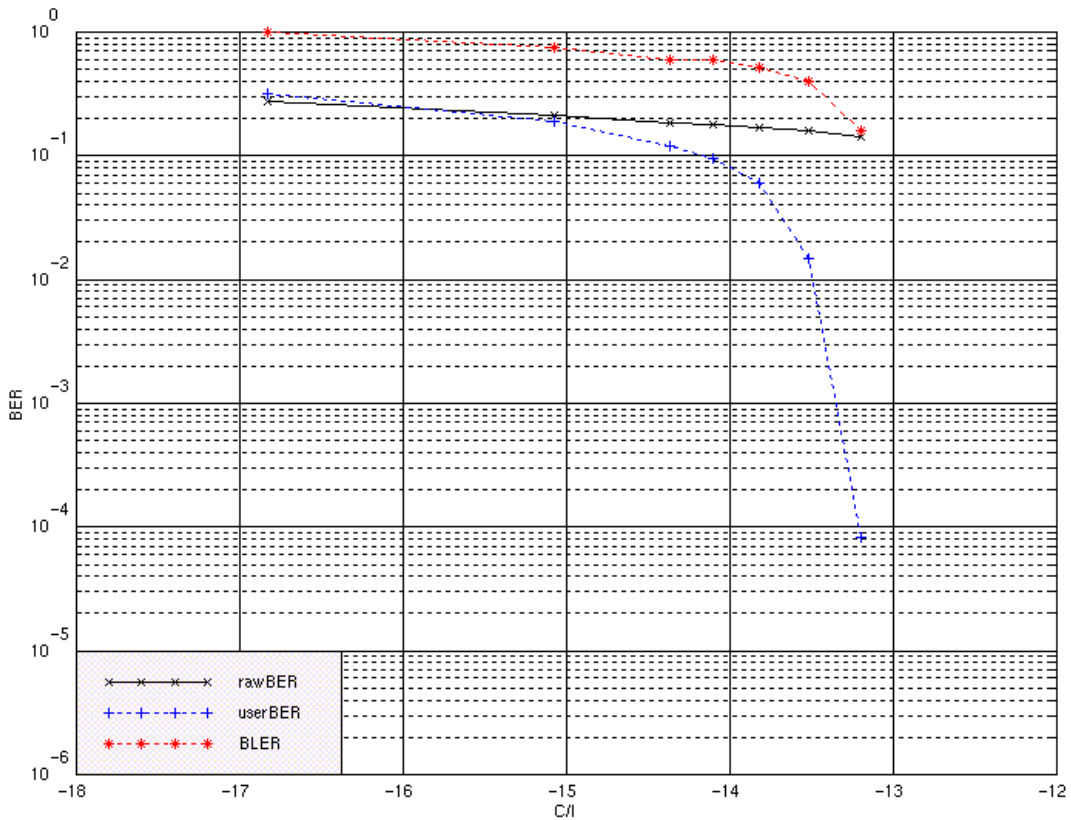


Figure BER vs. C/I for 384kbps

Simulation for 2Mbps

The simulations for the indoor environments in uplink are considered. The channel model is compatible with the one in UMTS 30.03. The main parameters are listed as following:

Parameters

Service: 2 Mbps service

Channel model: Indoor A

Channel coding: None

Modulation/Demodulation: 8PSK;

Power Control: Ideal power control

Frame structure: 5ms

Number of time slot: 5

Codes per time slot: 16

Simulation Results

The following table and figures in next pages present the simulation results for 2 Mbps service without channel coding considered.

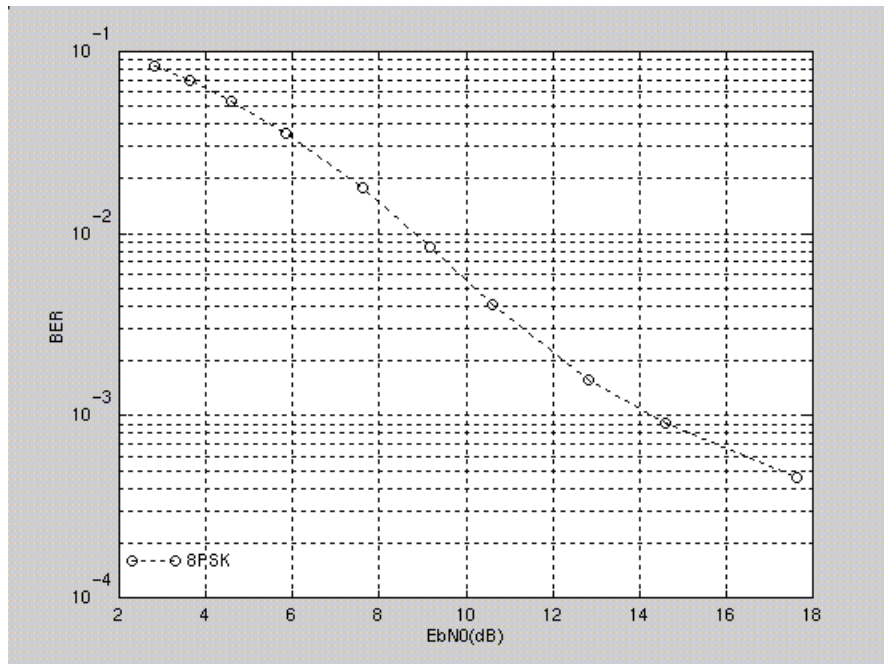


Figure : BER vs. EbNo for 2 Mbps service

(without coding using 8PSK modulation scheme)

13 Examples of service mapping

B.1 BCH

~~Note: Other means for BCH indication are under consideration.~~

Table B.1 Parameters for BCH

| | |
|----------------------|--|
| Transport block size | 246 bits +1bit (*) |
| CRC | 16 bits |
| Coding | CC, coding rate = 1/3 This has to be included in table 1 in 25.222 4.2.3. |
| TTI | 20 ms |
| Midamble | 144 chips |
| Codes and time slots | SF = 16 2 codes x 1 time slot |
| TFCI | 0 bit |
| L1 control signals | 0 bit |

~~Note: The example is applied to BCH without multiplexing PCH and FACH.~~

~~*: 1 extra bit in transport block is used for BCH indication.~~

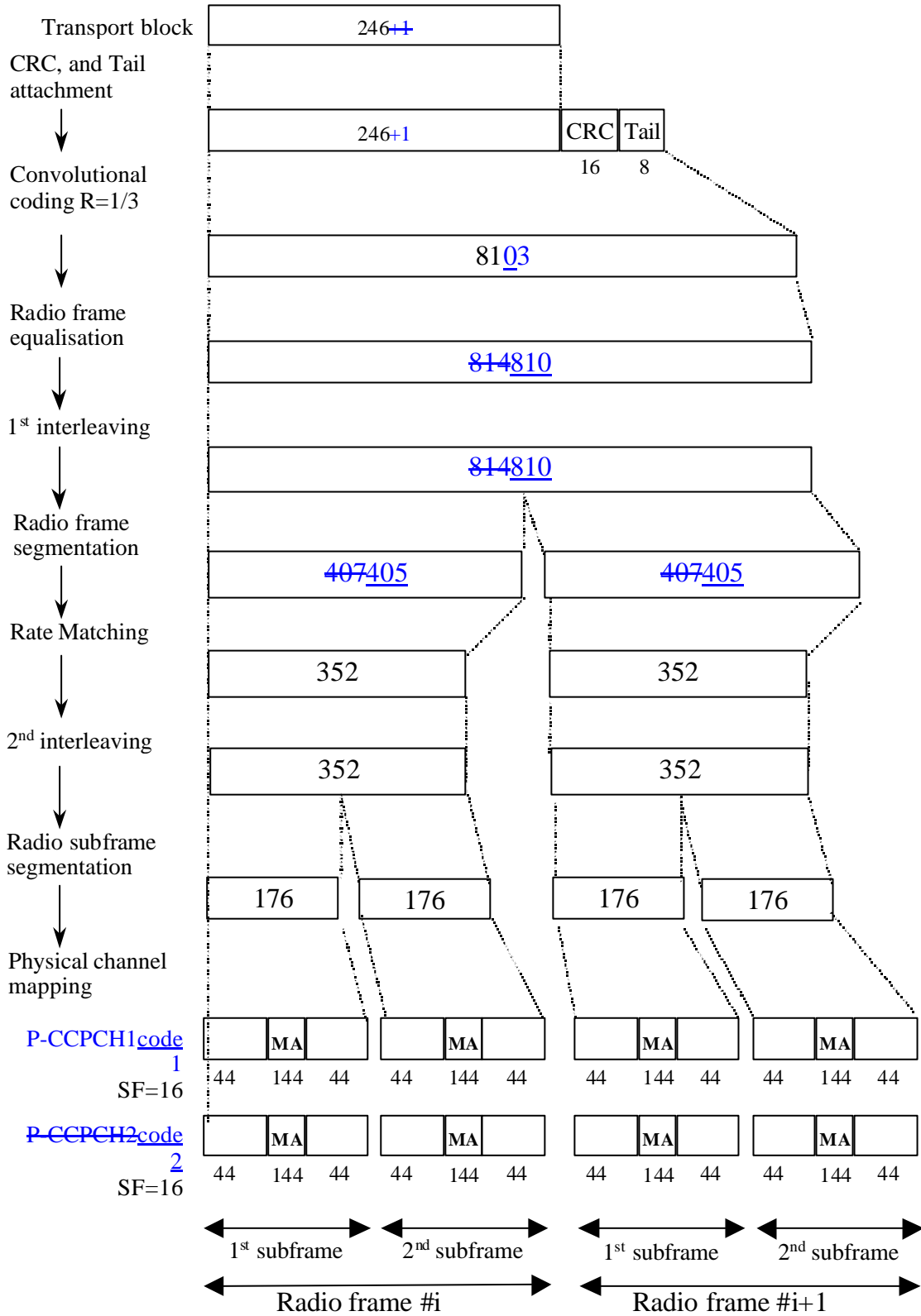


Figure B.1 Service mapping for BCH

B.2 2.4kbps data for downlink

Table B.2 Parameter examples for 2.4kbps data

| | |
|--------------------------|-----------------------|
| Transport block set size | 48 bits |
| CRC | 16 bits |
| Coding | CC, coding rate = 1/2 |
| TTI | 20 ms |

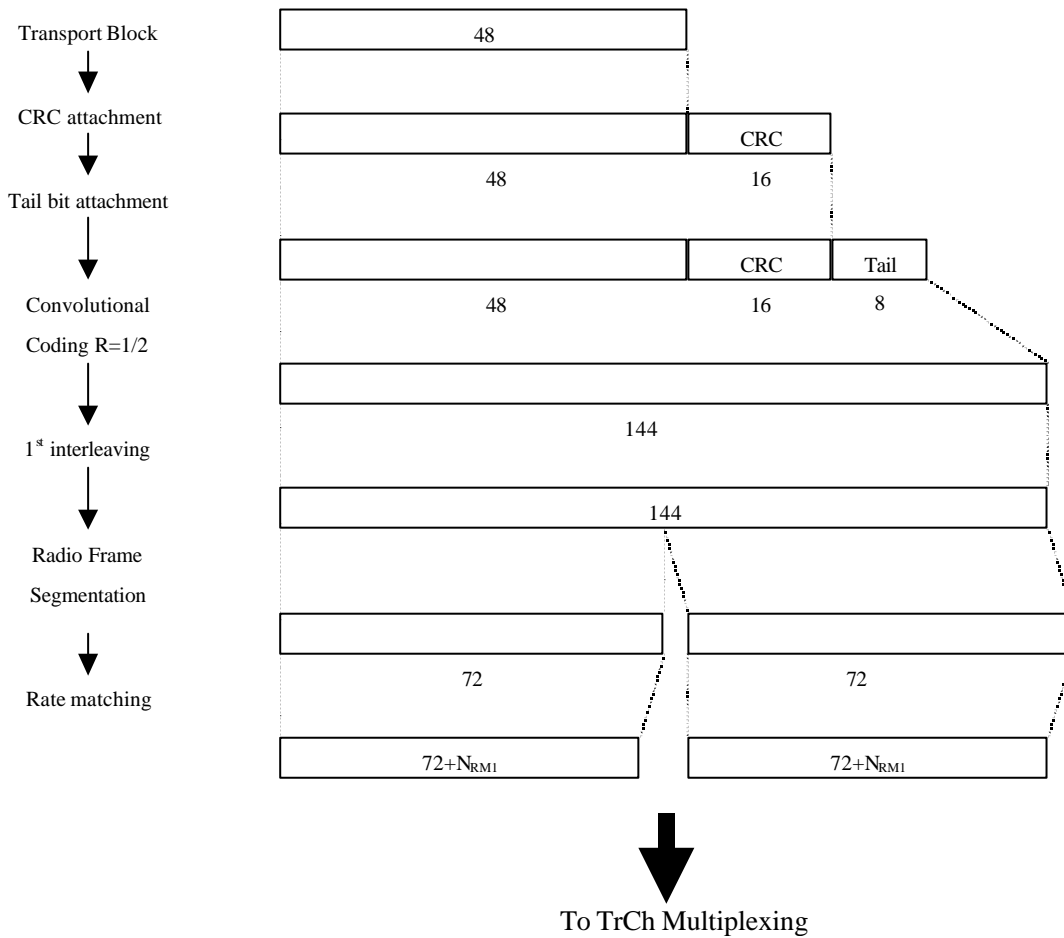


Figure B.2 Channel coding for 2.4kbps data

B.3 12.2kbps data for downlink

Note: this example can be applied to AMR speech

Table B.3 Parameter examples for 12.2kbps data

| | |
|----------------------|---|
| Number of TrChs | 3 |
| Transport block size | 81bits(TrCh#1) 103bits(TrCh#2) 60bits(TrCh#3) |
| CRC | 12(Only for TrCh#1) |
| Coding | CC, coding rate = 1/2, class B, C CC, coding rate = 1/3, class A |
| TTI | 20 ms |
| Midamble | 144 chips |
| Codes and time slots | SF = 16 2 codes x 1 time slots |
| TFCI | 16bits (8 bits in each subframe) |
| L1control signals | 4bits |

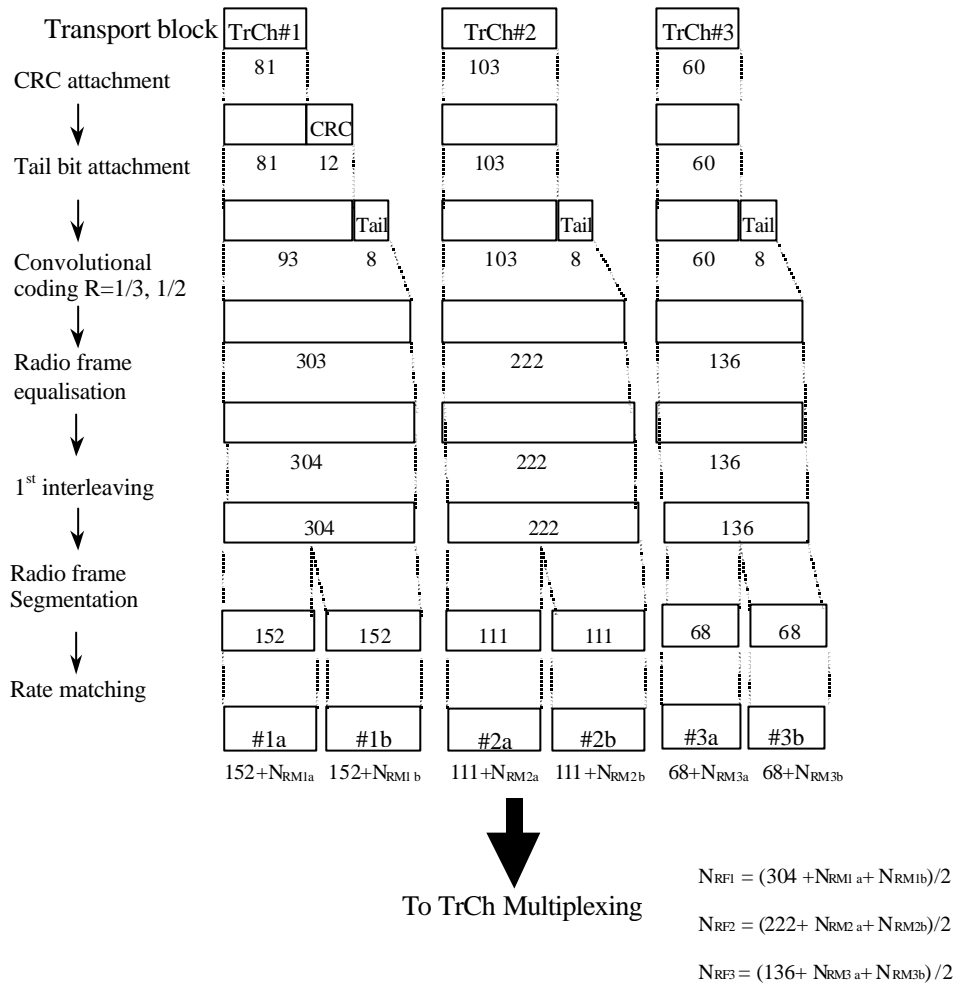
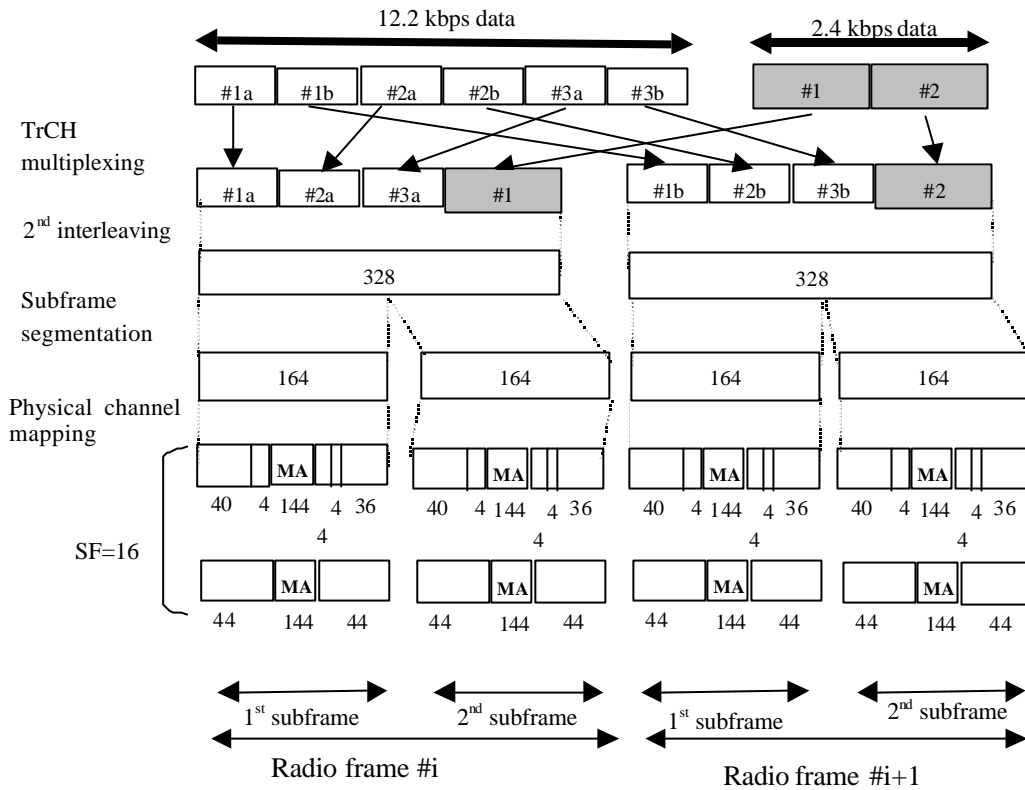


Figure B.3 Channel coding for 12.2kbps AMR

B.3-1 Example for multiplexing of 12.2 kbps data and 2.4 kbps data



B.4 384kbps packet data for downlink

Table B.4 Parameter examples for 384kbps packet data

| | |
|--------------------------|------------------------------------|
| The number of TrChs | 1 |
| Transport block set size | 3840*B bits(B=0,1,2) |
| Segmentation C | 1 (B = 0, 1) or 2 (B = 2) |
| CRC | 16 bits |
| Coding | Turbo coding, coding rate = 1/3 |
| TTI | 20 ms |
| Midamble | 144chips |
| Codes and time slots | SF = 16 16 codes x 4 time slots |
| TFCI | 16bits |
| L1 signals | 4 bits |

~~1.28Mcps functionality for UTRA TDD Physical Layer (3GPP TS 25.101 Action 1) (2000-07)~~
~~UTRA TDD Physical Layer (3GPP TS 25.101) (2000-07)~~

~~Note1: 13codes*4 time slots+12codes*1 time slot is under considered.~~

~~Note2~~Note1: Convolutional code with code rate 1/3 is optional for 384kbps packet data if UE capability supports it. B=2 for the figure B.4.

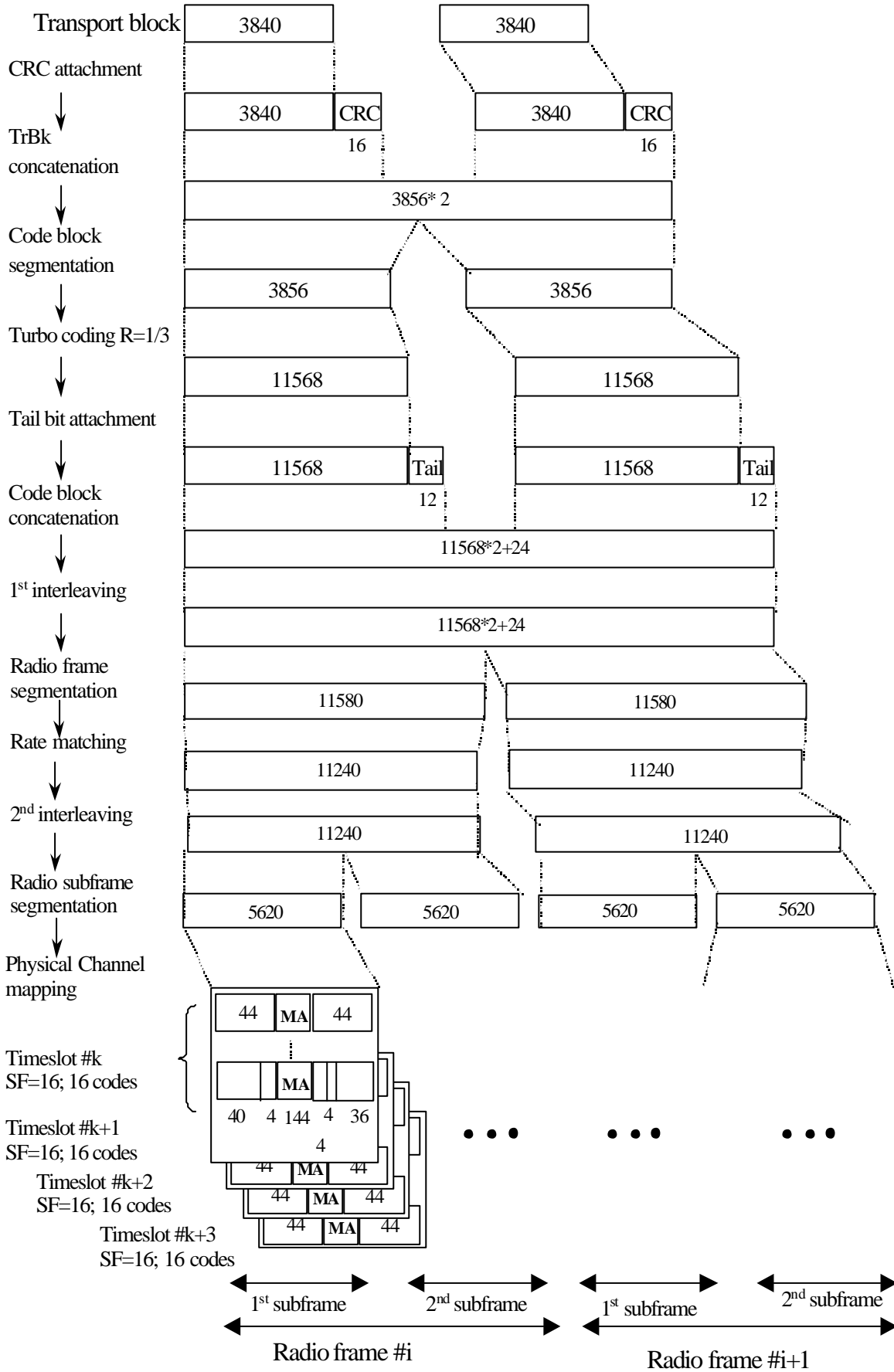


Figure B.4 Service mapping for 384kbps packet data

B.5 2Mbps packet data for downlink

In low chip rate TDD optional, 2Mbps service is only used in some special environment. E.g. Indoor environment

Table B.5 Parameter examples for 2Mbps packet data

| | |
|----------------------|----------------------------------|
| Transport block size | 20480*B bits(B=0,1) |
| CRC | 24 bits |
| Coding | no |
| TTI | 10 ms |
| Midamble | 144 chips |
| Codes and time slots | SF = 1 1 codes x 5 time slots |
| TFCI | 24bits |
| L1control signals | 6bits |

Note1: 8PSK has to be used to provide 2Mbps packet data service. B=1 for the figure B.5.

Note2: other mapping schemes, e.g. using more resource unit and using some channel coding, or increasing the number of the code block segmentation to reduce BLER are considered.

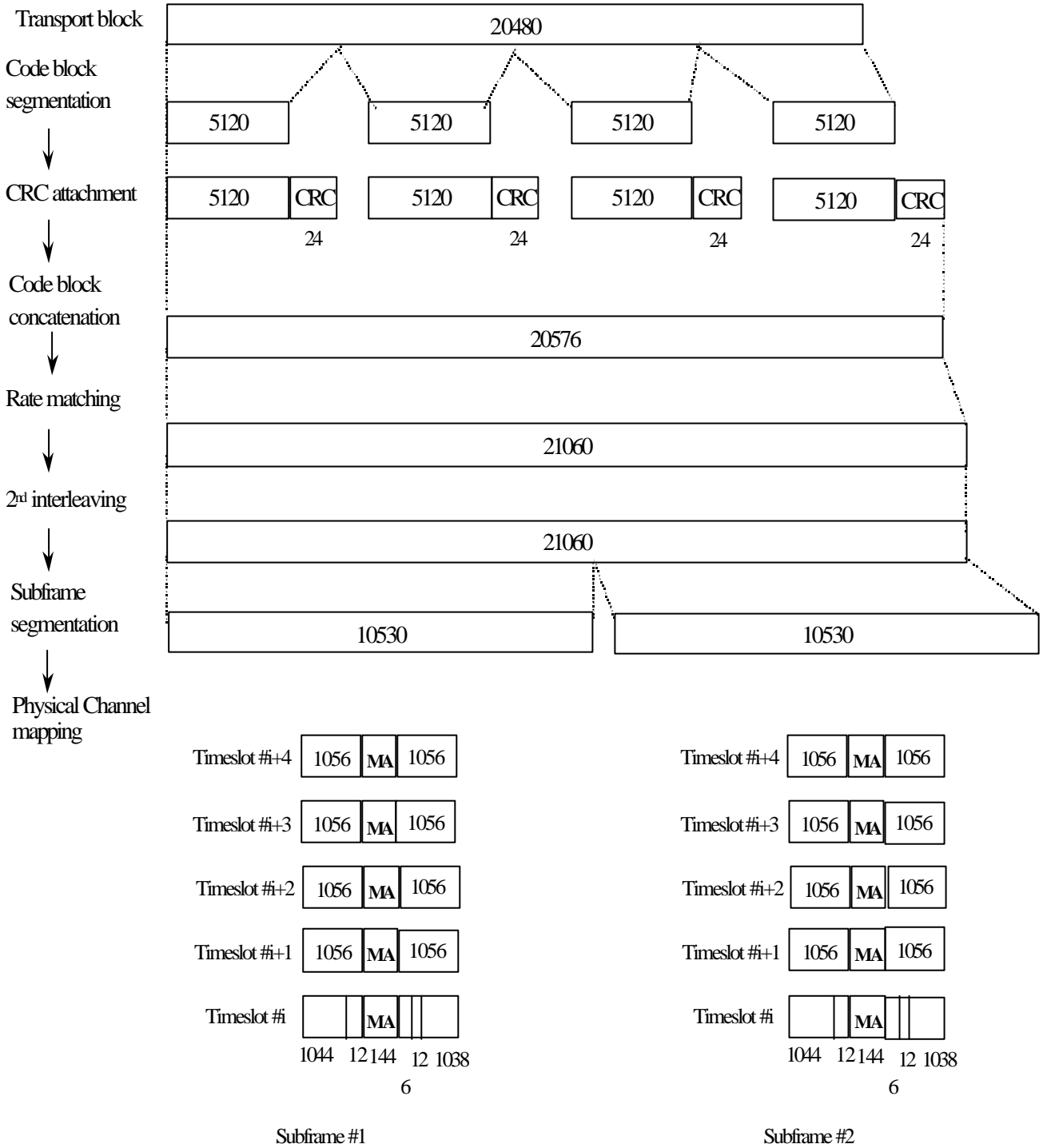


Figure B.5 Service mapping for 2Mbps packet data

14 History

| Document history | | |
|------------------|--------------|--|
| V0.0.1 | January 2000 | Created in WG#10 in Beijing, Table of contents approved, R1-00-149 |
| V0.0.2 | March 2000 | New structure created according to the comments at the WG1#11, San Diego |
| V0.0.3 | March 2000 | Document renamed according to the conclusions in RAN#8, Madrid |
| V0.0.4 | April 2000 | Updated according to the conclusions in WG1#12, Seoul |
| V0.1.0 | April 2000 | WG1 approved version |
| V0.2.0 | May 2000 | Updated according to the conclusions in WG1#13 and approved, Tokyo |
| V0.2.1 | June 2000 | Updated according to the AH on the NB-TDD (R1-00-0840) |
| V1.0.0 | June 2000 | Approved version in the NB-TDD AH (R1-00-0841) |
| V1.0.1 | July 2000 | Draft for approval after some new proposals added |
| V1.1.0 | July 2000 | Approved version at WG1#14, Oulu |

Editor information:

Mirko Aksentijevic

Nokia Networks

Email: mirko.aksentijevic@nokia.com