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TSG-RAN Working Group 2 (Radio L2 and Radio L3) R2-010752
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Source: **TSG-RAN WG2**

To: **TSG-RAN WG3**

Cc: **TSG-RAN WG1**

Title: **LS on Delay times in the control plane**

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In RAN2 there have been discussions on the benefits of Gated DPCCH Transmission (Gating) over using CELL_FACH state. The gains of Gating over using CELL_FACH are being discussed from the point of signalling load and delay aspects. While Gating requires a physical channel reconfiguration with two informations: Gating rate and direction, using CELL_FACH requires a switching from CELL_FACH to CELL_DCH in order to transfer packet data on DSCH. There was, therefore, a concern that using CELL_FACH requires much more signalling load and delay such as physical channel synchronization, FACH scheduling to set up DCH channel again, and processing delay to reconfigure DCH on Node B than Gating. RAN2 would like to kindly ask that RAN3 answer the following questions.

1. Regarding delay for switching from CELL_FACH to CELL_DCH the following values are assumed by Samsung Electronics:

- **Branch delay**
  - **RNC ✍ Node B: 14.2 ms**
  - **Node B ✍ RNC: 27.2 ms**
  - **RNC ✍ UE: 49.2 ms**
  - **UE ✍ Node B: 62.2 ms**

  + Tcontrol: Additional processing delay in the control plane (0~90 ms)
- **DSCH resource scheduling (50 ms)**
- **Processing delay (50 ms)**
- **FACH scheduling (100 ms)**
- **Physical Channel Synch. (150 ms)**

The branch delay is estimated as a value based on TR 25.932 Delay Budget within the Access Stratum which guides delay values in the user plane. The branch delay in the control plane is assumed to have

0~90 ms of additional delay to those in the user plane. However, there was a concern that delay values in the control plane is much longer than those in the user plane.

RAN2 would like to ask RAN3 whether the delay value ranges of **14.2~104.2 ms** for transferring message from RNC to Node B and **27.2~117.2 ms** from Node B to RNC in the control plane are acceptable or not. If not acceptable, what values are reasonable for the control plane?

2. From the viewpoint of Iub/Iur, what overheads are additionally required for switching from CELL_FACH to CELL_DCH compared to Gating. In RAN WG2's discussion, regarding delay, 50 ms of the processing delay for the reconfiguration of Node B and 100 ms of delay for the FACH scheduling were issued.

Please find attached contributions of the comparison between Gating and Using CELL_FACH.


R2-010128.doc


R2-010728.doc