TSG-RAN Working Group 1 meeting #17
Stockholm, Sweden
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Agenda item: Release 2000 issues / AH22
Source: Nokia
Title: Further clarifications on outer loop power control during DPCCH gating

Document for: Discussion & Decision

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1. Introduction

The use of outer loop power control was discussed against the ealier finding that DPCCH BER itself can not be used for basis of the outer loop SIR target adjustment. This contribution gives further clarification to the questions raised and also presents the latest developments on the outer loop in TSG RAN WG2, as reflected in section 2 from the approved WG2 CR on the topic.

2. Present outer loop power control method during DTX

The present method for outer loop power control during normal DTX, non-gating state, is that encoded CRC may transmitted with zero length TrCH block. This can be found from TS 25.212 , section 4.2.1.1, from which the relevant part is copy pasted below. If case of CRC is not present, the outer loop is frozen, as given in 25.331, see further after 25.212 section.

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If no transport blocks are input to the CRC calculation ($M_i = 0$), no CRC attachment shall be done. If transport blocks are input to the CRC calculation (M_i ? 0) and the size of a transport block is zero ($A_i = 0$), CRC shall be attached, i.e. all parity bits equal to zero.

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8.6.5.4 DCH quality target

At PhyCH establishment, the UE sets an initial downlink target SIR value based on the received IEs "DCH quality target".
The "DCH quality target" IE for a given DCH shall be used by the UE to set the target SIR for the downlink power control. in case BLER measurement is possible for this DCH. i;e.CRC exists in all transport formats in downlink TFS,

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In the chapters below it is discussed, what could be the best method for outer loop power control during gating state.

3. Possible way forward on the outer loop power control methods during gating state

- A) In case of such a transport format is not specified where zero transport format is used together with CRC, then the outerloop power control target is considered frozen with DPCCH gating as is done with normal operation as well
- B) In case CRC is attached to zero TrCH block , then the CRC on DPDCH is mapped to the active slots during the TTI in the gated frames.

This means that we need to define, that during normal gating the physical channel mapping, both in uplink and downlink, is changed so that the encoded CRC bits will be mapped only to those slots, where DPCCH is also transmitted. See the

appendix , what parts of the multiplexing diagrams would be affected, it is shown there in blue. The detailed explanation of the required changes for the alternative B are given in the next section.

4. Changes needed in the multiplexing in TS 25.212

4.1 Physical channel mapping

Relevant part of the present definition

It is defined in sections 4.2.12.1 and 4.2.12.2, physical channel mapping for uplink and downlink, that during compressed mode, bits are mapped only to certain slots of the frame.

Required changes

Similar kind of addition is needed for gating, saying that during gating, bits are mapped only to certain slots of the frame.

In uplink :
?? during normal gating mode, the bits are mapped only to those slots, where DPCCH is also transmitted.
?? during embedded mode, the bits are mapped to all slots in the frame

In downlink:
?? during normal gating mode the bits are mapped only to those slots where DPCCH is also transmitted
?? during embedded mode, the bits are mapped to all slots in the frame

Here : normal gating mode = frames where only CRCs with zero length TrCH block(s) is (are) transmitted
embedded mode =frames where at least one non-zero length TrCH block is transmitted

This means that during RX gating [2,3], in every Kth frame UE receiver needs to decode the TFCI, before it knows that in what slots the bits are mapped to. If TFCI defines that there are only zero length transport blocks in the frame, then UE knows that the bits are mapped to only certain slots of the frame. And if TFCI defines that there is at least one non-zero length transport block in the frame, then UE knows that the bits are mapped to all slots in the frame.

The similar procedure is required from NodeB in uplink, in every frame. NodeB has to use pilot energy comparison to detect whether the frame is in normal gating mode or in embedded mode. In embedded mode all the pilot fields exist. If it detects that the frame is in normal gating mode, it knows that DPDCH is transmitted in the same slots as DPCCH. If it detects that the frame is in embedded mode, then it decodes the TFCI, and decodes the data from all slots in the frame.

4.2 2nd Insertion of DTX indication bits in downlink

Relevant part of the present definition

Presently it is defined in section 4.2.9.2. "2nd insertion of DTX indication bits " that:
?? S is the number of bits from TrCH multiplexing
?? P is the number of PhCHs bits
?? R is the number of bits in one radio frame , including DTX indication bits.

Required changes:

1) In embedded mode, the same definition can be used as before. So no changes are needed.

2) During normal gating mode, R needs to be replaced by Rgating, where:
   ?? Rgating=R/3 if gating rate=1/3
   ?? Rgating=R/5 if gating rate=1/5

4.3 Rate matching in uplink

Relevant part of the present definition

Presently it is defined in section 4.2.7. "Rate matching" that:

?? $N_{data,j}$ is the total number of bits that are available for the CCTrCH in a radio frame with transport format combination j.

Required changes:

1) In embedded mode, the same definition can be used as before. So no changes needed.

2) In normal gating mode, $N_{data,j}$ needs to be replaced by $N_{data,j}^{gating}$, where:

   ?? $N_{data,j}^{gating} = N_{data,j,}$ /3 if gating rate=1/3

   ?? $N_{data,j}^{gating} = N_{data,j}$ /5 if gating rate=1/5

5. Conclusion and proposal

It is proposed that outer loop power control based on CRC attached to zero transport block will be used also during DPCCH gating, indicated as option B earlier. This is because DPCCH BER will not offer good enough performance for outer loop [1]. Depending on the network selection also case A with SIR target frozen during gating may be applied when transport blocks with zero length and CRC do not exist.

This will mean that DPCCH gating concept will actually depending on the parameter setting correspond to DPCCH+DPDCH gating, since both DPCCH and DPDCH will contain transmitted bits only in certain slots of the frame.

The proposed TR text on issue is given in a separate contribution, R1-00-1461.

References

[1] R4-00-0013, Nokia, " Downlink Outer Loop Power Control based on physical channel BER" , San Jose, US , January 17-21, 2000.

[2] R1-00-1079, Nokia, "Proposal of using both tx and rx gating " , Berlin, Germany , August 22-25, 2000.

[3] R1-00-1338, Nokia, "Further clarifications on RX gating " , Stockholm, Sweden , November 21-24, 2000.

[4] R2-00-2459, Nortel Networks, "DCH Quality Target", CR 25.331-628, November 2000

Annex 1: Blocks where changes are needed in TS 25.212.

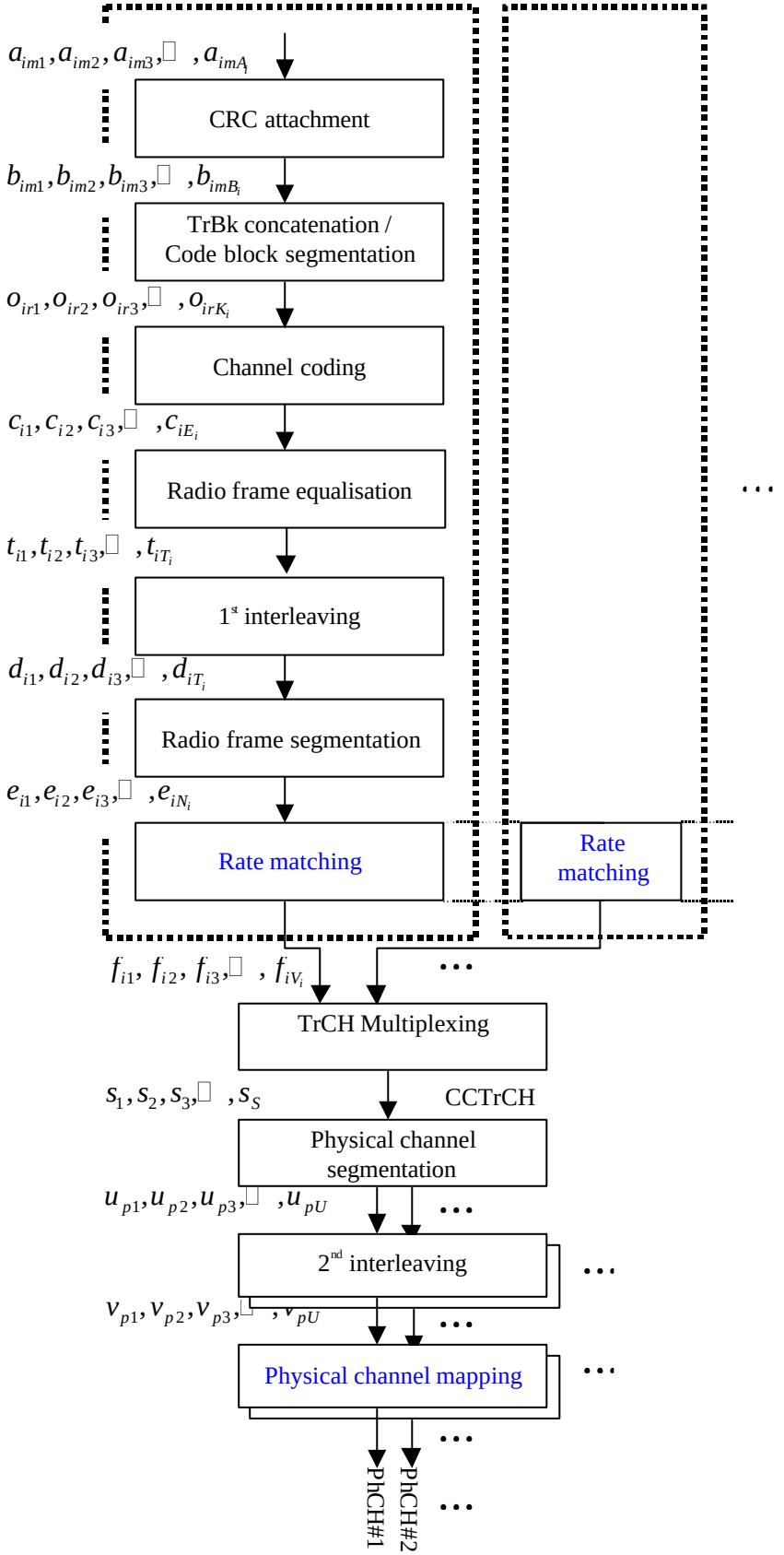

Figure 1: Transport channel multiplexing structure for uplink

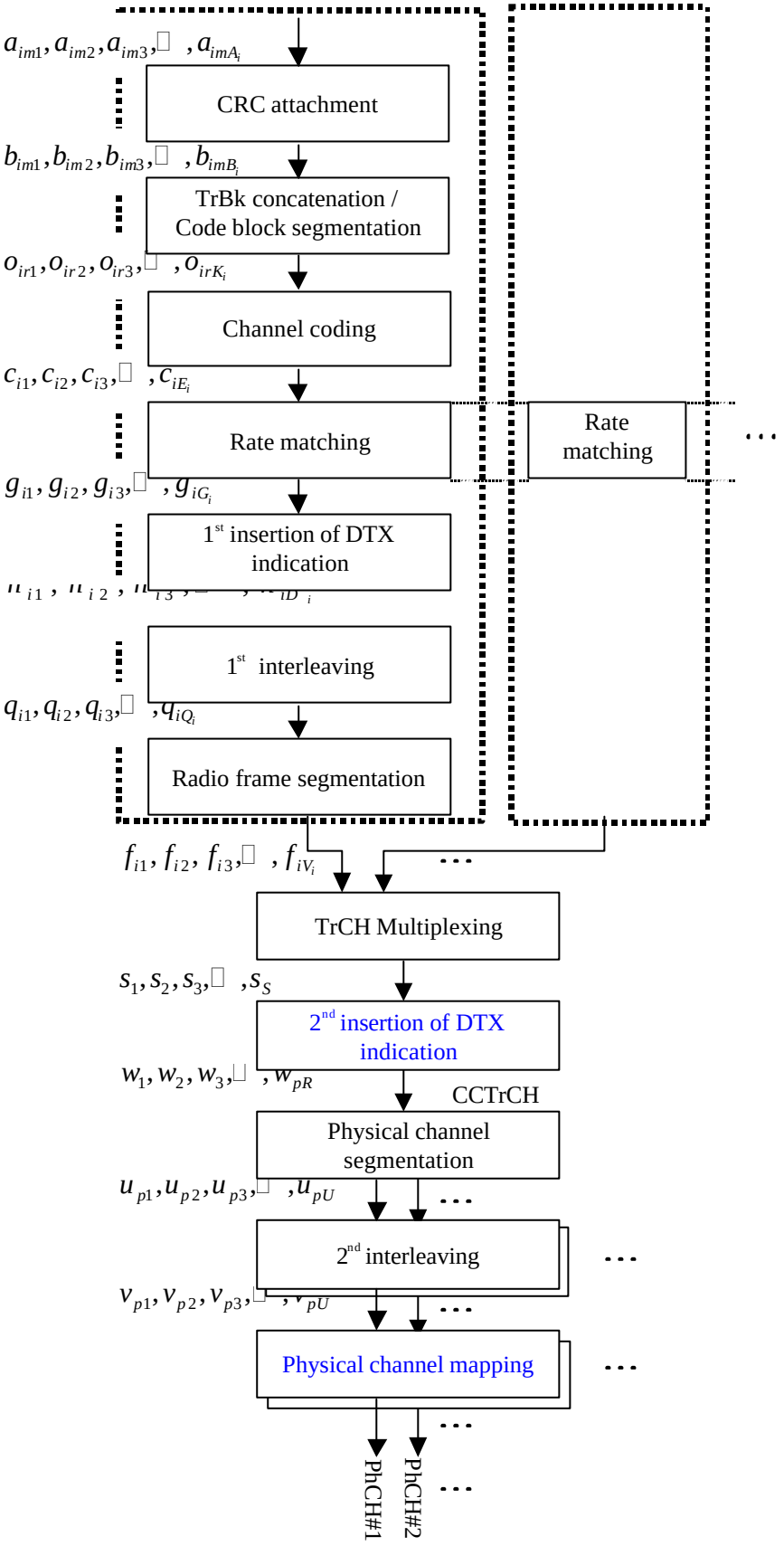

Figure 2: Transport channel multiplexing structure for downlink