TSG-RAN WG1 meeting #17 **R1-001405**
Stockholm, SE
November 20th $-$ 24th, 2000

Agenda item:

Source: Golden Bridge Technology / LG Electronics

Title: CR 090 to TS 25.211 PCPCH/DL-DPCCH timing relation

Document for: Discussion and Approval.

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A timing relationship between the start of the reception of DL-DPCCH (for CPCH) at UE and the PCPCH power control preamble is defined in order to harmonise with the already established timing relation between the UL / DL DPCCH at the UE. The timing of the PCPCH power control preamble is delayed by $T_o = 1024$ chips from that of the corresponding DL-DPCCH measured at the UE antenna as shown in Figure 31.

3GPP TSG-RAN WG1 Meeting #17

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e.g. for 3GPP use the format TP-99xxx
or for SMG, use the format P-99-xxx

CHANGE REQUEST	*Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.*

25.211 **CR** **090**   Current Version: **3.4.0**

GSM (AA.BB) or 3G (AA.BBB) specification number ?   ? *CR number as allocated by MCC support team*

For submission to: **TSG RAN #10**   for approval **X**   strategic **☐**
list expected approval meeting # here   for information **☐**   non-strategic **☐**   *(for SMG use only)*
?

Form: CR cover sheet, version 2 for 3GPP and SMG   The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc

Proposed change affects:
(at least one should be marked with an X)
(U)SIM **☐**   ME **X**   UTRAN / Radio **X**   Core Network **☐**

Source:	Golden Bridge Technology and LG Electronics	**Date:**	20 November, 2000

Subject:	PCPCH/DL-DPCCH Timing Relationship

Work item:	

Category:

(only one category shall be marked with an X)

F	Correction	**X**	**Release:**	Phase 2	☐
A	Corresponds to a correction in an earlier release	☐		Release 96	☐
B	Addition of feature	☐		Release 97	☐
C	Functional modification of feature	☐		Release 98	☐
D	Editorial modification	☐		Release 99	**X**
				Release 00	☐

Reason for change:	The timing relation between the start of the reception of DL-DPCCH at the UE and the start of the PCPCH power control preamble is defined in this contribution.

Clauses affected:	7.4

Other specs affected:

Other 3G core specifications	☐	?	List of CRs:
Other GSM core specifications	☐	?	List of CRs:
MS test specifications	☐	?	List of CRs:
BSS test specifications	☐	?	List of CRs:
O&M specifications	☐	?	List of CRs:

Other comments:	

7.4 PCPCH/AICH timing relation

The uplink PCPCH is divided into uplink access slots, each access slot is of length 5120 chips. Uplink access slot number n is transmitted from the UE $?_{p-a1}$ chips prior to the reception of downlink access slot number n, n =0, 1, …,14.

The timing relationship between preambles, AICH, and the message is the same as PRACH/AICH. Note that the collision resolution preambles follow the access preambles in PCPCH/AICH. However, the timing relationships between CD-Preamble and CD/CA-ICH is identical to RACH Preamble and AICH. The timing relationship between CD/CA-ICH and the Power Control Preamble in CPCH is identical to AICH to message in RACH. The T_{cpch} timing parameter is identical to the PRACH/AICH transmission timing parameter. When T_{cpch} is set to zero or one, the following PCPCH/AICH timing values apply.

Note that a1 corresponds to AP-AICH and a2 corresponds to CD/CA-ICH.

$?_{p-p}$ =   Time to next available access slot, between Access Preambles.

     Minimum time = 15360 chips + 5120 chips X Tcpch

     Maximu m time = 5120 chips X 12 = 61440 chips

     Actual time is time to next slot (which meets minimum time criterion) in allocated access slot subchannel group.

$?_{p-a1}$ =   Time between Access Preamble and AP-AICH has two alternative values: 7680 chips or 12800 chips, depending on T_{cpch}

$?_{a1-cdp}$ =   Time between receipt of AP-AICH and transmission of the CD Preamble $?_{a1-cdp}$ has a minimum value of $?_{a1-cdp, min}$ =7680 chips.

$?_{p-cdp}$ =   Time between the last AP and CD Preamble. $?_{p-cdp}$ has a minimum value of $?_{p-cdp-min}$ which is either 3 or 4 access slots , depending on T_{cpch}

$?_{cdp-a2}$ =   Time between the CD Preamble and the CD/CA-ICH has two alternative values: 7680 chips or 12800 chips, depending on T_{cpch}

$?_{cdp-pcp}$ =   Time between CD Preamble and the start of the Power Control Preamble is either 3 or 4 access slots , depending on T_{cpch}.

The time between the start of the reception of DL-DPCCH slot at UE and the Power Control Preamble is T_0 chips, where T_0 is as in subclause 7.6.3.

The message transmission shall start 0 or 8 slots after the start of the power control preamble depending on the length of the power control preamble.

Figure 31 illustrates the PCPCH/AICH timing relationship when T_{cpch} is set to 0 and all access slot subchannels are available for PCPCH.

AP-AICH   CD/CA-ICH   DPCCH (DL)

T_a

Power Control, Pilot and CPCH control commands

τ_{p-a1} τ_{a1-cdp} τ_{cdp-a2}

APs

CD/CA   [Example shown is for Tcpch = 0]

0 or 8 slots

Power Control Preamble

PCPCH (UL)

P0   P1   P1

τ_{p-p} τ_{p-cdp} $\tau_{cdp-pcp}$

Information and Control Data

AP-AICH   CD/CA-ICH   DPCCH (DL)

T_a

Power Control, Pilot and CPCH control commands

τ_{p-a1} τ_{a1-cdp} τ_{cdp-a2}

APs

CD/CA   [Example shown is for Tcpch = 0]

0 or 8 slots
Power Control Preamble

T_0

PCPCH (UL)

P0   P1   P1

τ_{p-p} τ_{p-cdp} $\tau_{cdp-pcp}$
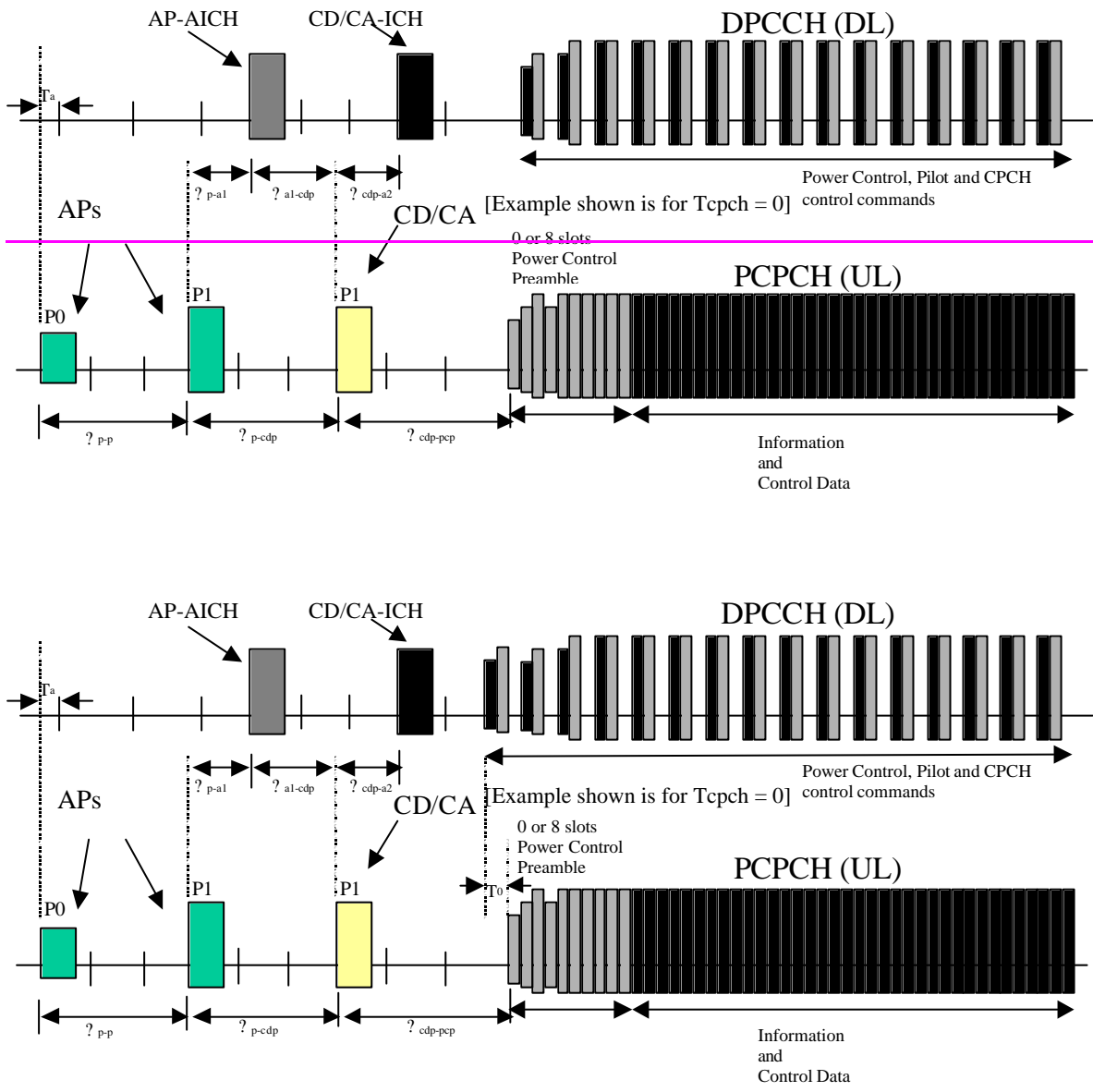
Information and Control Data

Figure 31: Timing of PCPCH and AICH transmission as seen by the UE, with $T_{cpch} = 0$