TSG-RAN Working Group 1 Meeting #17 ***TSGR1#17(00)1378***

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Agenda Item: **AH24: High Speed Downlink Packet Transmission**
Source: **SONY Corporation**
Title: **Delay on Control Information for HS-DSCH**
Document for: **Discussion**

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1. Introduction

This document discusses the issue of throughput sensitivity on DL channel quality measurement delay. The intention of the document is to start some discussion on UL and DL control message formats and timing relations that have a large impact on measurement delay. The document also presents a delay compensation mechanism using DL transmission power control commands and shows that it may be able to recover some of the throughput lost due to the measurement delay.

2. Influence of Delay on Downlink Channel Quality Report

The proposed HS-DSCH [1] requires feedback information from UE that indicates the estimate of DL channel conditions in order to determine modulation and coding scheme to be applied. In general, better estimate of channel condition would provide more efficient use of channel capacity. However, in practice, delay associated with each of following feedback process contributes to inaccuracy of the estimate under varying channel conditions.

i. Measurement of DL channel quality by UE (T_meas)
ii. Transmission of measured channel quality by UE (T_enc)
iii. Demodulation/Decoding of measurement quality report by Node-B (T_dec)
iv. Resource management and determination of AMCS mode by Node-B (T_proc)
v. Transmission of HS-DSCH control message (TF) and HS-DSCH data by Node-B (T_tx)

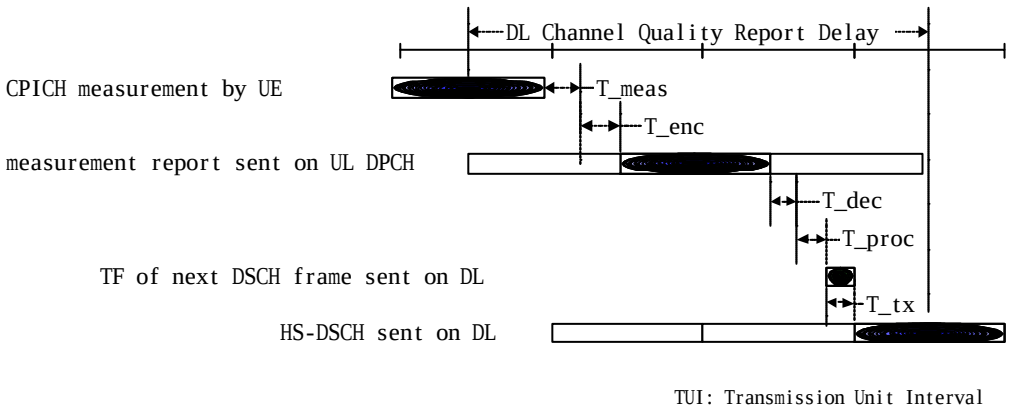

Fig. 1 Delay on DL Channel Quality Report

For T_enc and T_dec, delay depends on frame structure of uplink control message. Either DPCCH or DPDCH can be used to carry the message. If DPDCH is used, longer delay needs to be allocated for multiplexing, encoding, de-multiplexing, and decoding. TTI of the message is also a determining factor. If the TTI of the message is different from Transmission Unit Interval (TUI) of DSCH, delay associated with each DSCH TUI will be different depending on the position of TUI.

For T_tx, delay depends on how much time in advance control information needs to be sent prior to DSCH transmission. In current R99 DSCH, TFI is sent 18 to 33-slot prior to the start of DSCH frame so that variable SF DSCH can be received without chip level buffering. For HS-DSCH with fixed-spreading factor, at least a presence of data indication and channelisation code needs to be sent to UE in advance. Transmission of AMCS mode indication may be sent later depending on the selection of H-ARQ scheme and Acknowledgment transmission timing restrictions. The concept of pointer channel proposed in [2] may also be flexible enough so that the timing difference between the transmission of TFI and HS-DSCH can be kept small.

Since the uplink nor downlink frame format for control message has not been determined at this stage, exact delay for DL channel quality report cannot be determined. In simulation performed in [3], 2-frame delay was used assuming that uplink DPCCH would carry the DL channel quality report to minimize the delay. However, the frame/slot structure for uplink control message proposed in [2] suggests that there may not be enough UL DPCCH resources left for DL channel quality report which forces the message to be mapped on DPDCH as Signaling Message. For such cases, an additional delay for multiplexing, encoding, de-multiplexing, decoding must be considered as shown in Fig. 2. Although 3-frame delay may be sufficient (current simulation assumption agreed in WG#1), simulations conducted in this document will consider 4-frame delay to give more timing flexibility. Other simulation parameters are in accordance with [4] and provided as an annex.

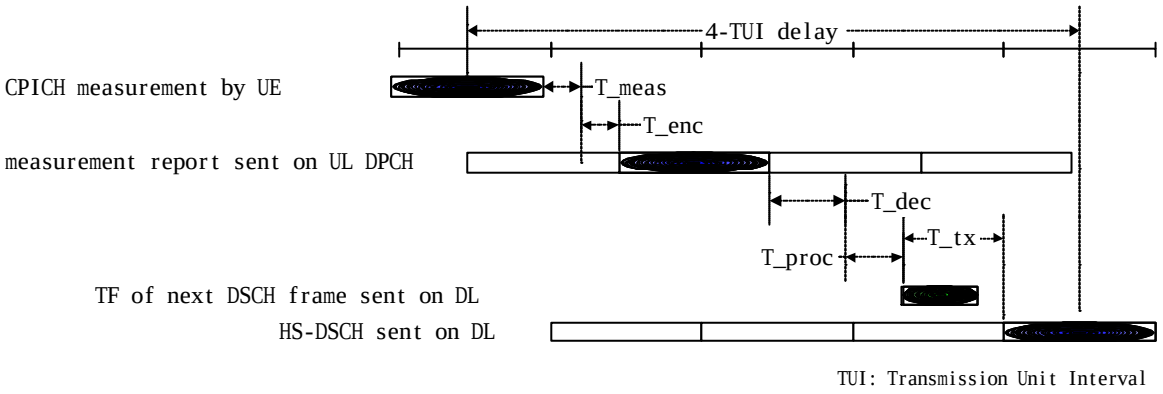

Fig. 2 Delay Model for Simulation

Fig. 3 shows the influence of DL quality report delay on throughput when no H-ARQ is used. For fading frequency less than 6Hz, the degradation is small enough so that using instantaneous SIR for AMCS mode selection is still beneficial. For fading frequency over 15Hz, however, the throughput degrades to the point below the hull indicating that the use of instantaneous SIR for mode selection may not be the choice.

Fig. 4 shows the throughput degradation when H-ARQ with max transmission count of 10 is used. For simplicity reason, Type-III soft-combining scheme with fixed AMCS mode during re-transmission is used. The larger degradation may appear if H-ARQ with variable re-transmission format (variable AMCS) according to a reported DL channel is utilized.

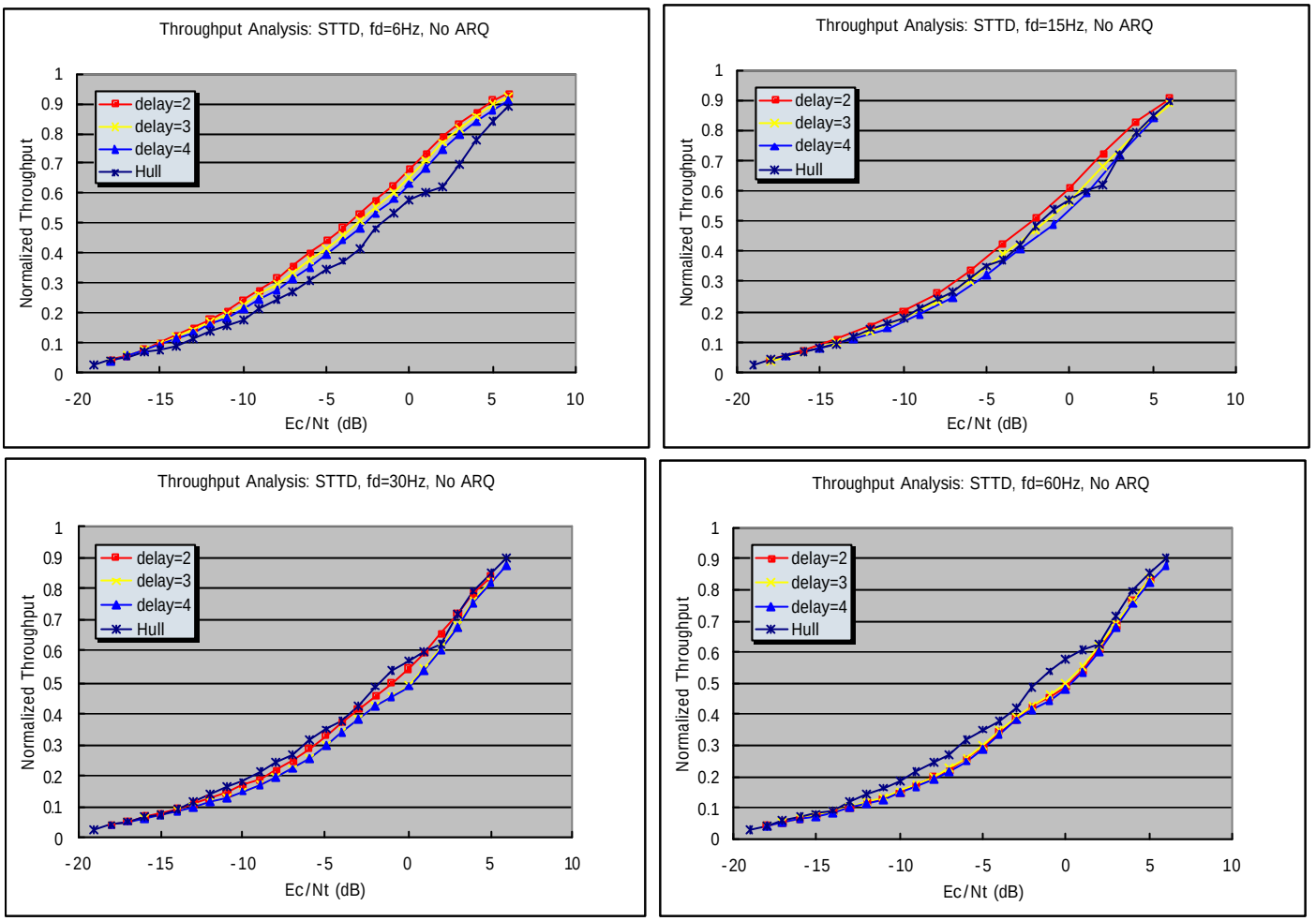

Fig. 3 Throughput degradation due to report delay (NO ARQ)

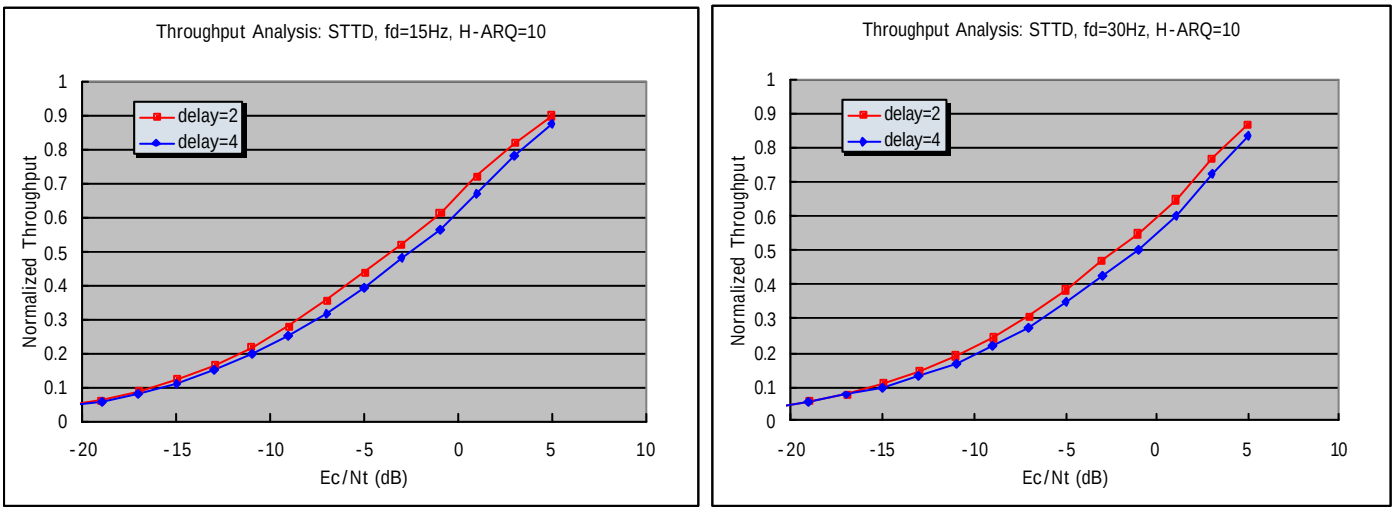

Fig. 4 Throughput degradation due to report delay (H-ARQ: Max-transmission count=10)

3. Delay Compensation using TPC

TPC commands for DL DPCH associated with HS-DSCH may be used to compensate for the DL channel condition report delay and its fundamental ability is evaluated. A concept of the use of TPC commands is illustrated in Fig. 5. TPC commands up to T_tx prior to transmission of HS-DSCH TUI are accumulated and used to adjust reported DL channel condition value. More generally, AMCS mode is selected based on DL channel quality estimated as below:

$$DL\_SIR = SIR\_report + alpha * \Delta TPC * \sum_{n} (1 - 2 * TPC\_cmd[n])$$

SIR_report is reported DL quality reported by UE, ΔTPC is UL power control step size applied, $TPC\_cmd[n]$ is decoded power control command at slot n, and $alpha$ is adjustment weight factor.

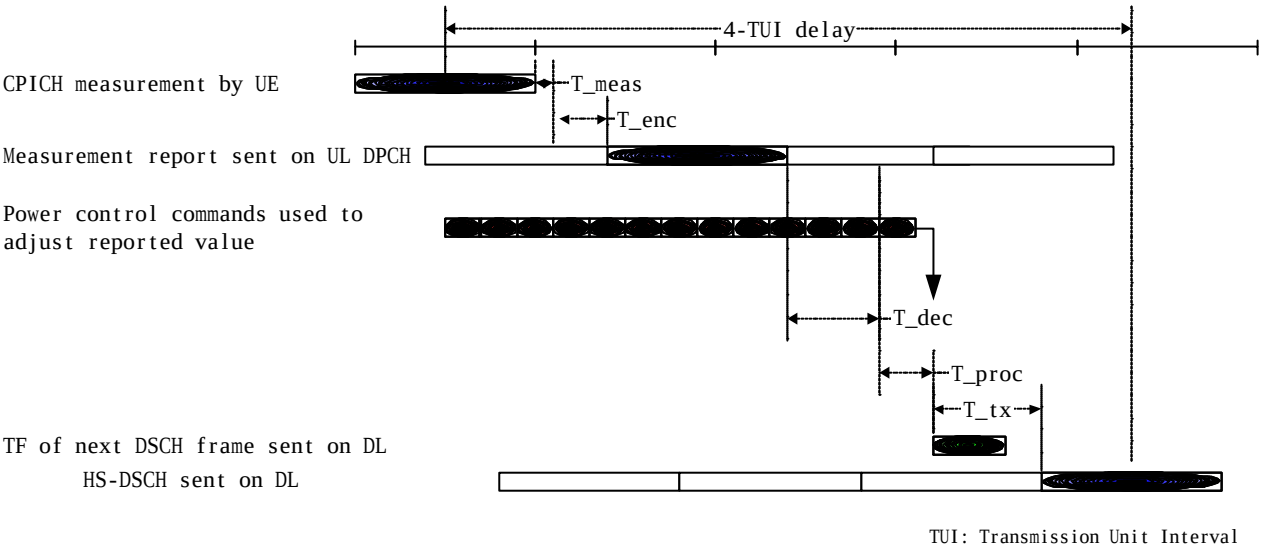

Fig. 5 Use of power control commands for DL channel quality report adjustment

Fig. 6 and Fig. 7 shows the throughput gain achieved using TPC commands to adjust the DL channel quality report. T_tx is set to 4-slot for the evaluation with 3% error in TPC commands. ΔTPC is set to 1dB and $alpha$ is set to 0.9375 in the simulation. For fading frequency up to 30Hz, gain over the hull characteristics can be achieved.

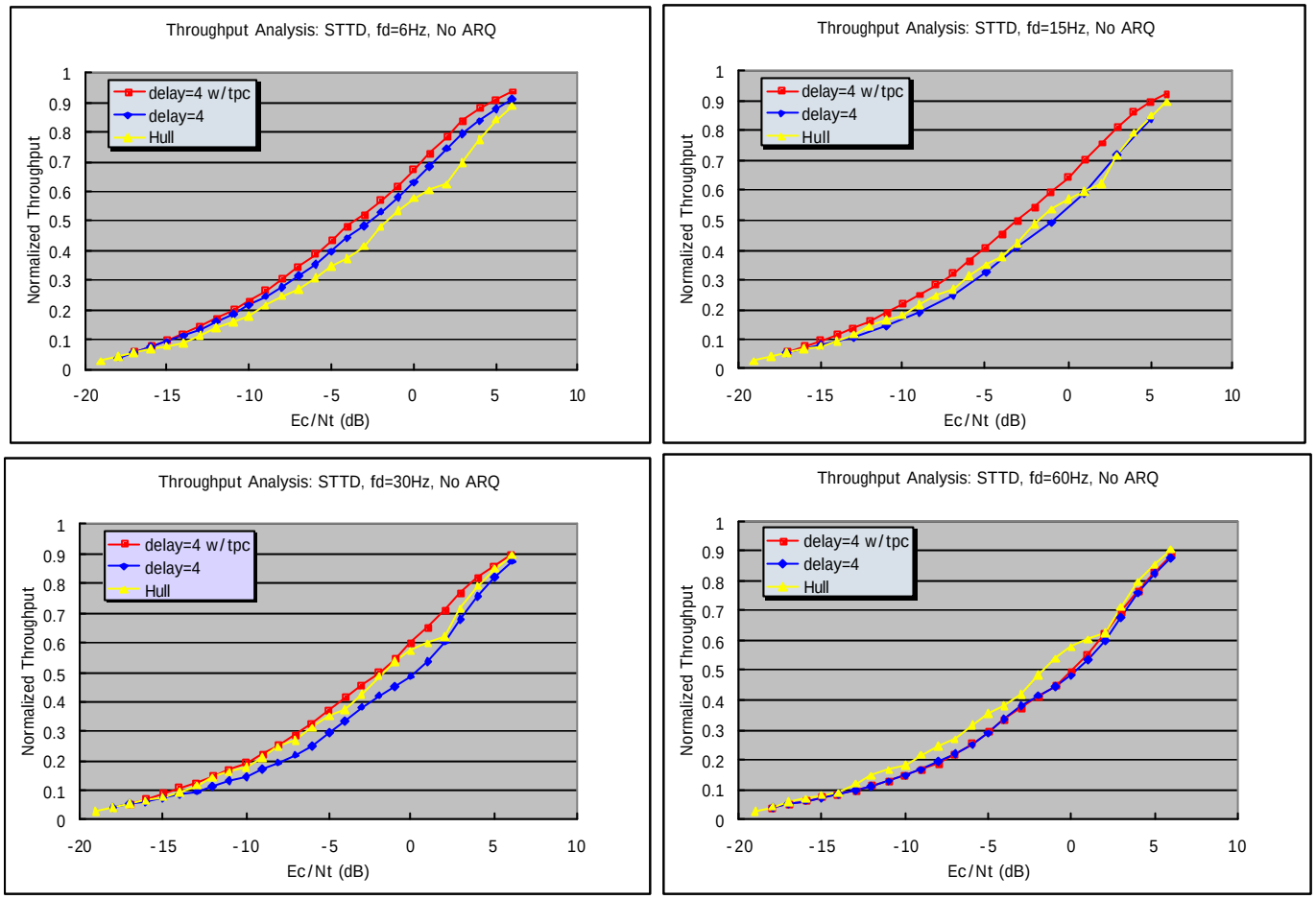

Fig. 6 Delay compensation with TPC (No ARQ: TPC error rate=3%)

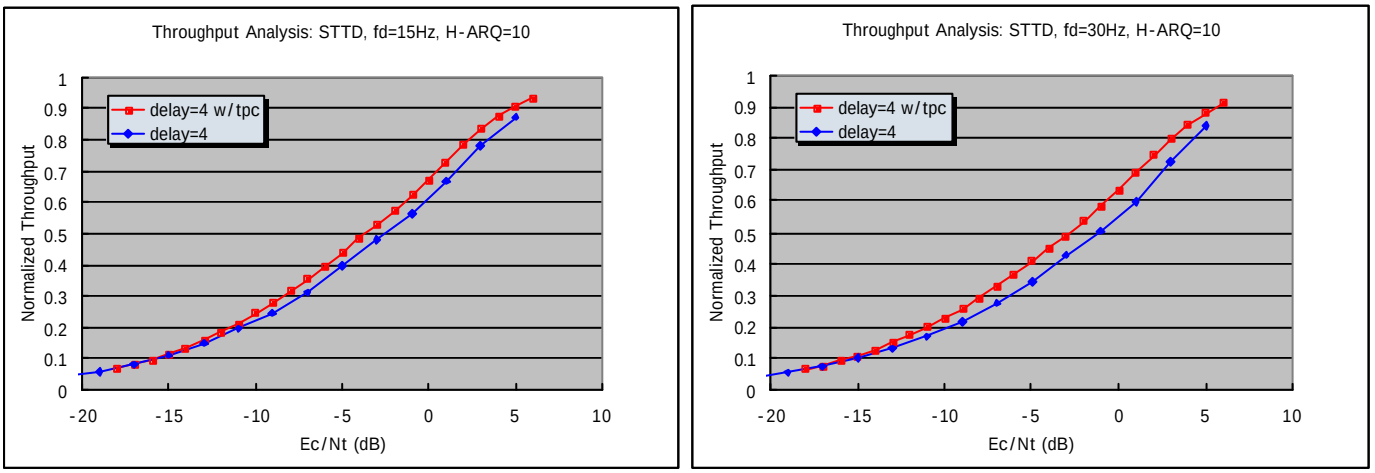

Fig. 7 Delay compensation with TPC (ARQ=10: TPC error rate=3%)

It must be noted that the gain shown here is dependent on T_tx. From throughput optimization and scheduling point of view, it is desirable to send control information (TF of HS-DSCH) aligned with the HS-DSCH TUI so that T_tx is minimized. On the other hand, for the receiver point of view, it is important that at least channelisation code information be received and decoded prior to receiving the first chip of the HS-DSCH TUI to

avoid chip level buffering. Actual gain achievable by TPC adjustment needs to be re-evaluated after a decision is made on TF transmission scheme for HS-DSCH.

It also must be noted that unlike DSCH, DPCH may go into soft-handover state where TPC commands sent from UE does not fully represent DSCH link condition. Further studies need to be carried out to investigate if gain can be achieved in DPCH soft-handover case. Primary cell indicator for DSCH power control, which is in progress for Release 4 work item, may be used to correlate TPC with DSCH link condition [5].

4. Conclusion

Longer processing delay of 4 Transmission Unit Intervals (TUI) for DL channel quality report is considered for throughput analysis of HS-DSCH. When considering the control message format and timing for both UL and DL, impact to measurement delay must be kept in mind. It is shown that throughput degradation for 15~30Hz fading condition is significant compared with previous simulation assumption which only allowed 2 TUIs for reporting delay. As for now, a transmission scheme for control messages and expected delay associated with them have not been discussed in detail.

The following issues need to be clarified and studied:

?? DL channel quality transmission scheme (Channel Type)
?? Reporting rate and delay for DL channel quality with respect to HS-DSCH TUI
?? HS-DSCH TF transmission scheme and associated delay

The document also showed some initial simulation results to indicate that use of accumulated TPC commands to adjust reported DL quality is effective to recover some of the throughput loss caused by reporting delay. Further study need to be carried out to validate its gain when associated DPCH is in soft-handover state.

5. References

[1] Motorola: “High Speed Packet Access”, TSGR1#13(00)0727, May. 2000
[2] Motorola: “Control Channel Structure for High Speed DSCH”, TSGR1#16(00)1242, Oct. 2000.
[3] SONY: “Simulation results for E-DSCH”, TSGR1#16(00)1238, Oct. 2000
[4] Ericsson, Motorola, Nokia: “Link Evaluation Methods for HSDPA” TSGR1#15(00)1093, Aug. 2000
[5] Panasonic, “Fast DSCH Scheduling Function”, TSGR2#13(00)1053, May. 2000
[6] Ericsson, Motorola, Nokia: “Common HSDPA System Simulation Assumptions” TSGR1#15(00)1094, Aug. 2000
[7] TR25.HSPA, “Physical Layer Aspects of UTRA High Speed Downlink Packet Access”, TSGR1#16(00)1316, Oct. 2000

ANNEX: SIMULATION PARAMETERS

The basic principle of link simulation condition is in line with simulation assumptions presented in [4]. The AMCS modes used in this document are shown in Table 1. Other simulation parameters are shown in Table 2.

Table 1 AMCS Mode

AMCS Mode	Modulation	TC Coding Rate	Data Rate (kbps/DSCH code)
1	QPSK	R=1/4	59.1
2	QPSK	R=1/2	118.2
3	QPSK	R=3/4	177.3
4	8PSK	R=3/4	267.3
5	16QAM	R=1/2	238.3
6	16QAM	R=3/4	357.3
7	64QAM	R=3/4	537.3

Table 2 Simulation Parameters

Spreading	Chip rate	3.84Mcps
	Over-sampling	None, 1-sample/chip
	PDSCH SF	32
	Pilot_Ec/Ior	-10dB
	DSCH_Ec/Ior	-14dB per code
Modulation	PDSCH Modulation	QPSK, 8PSK, 16QAM, 64QAM
	Channel Estimate	CPICH
FEC	DSCH FEC	PCC TC: k=4, R=1/4, R=1/2, 3/4:
	Frame Length	3.33msec (5-slot)
	Interleave Length	3.33msec (5-slot)
Adaptation	DSCH SIR Estimation	from CPICH and power offset Info.
	SIR report delay	1-PDSCH Frame (3.33msec)
Radio Channel	Antenna Diversity	STTD
	Channel	1-path: 6Hz, 15Hz, 30Hz, 60Hz flat fade
	Feedback Info. Error Rate	0%
	TPC error rate	3%
Other	ARQ Scheme	Chase combine (Type III)
	Max re-transmission number	1,10 (1=No retransmission)
	Power Control for DSCH	No
	Associated DPCH modeling	SF=256 Power controlled with fixed SIR target