TSG-RAN Working Group 1 meeting #17
Stockholm, Sweden
November 21st – 24th, 2000

TSGR1#17(00)1337

Agenda item: Release 2000 issues / AH22
Source: Nokia
Title: Outer loop power control during DPCCH gating
Document for: Discussion & Decision

---

1. Introduction

There has not yet been any discussion, how the outer loop power control would work during DPCCH gating state. In this contribution it is shortly explained what is the presently specified outer loop power control method during normal DTX, non-gating state.

After that it is discussed what kind of outer loop method would be best suited to be used during DPCCH gating.

2. Present outer loop power control method during DTX

The present method for outer loop power control during normal DTX, non-gating state, is that encoded CRC is transmitted with zero length TrCH block. This can be found from TS 25.212 , section 4.2.1.1, from which the relevant part is copy pasted below.

----------copy paste from TS 25.212, v.3.3.0, section 4.2.1.1. starts here ----------

If no transport blocks are input to the CRC calculation (M_i = 0), no CRC attachment shall be done. If transport blocks are input to the CRC calculation (M_i ? 0) and the size of a transport block is zero (A_i = 0), CRC shall be attached, i.e. all parity bits equal to zero.

----------copy paste from TS 25.212, section 4.2.1.1. ends here ----------

In the chapters below it is discussed, what could be the best method for outer loop power control during gating state.

3. Possible outer loop power control methods during gating state

3.1 Outer loop based on DPCCH

One idea could be to run the outer loop power control based on something transmitted on DPCCH, since the present concept of DPCCH gating assumes that during gating no DPDCH is transmitted. Typically this would be called DPCCH BER based outer loop method.

Using DPCCH BER for outer loop has however been discussed extensively in WG4 , and the conclusion was that DPCCH BER does not offer a good enough performance for outer loop power control. The reason is that if the number of taps or even their relative magnitude varies in the channel impulse response, the mapping of DPCCH BER to actual real QoS (=FER), can vary almost two orders of magnitude, from 10^{-2} almost to 10^{-4} [1]. Thus if outer loop tries to keep the physical channel BER stable, it means that the final QoS (=FER) varies. This was exactly the reason, why it was decided not to accept DPCCH BER measurement to drive the outer loop in Release99, and thus this cannot be seen as an appropriate method to run the outer loop power control either during DPCCH gating.

3.2 Outer loop based on CRC attached with zero length TrCH block

So, if outer loop power control cannot be based on any data transmitted on DPCCH, the logical conclusion is that it has to be based on DPDCH somehow. If it has already been specified that during normal DTX, non-gating state, outer loop is based on CRC attached to zero TrCH block , it is most straightforward to use the same method during gating. And it has been shown in WG4, that CRC based outer loop has the best performance.

This means that we need to define, that during normal gating the physical channel mapping, both in uplink and downlink, is changed so that the encoded CRC bits will be mapped only to those slots, where DPCCH is also transmitted. See the appendix , what parts of the multiplexing diagrams would be affected, it is shown there in blue. The detailed explanation of the required changes are given in the next section.

4. Changes needed in the multiplexing in TS 25.212

4.1 Physical channel mapping

Relevant part of the present definition

It is defined in sections 4.2.12.1 and 4.2.12.2, physical channel mapping for uplink and downlink, that during compressed mode, bits are mapped only to certain slots of the frame.

Required changes

Similar kind of addition is needed for gating, saying that during gating, bits are mapped only to certain slots of the frame.

In uplink :
?? during normal gating mode, the bits are mapped only to those slots, where DPCCH is also transmitted.
?? during embedded mode, the bits are mapped to all slots in the frame

In downlink:
?? during normal gating mode the bits are mapped only to those slots where DPCCH is also transmitted
?? during embedded mode, the bits are mapped to all slots in the frame

Here : normal gating mode = frames where only CRCs with zero length TrCH block(s) is (are) transmitted
embedded mode =frames where at least one non-zero length TrCH block is transmitted

This means that during RX gating [2,3], in every Kth frame UE receiver needs to decode the TFCI, before it knows that in what slots the bits are mapped to. If TFCI defines that there are only zero length transport blocks in the frame, then UE knows that the bits are mapped to only certain slots of the frame. And if TFCI defines that there is at least one non-zero length transport block in the frame, then UE knows that the bits are mapped to all slots in the frame.

The similar procedure is required from NodeB in uplink, in every frame. NodeB has to use pilot energy comparison to detect whether the frame is in normal gating mode or in embedded mode. In embedded mode all the pilot fields exist. If it detects that the frame is in normal gating mode, it knows that DPDCH is transmitted in the same slots as DPCCH. If it detects that the frame is in embedded mode, then it decodes the TFCI, and decodes the data from all slots in the frame.

4.2 2nd Insertion of DTX indication bits in downlink

Relevant part of the present definition

Presently it is defined in section 4.2.9.2. "2nd insertion of DTX indication bits " that:

?? S is the number of bits from TrCH multiplexing
?? P is the number of PhCHs bits
?? R is the number of bits in one radio frame , including DTX indication bits.

Required changes:

1) In embedded mode, the same definition can be used as before. So no changes are needed.

2) During normal gating mode, R needs to be replaced by Rgating, where:
   ?? Rgating=R/3 if gating rate=1/3
   ?? Rgating=R/5 if gating rate=1/5

4.3 Rate matching in uplink

Relevant part of the present definition

Presently it is defined in section 4.2.7. "Rate matching" that:

?? $N_{data,j}$ is the total number of bits that are available for the CCTrCH in a radio frame with transport format combination j.

Required changes:

1) In embedded mode, the same definition can be used as before. So no changes needed.

2) In normal gating mode, $N_{data,j}$ needs to be replaced by $N_{data,j}^{gating}$, where:
   ?? $N_{data,j}^{gating} = N_{data,j,}$ /3 if gating rate=1/3
   ?? $N_{data,j}^{gating} = N_{data,j}$ /5 if gating rate=1/5

5. Conclusion and proposal

It is proposed that outer loop power control based on CRC attached to zero transport block will be used also during DPCCH gating. This is because DPCCH BER will not offer good enough performance for outer loop [1].

This will mean that DPCCH gating concept will actually be DPCCH+DPDCH gating, since both DPCCH and DPDCH will contain transmitted bits only in certain slots of the frame. The sections that require changes in multiplexing definition the TS 25.212, are physical channel mapping in uplink and downlink, 2nd DTX insertion in downlink, and rate matching in uplink.

References

[1] R4-00-0013, Nokia, " Downlink Outer Loop Power Control based on physical channel BER" , San Jose, US , January 17-21, 2000.

[2] R1-00-1079, Nokia, "Proposal of using both tx and rx gating " , Berlin, Germany , August 22-25, 2000.

[3] R1-00-1338, Nokia, "Further clarifications on RX gating " , Stockholm, Sweden , November 21-24, 2000.

Annex 1: Blocks where changes are needed in TS 25.212.

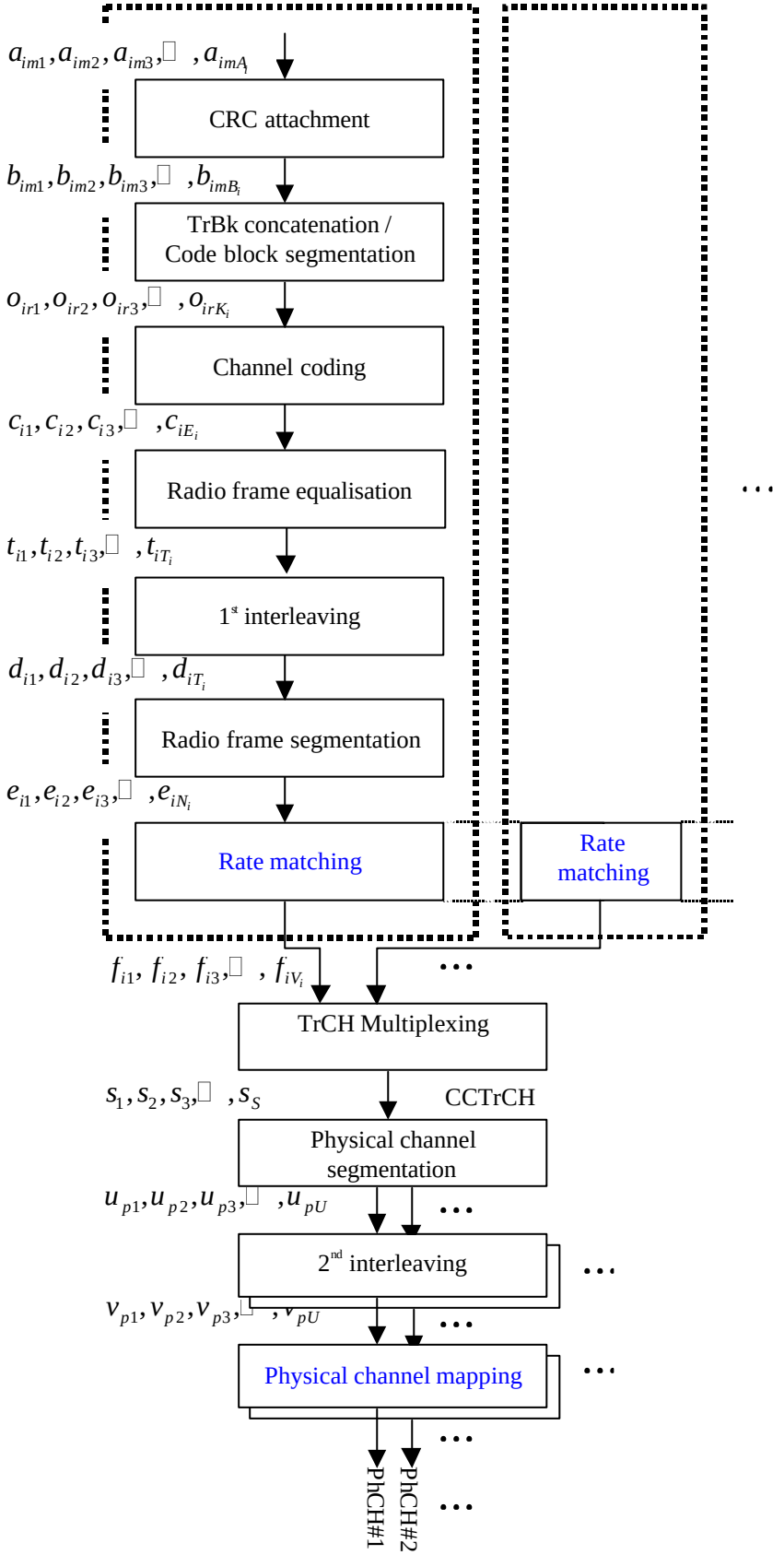

Figure 1: Transport channel multiplexing structure for uplink

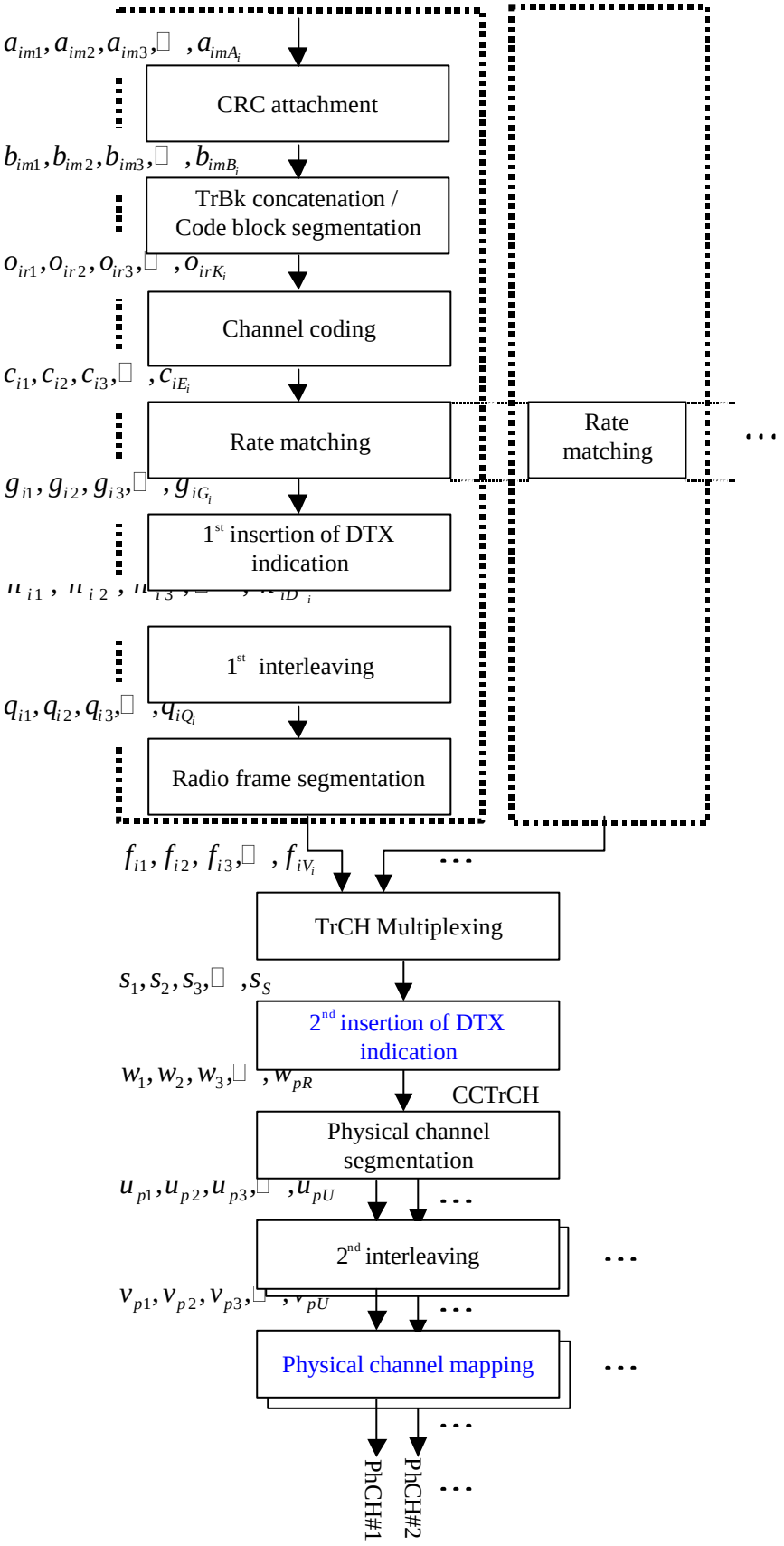

Figure 2: Transport channel multiplexing structure for downlink