3GPP TSG RAN WG1 Meeting #9
Dresden, Germany, Nov 30 - Dec 3, 1999

Document R1-99L07
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CHANGE REQUEST

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25.211 CR 005r1 Current Version: 3.0.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to: TSG-RAN #6	for approval	X	strategic		(for SMG use only)
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Proposed change affects: (U)SIM [ ] ME [X] UTRAN / Radio [X] Core Network [ ]
(at least one should be marked with an X)

Source: Ericsson **Date:** 1999-12-02

Subject: Editorial corrections

Work item: TS25.211

Category:
(only one category shall be marked with an X)

F	Correction	X
A	Corresponds to a correction in an earlier release	
B	Addition of feature	
C	Functional modification of feature	
D	Editorial modification	

Release:

Phase 2	
Release 96	
Release 97	
Release 98	
Release 99	X
Release 00	

Reason for change: Several editorial corrections are collected in this CR.

Clauses affected: 3.3, 5.2.1, 5.3.2, 5.3.3.1.2, 5.3.3.2, 5.3.3.3, 5.3.3.7, 6, 7.6.3 of TS25.211

Other specs affected:

Other 3G core specifications		→ List of CRs:
Other GSM core specifications		→ List of CRs:
MS test specifications		→ List of CRs:
BSS test specifications		→ List of CRs:
O&M specifications		→ List of CRs:

Other comments:

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3.3 Abbreviations

For the purposes of the present document, the following abbreviations apply:

AI	Acquisition Indicatior
AICH	Acquisition Indication Channel
AP	Access Preamble
BCH	Broadcast Channel
CCPCH	Common Control Physical Channel
CCTrCH	Coded Composite Transport Channel
CD	Collision Detection
CPCH	Common Packet Channel
CPICH	Common Pilot Channel
DCH	Dedicated Channel
DPCCH	Dedicated Physical Control Channel
DPCH	Dedicated Physical Channel
DPDCH	Dedicated Physical Data Channel
DSCH	Downlink Shared Channel
DTX	Discontinuous Transmission
FACH	Forward Access Channel
FBI	Feedback Information
MUI	Mobile User Identifier
PCH	Paging Channel
P-CCPCH	Primary Common Control Physical Channel
PCPCH	Physical Common Packet Channel
PDSCH	Physical Downlink Shared Channel
PI	Page Indicatior
PICH	Page Indication Channel
PRACH	Physical Random Access Channel
PSC	Primary Synchronisation Code
RACH	Random Access Channel
RNC	Radio Network Controller
S-CCPCH	Secondary Common Control Physical Channel
SCH	Synchronisation Channel
SF	Spreading Factor
SFN	System Frame Number
SSC	Secondary Synchronisation Code
STTD	Space Time Transmit Diversity
TFCI	Transport Format Combination Indicator
TSTD	Time Switched Transmit Diversity
TPC	Transmit Power Control
UE	User Equipment
UTRAN	UMTS Terrestrial Radio Access Network

5.2.1 Dedicated uplink physical channels

There are two types of uplink dedicated physical channels, the uplink Dedicated Physical Data Channel (uplink DPDCH) and the uplink Dedicated Physical Control Channel (uplink DPCCH).

The DPDCH and the DPCCH are I/Q code multiplexed within each radio frame (see [4]).

The uplink DPDCH is used to carry dedicated data generated at Layer 2 and above, i.e. the dedicated transport channel (DCH). There may be zero, one, or several uplink DPDCHs on each Layer 1 connection.

The uplink DPCCH is used to carry control information generated at Layer 1. The Layer 1 control information consists of known pilot bits to support channel estimation for coherent detection, transmit power-control (TPC) commands, feedback information (FBI), and an optional transport-format combination indicator (TFCI). The transport-format combination indicator informs the receiver about the instantaneous parameters of the different transport channels multiplexed on the uplink DPDCH, and corresponds to the data transmitted in the same frame. It is the UTRAN that determines if a TFCI should be transmitted, hence making it ~~is~~ mandatory for all UEs to support the use of TFCI in the uplink. There is one and only one uplink DPCCH on each Layer 1 connection.

Figure 1 shows the frame structure of the uplink dedicated physical channels. Each frame of length 10 ms is split into 15 slots, each of length T_{slot} = 2560 chips, corresponding to one power-control period. A super frame corresponds to 72 consecutive frames, i.e. the super-frame length is 720 ms.

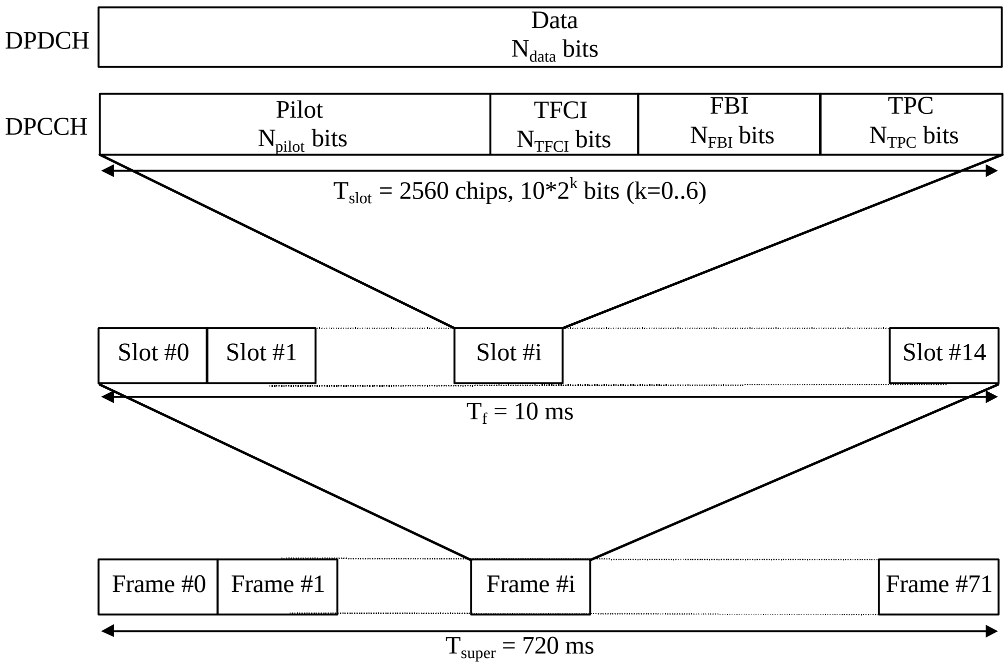

Figure 1: Frame structure for uplink DPDCH/DPCCH

The parameter k in figure 1 determines the number of bits per uplink DPDCH/DPCCH slot. It is related to the spreading factor SF of the physical channel as SF = $256/2^k$. The DPDCH spreading factor may thus range from 256 down to 4. Note that an uplink DPDCH and uplink DPCCH on the same Layer 1 connection generally are of different rates, i.e. have different spreading factors and different values of k.

The exact number of bits of the different uplink DPCCH fields (N_{pilot}, N_{TFCI}, N_{FBI}, and N_{TPC}) is determined in table 2. The field order and total number of bits/slot are fixed, though the number of bits per field may vary during a connection.

The values for the number of bits per field are given in table 1 and table 2. The channel bit and symbol rates given in table 1 are the rates immediately before spreading. The pilot patterns are given in table 3 and table 4, the TPC bit pattern is given in table 5.

The N_{FBI} bits are used to support techniques requiring feedback between the UE and the UTRAN Access Point (=cell transceiver), including closed loop mode transmit diversity and site selection diversity (SSDT). The exact details of the FBI field are shown in figure 2 and described below.

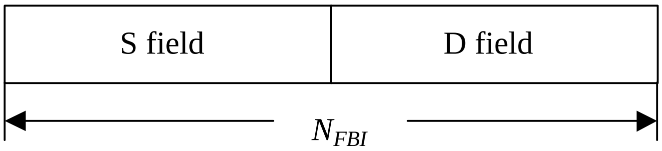

Figure 2: Details of FBI field

The S field is used for SSDT signalling, while the D field is used for ~~FB~~ Closed Loop Mode Transmit Diversity ~~S~~signalling. ~~Each of t~~The S field can be of length 0, 1 or 2. ~~and~~ The D field~~s~~ can be of length 0~~,~~ or 1. ~~or 2, with a~~ The total FBI field size N_{FBI} is according to table 2 (DPCCH fields). Simultaneous use of SSDT power control and ~~FB~~ Closed Loop Mode Transmit Diversity requires that ~~both~~ the S ~~and D~~ field~~s~~ ~~be~~ is of length 1. The use of these FBI fields is described in [5].

5.3.2 Dedicated downlink physical channels

There is only one type of downlink dedicated physical channel, the Downlink Dedicated Physical Channel (downlink DPCH).

Within one downlink DPCH, dedicated data generated at Layer 2 and above, i.e. the dedicated transport channel (DCH), is transmitted in time-multiplex with control information generated at Layer 1 (known pilot bits, TPC commands, and an optional TFCI). The downlink DPCH can thus be seen as a time multiplex of a downlink DPDCH and a downlink DPCCH, compare section 5.2.1. It is the UTRAN that determines if a TFCI should be transmitted, hence making it is mandatory for all UEs to support the use of TFCI in the downlink.

Figure 10 shows the frame structure of the downlink DPCH. Each frame of length 10 ms is split into 15 slots, each of length T_{slot} = 2560 chips, corresponding to one power-control period. A super frame corresponds to 72 consecutive frames, i.e. the super-frame length is 720 ms.

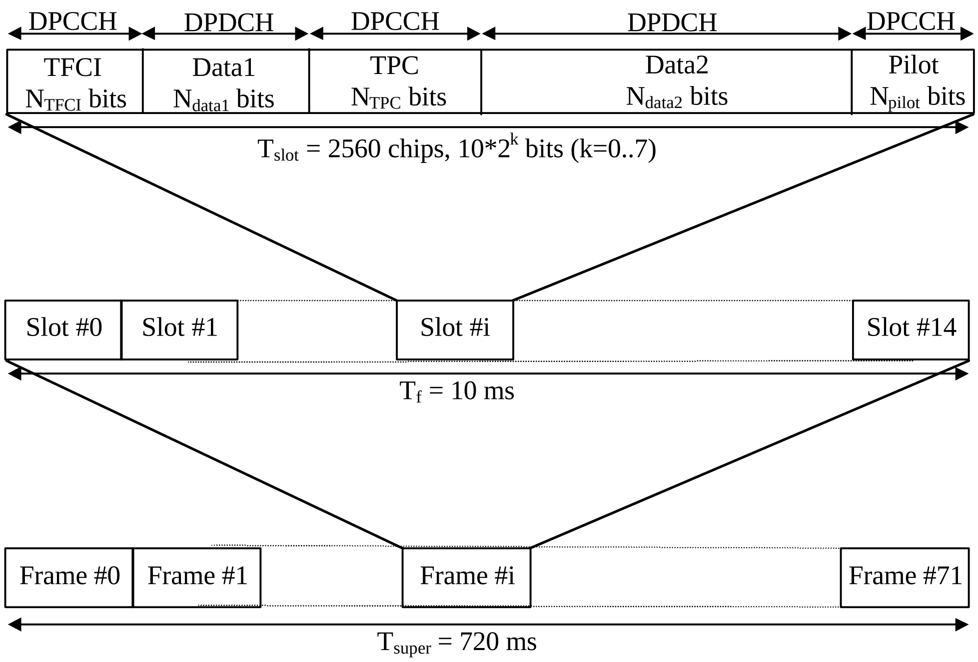

Figure 10: Frame structure for downlink DPCH

The parameter k in figure 10 determines the total number of bits per downlink DPCH slot. It is related to the spreading factor SF of the physical channel as SF = $512/2^k$. The spreading factor may thus range from 512 down to 4.

The exact number of bits of the different downlink DPCH fields (N_{pilot}, N_{TPC}, N_{TFCI}, N_{data1} and N_{data2}) is determined in table 11.The overhead due to the DPCCH transmission has to be negotiated at the connection set-up and can be re-negotiated during the communication, in order to match particular propagation conditions.

There are basically two types of downlink Dedicated Physical Channels; those that include TFCI (e.g. for several simultaneous services) and those that do not include TFCI(e.g. for fixed-rate services). These types are reflected by the duplicated rows of table 11. The channel bit and symbol rates given in table 11 are the rates immediately before spreading.

Table 11: DPDCH and DPCCH fields

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/Frame			Bits/ Slot	DPDCH Bits/Slot		DPCCH Bits/Slot		
				DPDCH	DPCCH	TOT		N_{Data1}	N_{Data2}	N_{TFCI}	N_{TPC}	N_{Pilot}
0	15	7.5	512	60	90	150	10	2	2	0	2	4
1	15	7.5	512	30	120	150	10	0	2	2	2	4
2	30	15	256	240	60	300	20	2	14	0	2	2
3	30	15	256	210	90	300	20	0	14	2	2	2
4	30	15	256	210	90	300	20	2	12	0	2	4
5	30	15	256	180	120	300	20	0	12	2	2	4
6	30	15	256	150	150	300	20	2	8	0	2	8
7	30	15	256	120	180	300	20	0	8	2	2	8
8	60	30	128	510	90	600	40	6	28	0	2	4
9	60	30	128	480	120	600	40	4	28	2	2	4
10	60	30	128	450	150	600	40	6	24	0	2	8
11	60	30	128	420	180	600	40	4	24	2	2	8
12	120	60	64	900	300	1200	80	4	56	8*	4	8
13	240	120	32	2100	300	2400	160	20	120	8*	4	8
14	480	240	16	4320	480	4800	320	48	240	8*	8	16
15	960	480	8	9120	480	9600	640	112	496	8*	8	16
16	1920	960	4	18720	480	19200	1280	240	1008	8*	8	16

* If TFCI bits are not used, then DTX shall be used in TFCI field.

The pilot symbol pattern is described in table 12. The shadowed part can be used as frame synchronization words. (The symbol pattern of the pilot symbols other than the frame synchronization word shall be “11”.) In table 12, the transmission order is from left to right. (Each two-bit pair represents an I/Q pair of QPSK modulation.)

Table 12: Pilot Symbol Pattern

	N_{pilot} = 2	N_{pilot} = 4		N_{pilot} = 8				N_{pilot} = 16							
Symbol #	0	0	1	0	1	2	3	0	1	2	3	4	5	6	7
Slot #0	11	11	11	11	11	11	10	11	11	11	10	11	11	11	10
1	00	11	00	11	00	11	10	11	00	11	10	11	11	11	00
2	01	11	01	11	01	11	01	11	01	11	01	11	10	11	00
3	00	11	00	11	00	11	00	11	00	11	00	11	01	11	10
4	10	11	10	11	10	11	01	11	10	11	01	11	11	11	11
5	11	11	11	11	11	11	10	11	11	11	10	11	01	11	01
6	11	11	11	11	11	11	00	11	11	11	00	11	10	11	11
7	10	11	10	11	10	11	00	11	10	11	00	11	10	11	00
8	01	11	01	11	01	11	10	11	01	11	10	11	00	11	11
9	11	11	11	11	11	11	11	11	11	11	11	11	00	11	11
10	01	11	01	11	01	11	01	11	01	11	01	11	11	11	10
11	10	11	10	11	10	11	11	11	10	11	11	11	00	11	10
12	10	11	10	11	10	11	00	11	10	11	00	11	01	11	01
13	00	11	00	11	00	11	11	11	00	11	11	11	00	11	00
14	00	11	00	11	00	11	11	11	00	11	11	11	10	11	01

The relationship between the TPC symbol and the transmitter power control command is presented in table 13.

Table 13: TPC Bit Pattern

TPC Bit Pattern			Transmitter power control command
N_{TPC} = 2	N_{TPC} = 4	N_{TPC} = 8	
11	1111	11111111	1
00	0000	00000000	0

For slot formats using TFCI, the TFCI value in each radio frame corresponds to a certain combination of bit rates of the DCHs currently in use. This correspondence is (re-)negotiated at each DCH addition/removal. The mapping of the TFCI bits onto slots is described in [3].

5.3.3.1.2 Secondary Common Pilot Channel

A Secondary Common Pilot Channel the following characteristics:

- Can use an arbitrary channelization code of SF=256, see [4]
- Scrambled by either the primary or a secondary scrambling code, see [4]
- Zero, one, or several per cell
- May be transmitted over only a part of the cell
- A Secondary CPICH may be the reference for the Secondary CCP~~C~~CH and the downlink DPCH. If this is the case, the UE is informed about this by higher-layer signalling.

5.3.3.2 Primary Common Control Physical Channel (P-CCPCH)

The Primary CCPCH is a fixed rate (30 kbps, SF=256) downlink physical channels used to carry the BCH.

Figure 15 shows the frame structure of the Primary CCPCH. The frame structure differs from the downlink DPCH in that no TPC commands, no TFCI and no pilot bits are transmitted. The Primary CCPCH is not transmitted during the first 256 chips of each slot. Instead, Primary SCH and Secondary SCH are transmitted during this period (see section 5.3.3.4).

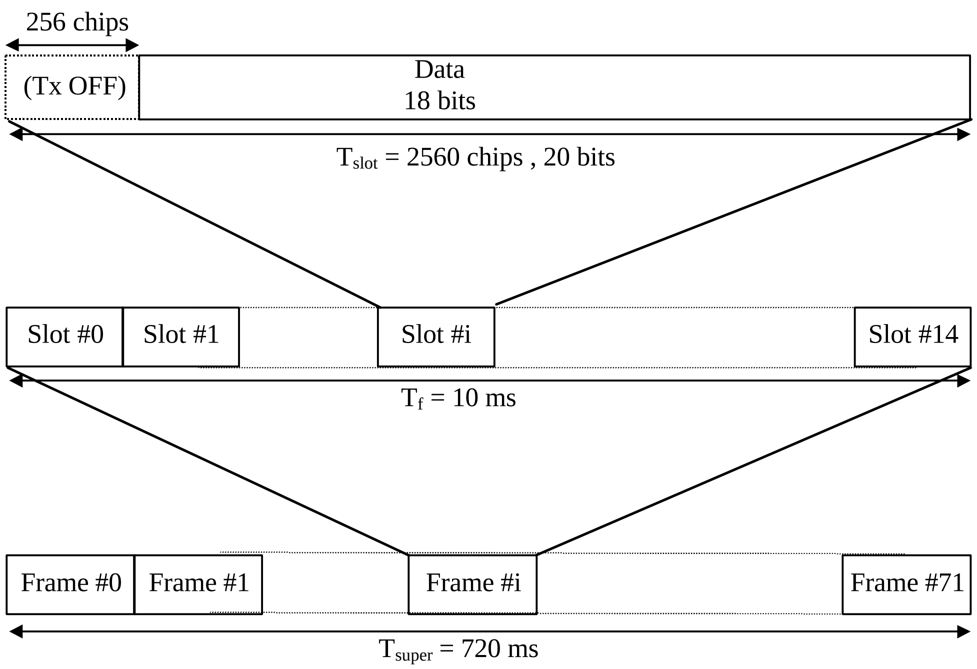

Figure 15: Frame structure for Primary Common Control Physical Channel

5.3.3.3 Secondary Common Control Physical Channel (S-CCPCH)

The Secondary CCPCH is used to carry the FACH and PCH. There are two types of Secondary CCPCH: those that include TFCI and those that do not include TFCI. It is the UTRAN that determines if a TFCI should be transmitted, hence making it mandatory for all UEs to support the use of TFCI. The set of possible rates is the same as for the downlink DPCH, see section 5.3.2. The frame structure of the Secondary CCPCH is shown in figure 17.

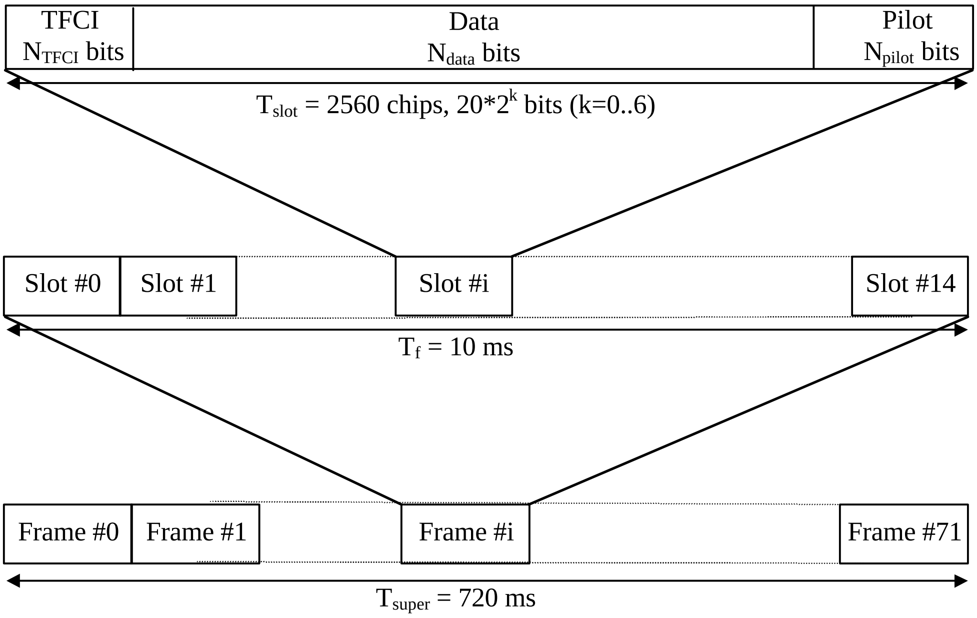

Figure 17: Frame structure for Secondary Common Control Physical Channel

The parameter k in figure 17 determines the total number of bits per downlink Secondary CCPCH slot. It is related to the spreading factor SF of the physical channel as $SF = 256/2^k$. The spreading factor range is from 256 down to 4.

The values for the number of bits per field are given in table 16 ~~and table 17~~. The channel bit and symbol rates given in table 16 are the rates immediately before spreading. The pilot patterns are given in table 18.

The FACH and PCH can be mapped to the same or to separate Secondary CCPCHs. If FACH and PCH are mapped to the same Secondary CCPCH, they can be mapped to the same frame. The main difference between a CCPCH and a downlink dedicated physical channel is that a CCPCH is not inner-loop power controlled. The main difference between the Primary and Secondary CCPCH is that the Primary CCPCH has a fixed predefined rate while the Secondary CCPCH can support variable rate with the help of the TFCI field included. Furthermore, a Primary CCPCH is continuously transmitted over the entire cell while a Secondary CCPCH is only transmitted when there is data available and may be transmitted in a narrow lobe in the same way as a dedicated physical channel (only valid for a Secondary CCPCH carrying the FACH).

Table 16: Secondary CCPCH fields~~ with pilot bits~~

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{data}	N_{pilot}	N_{TFCI}
0	30	15	256	300	20	20	0	0
~~0~~1	30	15	256	300	20	12	8	0
2	30	15	256	300	20	18	0	2
3~~1~~	30	15	256	300	20	10	8	2
4	60	30	128	600	40	40	0	0
5~~2~~	60	30	128	600	40	32	8	0
6	60	30	128	600	40	38	0	2
7~~3~~	60	30	128	600	40	30	8	2
8	120	60	64	1200	80	72	0	8*
9~~4~~	120	60	64	1200	80	64	8	8*
10	240	120	32	2400	160	152	0	8*
11~~5~~	240	120	32	2400	160	144	8	8*
12	480	240	16	4800	320	312	0	8*
13~~6~~	480	240	16	4800	320	296	16	8*
14	960	480	8	9600	640	632	0	8*
15~~7~~	960	480	8	9600	640	616	16	8*
16	1920	960	4	19200	1280	1272	0	8*
17~~8~~	1920	960	4	19200	1280	1256	16	8*

* If TFCI bits are not used, then DTX shall be used in TFCI field.

~~Table 17: Secondary CCPCH fields without pilot bits~~

~~Slot Format #i~~	~~Channel Bit Rate (kbps)~~	~~Channel Symbol Rate (ksps)~~	~~SF~~	~~Bits/ Frame~~	~~Bits/ Slot~~	~~N_{data}~~	~~N_{pilot}~~	~~N_{TFCI}~~
~~0~~	~~30~~	~~15~~	~~256~~	~~300~~	~~20~~	~~20~~	~~0~~	~~0~~
~~1~~	~~30~~	~~15~~	~~256~~	~~300~~	~~20~~	~~18~~	~~0~~	~~2~~
~~2~~	~~60~~	~~30~~	~~128~~	~~600~~	~~40~~	~~40~~	~~0~~	~~0~~
~~3~~	~~60~~	~~30~~	~~128~~	~~600~~	~~40~~	~~38~~	~~0~~	~~2~~
~~4~~	~~120~~	~~60~~	~~64~~	~~1200~~	~~80~~	~~72~~	~~0~~	~~8*~~
~~5~~	~~240~~	~~120~~	~~32~~	~~2400~~	~~160~~	~~152~~	~~0~~	~~8*~~
~~6~~	~~480~~	~~240~~	~~16~~	~~4800~~	~~320~~	~~312~~	~~0~~	~~8*~~
~~7~~	~~960~~	~~480~~	~~8~~	~~9600~~	~~640~~	~~632~~	~~0~~	~~8*~~
~~8~~	~~1920~~	~~960~~	~~4~~	~~19200~~	~~1280~~	~~1272~~	~~0~~	~~8*~~

~~* If TFCI bits are not used, then DTX shall be used in TFCI field.~~

The pilot symbol pattern is described in table 18. The shadowed part can be used as frame synchronization words. (The symbol pattern of pilot symbols other than the frame synchronization word shall be “11”). In table 18, the transmission order is from left to right. (Each two-bit pair represents an I/Q pair of QPSK modulation.)

5.3.3.7 Page Indication Channel (PICH)

The Page Indicator Channel (PICH) is a fixed rate (SF=256) physical channel used to carry the Page Indicators (PI). The PICH is always associated with an S-CCPCH to which a PCH transport channel is mapped.

Figure 22 illustrates the frame structure of the PICH. One PICH frame of length 10 ms consists of 300 bits. Of these, 288 bits are used to carry Page Indicators. The remaining 12 bits are not used.

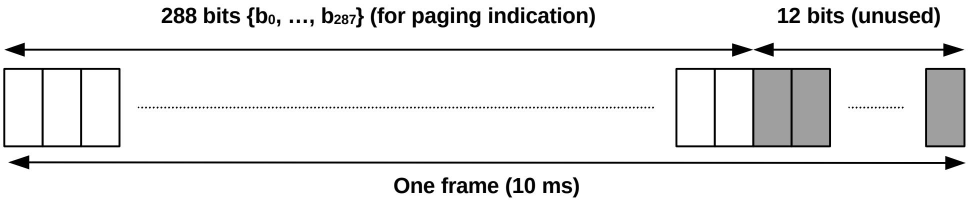

Figure 22: Structure of Page Indicator Channel (PICH)

N Page Indicators $\{PI_0, \ldots, PI_{N-1}\}$ are transmitted in each PICH frame, where N=18, 36, 72, or 144. The mapping from $\{PI_0, \ldots, PI_{N-1}\}$ to the PICH bits $\{b_0, \ldots, b_{287}\}$ are according to table 21.

Table 21: Mapping of Page Indicators (PI) to PICH bits

Number of PI per frame (N)	$PI_i = 1$	$PI_i = 0$
N=18	$\{b_{16i}, \ldots, b_{16i+15}\} = \{1,1,\ldots,1\}$	$\{b_{16i}, \ldots, b_{16i+15}\} = \{0,0,\ldots,0\}$
N=36	$\{b_{8i}, \ldots, b_{8i+7}\} = \{1,1,\ldots,1\}$	$\{b_{8i}, \ldots, b_{8i+7}\} = \{0,0,\ldots,0\}$
N=72	$\{b_{4i}, \ldots, b_{4i+3}\} = \{1, 1,\ldots,1\}$	$\{b_{4i}, \ldots, b_{4i+3}\} = \{0, 0,\ldots,0\}$
N=144	$\{b_{2i}, b_{2i+1}\} = \{1,1\}$	$\{b_{2i}, b_{2i+1}\} = \{0,0\}$

If a Paging Indicator in a certain frame is set to "1" it is an indication that UEs associated with this Page Indicator should read the corresponding frame of the associated S-CCPCH.

6 Mapping of transport channels onto physical channels

Figure 23 summarises the mapping of transport channels onto physical channels.

Transport Channels	**Physical Channels**
DCH	Dedicated Physical Data Channel (DPDCH)
	Dedicated Physical Control Channel (DPCCH)
RACH	Physical Random Access Channel (PRACH)
CPCH	Physical Common Packet Channel (PCPCH)
	Common Pilot Channel (CPICH)
BCH	Primary Common Control Physical Channel (P-CCPCH)
FACH	Secondary Common Control Physical Channel (S-CCPCH)
PCH	
	Synchronisation Channel (SCH)
DSCH	Physical Downlink Shared Channel (PDSCH)
	Acquisition Indication Channel (AICH)
	Page Indication Channel (PICH)

~~Transport Channels~~	~~Physical Channels~~
~~BCH~~	~~Primary Common Control Physical Channel (P-CCPCH)~~
~~FACH~~ ~~PCH~~	~~Secondary Common Control Physical Channel (S-CCPCH)~~
~~RACH~~	~~Physical Random Access Channel (PRACH)~~
~~CPCH~~	~~Physical Common Packet Channel (PCPCH)~~
~~DCH~~	~~Dedicated Physical Data Channel (DPDCH)~~
	~~Dedicated Physical Control Channel (DPCCH)~~
	~~Synchronisation Channel (SCH)~~
~~DSCH~~	~~Physical Downlink Shared Channel (PDSCH)~~
	~~Page Indication Channel (PICH)~~
	~~Acquisition Indication Channel (AICH)~~

Figure 23: Transport-channel to physical-channel mapping

The DCHs are coded and multiplexed as described in [3] , and the resulting data stream is mapped sequentially (first-in-first-mapped) directly to the physical channel(s). The mapping of BCH and FACH/PCH is equally straightforward, where the data stream after coding and interleaving is mapped sequentially to the Primary and Secondary CCPCH respectively. Also for the RACH, the coded and interleaved bits are sequentially mapped to the physical channel, in this case the message part of the random access burst on the PRACH.

7.6.3 Uplink/downlink timing at UE

At the UE, the uplink DPCCH/DPDCH frame transmission takes place approximately T_0 chips after the reception of the first significant path of the corresponding downlink DPCCH/DPDCH frame. T_0 is a constant defined to be 1024 chips. More information about the uplink/downlink timing relation and meaning of T_0 can be found in [5]~~, section 4.5~~.