3GPP TSG RAN WG1 ***TSGR1#9(99)k52***
November 30 – December 3, 1999, Dresden, Germany

Agenda item: **Ad hoc 14**

Source: **Philips**

Title: **Text Proposal for Timing for Initialisation Procedures**

Document for: **Decision**

Introduction

This paper is a revision of R1-99i17 following email and offline discussions.

The aim of the text proposal is to clarify the timing requirements for initialisation of DCHs and DSCHs, replacing the text currently found in section 7.1 of TS 25.214 with a new section 7.7 in TS 25.211.

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Dresden, Germany, 30 Nov – 3 Dec 1999

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3G25.211	CR	017	Current Version:	3.0.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to:	TSG RAN #6	for approval	X	strategic		(for SMG use only)
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Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc*

Proposed change affects: *(at least one should be marked with an X)*	(U)SIM		ME	X	UTRAN / Radio	X	Core Network	

Source: Philips **Date:** 1999-12-01

Subject: Timing for initialisation procedures

Work item:

Category: *(only one category shall be marked with an X)*

F	Correction	
A	Corresponds to a correction in an earlier release	
B	Addition of feature	
C	Functional modification of feature	X
D	Editorial modification	

Release:

Phase 2	
Release 96	
Release 97	
Release 98	
Release 99	X
Release 00	

Reason for change:
The current text in section 7 of TS25.214 describing rapid initialisation of DCHs is unclear and inconsistent with other parts of the specifications.
CR214-015rev1 has moved the power control information out of section 7 of TS25.214. The remaining information is timing information, which should be in TS25.211.
This CR creates a new section in TS25.211 for a clarified version of the timing information from section 7 of TS25.214.
There is also an editorial change to a cross-reference in section 7.6.3.

Clauses affected:
7 Timing relationship between physical channels (new section 7.7)
7.6.3 Uplink / downlink timing at UE

Other specs affected:

Other 3G core specifications	X	→ List of CRs:	CR25214-018rev1
Other GSM core specifications		→ List of CRs:	
MS test specifications		→ List of CRs:	
BSS test specifications		→ List of CRs:	
O&M specifications		→ List of CRs:	

Other comments:

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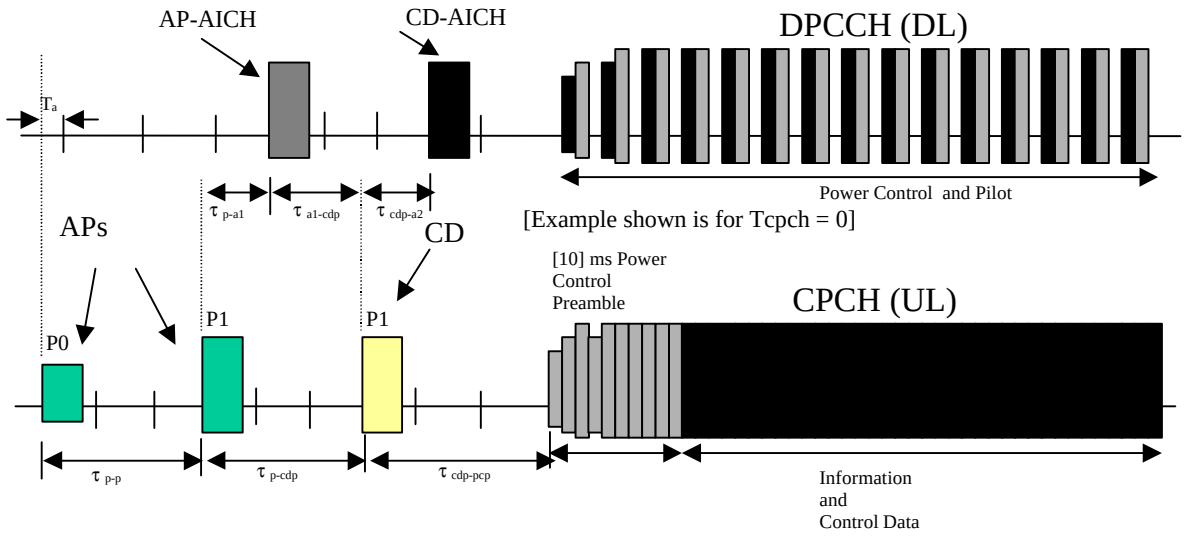

Figure 27: Timing of PCPCH and AICH transmission as seen by the UE, with T_{cpch}= 0

7.5 DPCH/PDSCH timing

The relative timing between a DPCH frame and the associated PDSCH frame is shown in figure 28.

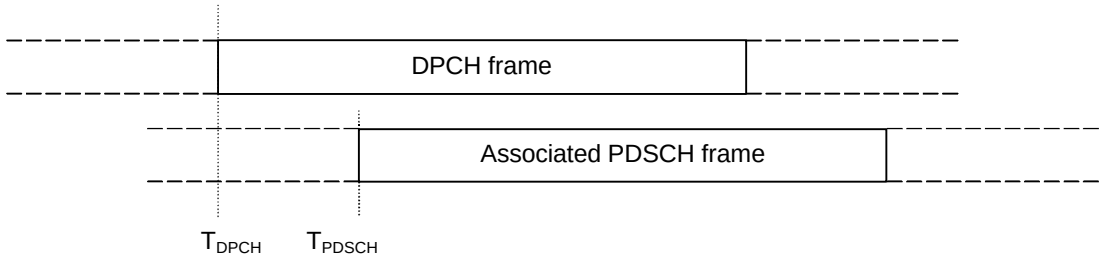

Figure 28: Timing relation between DPCH frame and associated PDSCH frame

The start of a DPCH frame is denoted T_{DPCH} and the start of the associated PDSCH frame is denoted T_{PDSCH}. Any DPCH frame is associated to one PDSCH frame through the relation -35840 chips < T_{DPCH} - T_{PDSCH} ≤ 2560 chips, i.e. the associated PDSCH frame starts anywhere between 1 slot before or up to 14 slots behind the DPCH.

7.6 DPCCH/DPDCH timing relations

7.6.1 Uplink

In uplink the DPCCH and all the DPDCHs transmitted from one UE have the same frame timing.

7.6.2 Downlink

In downlink, the DPCCH and all the DPDCHs carrying CCTrCHs of dedicated type to one UE have the same frame timing.

7.6.3 Uplink/downlink timing at UE

At the UE, the uplink DPCCH/DPDCH frame transmission takes place approximately T_0 chips after the reception of the first significant path of the corresponding downlink DPCCH/DPDCH frame. T_0 is a constant defined to be 1024 chips. More information about the uplink/downlink timing relation and meaning of T_0 can be found in [5], section 4.~~5~~3.

7.7 Timing relations for initialisation of channels

Figure 29 shows the timing relationships between the physical channels involved in the initialisation of a DCH.

The maximum time permitted for the UE to decode the relevant FACH frame before the first frame of the DPCCH is received shall be $T_{B\text{-}min}$ = 38400 chips (i.e.15 slots).

The downlink DPCCH shall commence at a time T_B after the end of the relevant FACH frame, where $T_B \geq T_{B\text{-}min}$ according to the following equation:

$$T_B = (T_n - T_k) \times 256 - N_{pcp} \times 2560 + N_{offset\_1} \times 38400 \text{ chips}$$, where:

N_{pcp} is a higher layer parameter set by the network, and represents the length (in slots) of the power control preamble (see [5], section 5.1.2.4).

N_{offset_1} is a parameter derived from the activation time set by higher layers. In order that $T_B \geq T_{B\text{-}min}$, N_{offset_1} shall be an integer number of frames such that:

$$N_{offset\_1} \geq \begin{cases} 1 \text{ when } T_n - T_k \geq \frac{T_{B-\min}}{256} + 10N_{pcp} - 150 \\ 2 \text{ when } \frac{T_{B-\min}}{256} + 10N_{pcp} - 300 \leq T_n - T_k < \frac{T_{B-\min}}{256} + 10N_{pcp} - 150 \\ 3 \text{ when } T_n - T_k < \frac{T_{B-\min}}{256} + 10N_{pcp} - 300 \end{cases}$$

T_n and T_k are parameters defining the timing of the frame boundaries on the DL DPCCH and S-CCPCH respectively (see section 7.1). These parameters are provided by higher layers.

The uplink DPCCH shall commence at a time T_C after the end of the relevant FACH frame, where

$$T_C = T_B + T_0 + N_{offset\_2} \times 38400 \text{ chips}$$, where T_0 is as in section 7.6.3 and N_{offset_2} is a UE-specific higher-layer parameter which shall be an integer number of frames greater than or equal to zero.

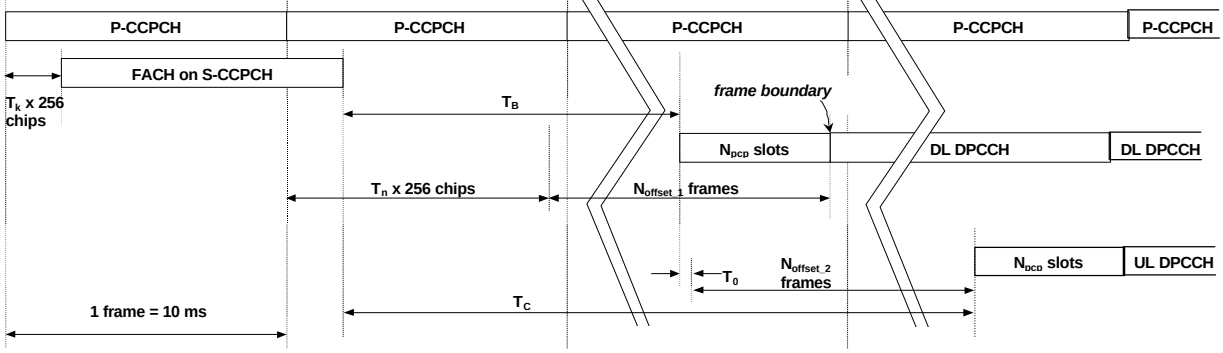

Figure 29: Timing for initialisation of DCH

The data channels shall not commence before the end of the power control preamble.

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3G25.214	CR	018rev1	Current Version:	3.0.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

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				Release 00	

Reason for change:
The current text in section 7 of TS25.214 describing rapid initialisation of DCHs is unclear and inconsistent with other parts of the specifications.
CR214-015rev1 has moved the power control information out of section 7 of TS25.214.
CR211-017 has created a new section in TS25.211 for a clarified version of the remaining information from section 7.1 of TS25.214.
This CR therefore deletes section 7.1 of TS25.214.

Clauses affected: 7.1 Rapid initialisation of DCH for packet data transfer

Other specs affected:

Other 3G core specifications	X	→ List of CRs:	CR25211-017
Other GSM core specifications		→ List of CRs:	
MS test specifications		→ List of CRs:	
BSS test specifications		→ List of CRs:	
O&M specifications		→ List of CRs:	

Other comments:

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7 Procedures in Packet Data Transfer

7.1 Rapid Initialization of DCH for Packet Data Transfer

A rapid initialization procedure for establishing a DCH is defined to support bursting packet data transfer. The rapid initialization may be invoked for downlink packet data transfer on the DSCH or uplink packet data transfer on the DCH. The procedure may also be invoked to resume a recently discontinued DCH connection.

7.1.1 Rapid Initialization of DCH for Packet Data Transfer using DSCH

The synchronization of the DSCH/DCH pair may be expedited so that data transmission using DSCH can commence in slightly over 10 ms following the FACH burst assigning the TFCI using DCH. Figure 3shows the timing diagram of RACH/FACH to DCH/DCH+DSCH state transition. The parameter T_A specifies the RACH/FACH response time. The parameters T_B, T_C and T_D are referenced relative to the FACH frame. T_B specifies the time period when the downlink DPCCH is started. The parameter T_C specifies the period at which the UE will start the uplink DPCCH. Finally, T_D specifies the period that the DCH will be stable and the first frame of data may arrive. The parameters T_B, T_C, and T_D have the following relationship:

$$T_B < T_C << T_D$$

$$T_D = T_B + N_{slots}*0.666$$

where N_{slots} is a positive integer.

In order to initialise fast uplink link power control loop, searcher and channel estimator at the Node B, the UE will adhere to the following:

- The transmission of uplink link DPCCH will start at N_{slots} slots (1 to 15 slots) prior to the scheduled downlink packet data transmission using DSCH.
- The DPCCH will be transmitted with an additional negative power offset P_{offset} from the computed open loop estimate.
- The initial power control step size for transmitting the DPCCH will be set at P_{step} (typically: 2dB).
- The UE will revert back to the normal power control (PC) step size upon the receipt of the first down power control command during the uplink DPCCH transmission phase,
- The step size always goes back to its nominal setting in the beginning of DSCH transmission

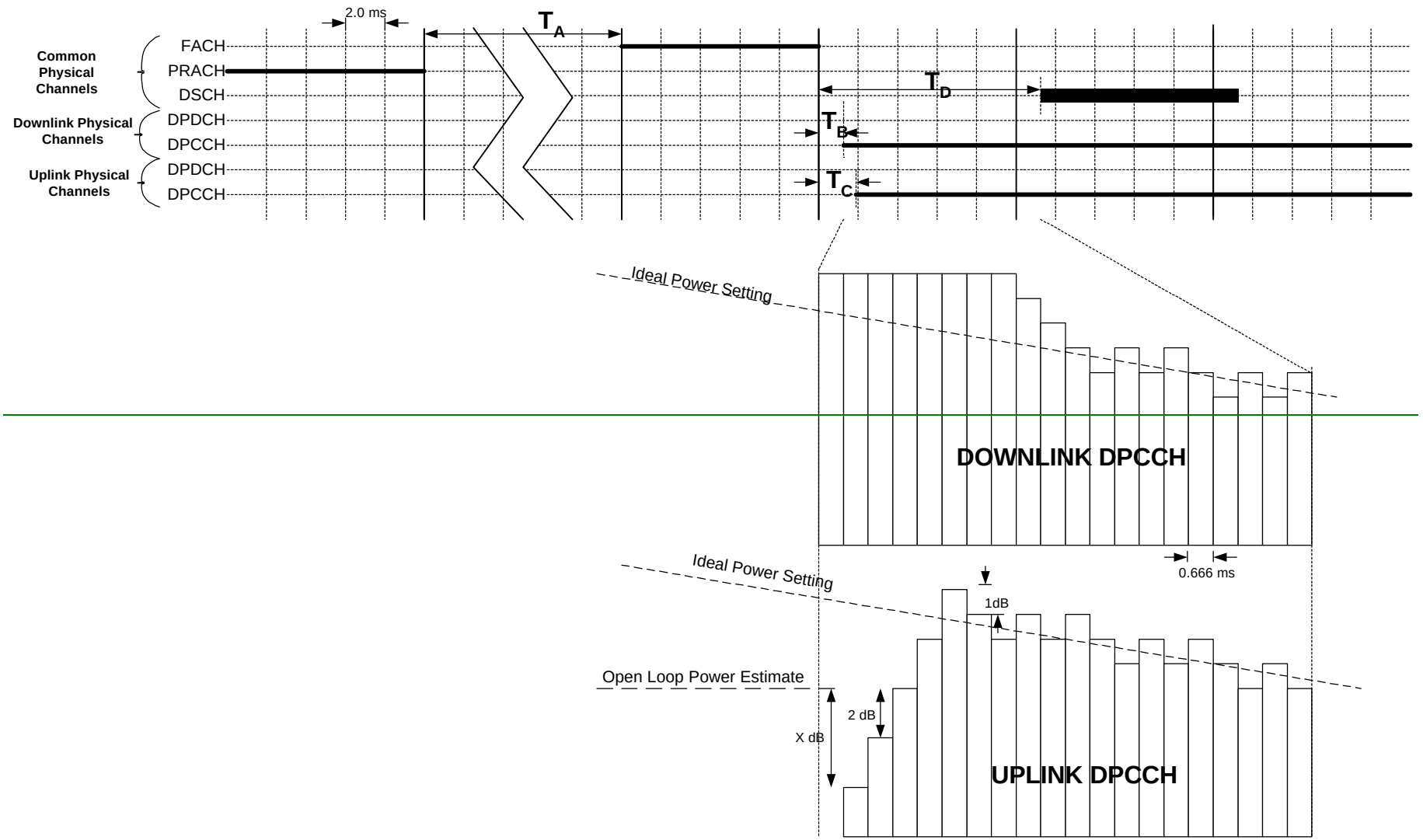
The parameters T_B, T_C, T_D, N_{slots}, P_{offset} and P_{step} may be negotiated with each individual UE or broadcast by the system so that the transition from RACH/FACH to DCH/DCH+DSCH sub-state is optimised.

7.1.2 Rapid Initialization of DCH for Uplink Packet Data Transfer

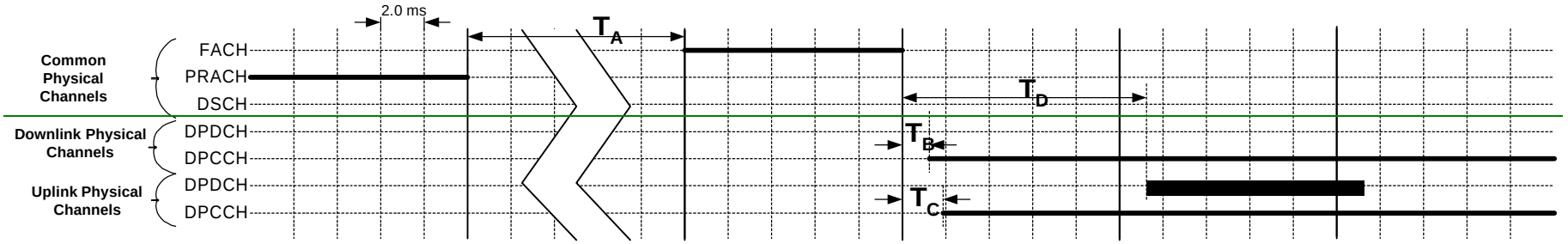
The synchronization of the DCH may also be expedited for the transfer of uplink packet data.. Figure 4 shows the same parameters T_B, T_C, and T_D applied to an uplink packet data transfer. The UE, upon detecting data in its queue, transmits a RACH with measurement report. After the UTRAN assigns the DCH via the FACH message, the downlink DPCCH is started after a time period T_B. The UE then begins transmission of the uplink DPCCH for reasons as outlined in section 7.3.4 at time period T_C. T_C is measured relative to the FACH transmit timing. Finally, the UE begins transmitting the data on the DPDCH after the period. The procedure for starting the uplink DPCCH transmission will be similar to Section 7.3.4.1

7.1.3 Resumption of DCH for Downlink or Uplink Packet Data Transfer

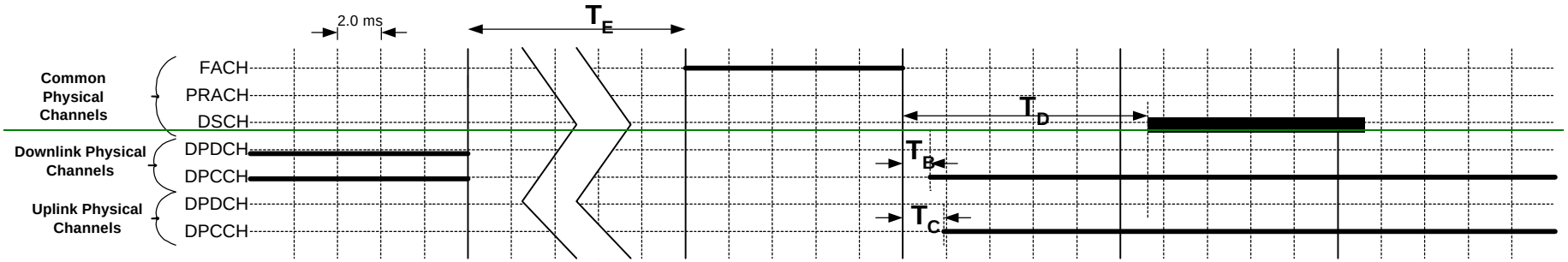
The synchronization of the DCH technique may be used to resume a DCH/DCH+DSCH connection that has been dropped for a short period.. This is applicable for packet data transfer using DSCH or uplink DPDCH or bi-directional data transfer using DSCH/Uplink DPDCH. Figure 5 shows the case where the DCH has been discontinued based on an inactivity timer T_E. The UTRAN, upon detecting data in the queue, may resume the DCH operation provided the period T_E has not elapsed. Typically T_E is set to 1000msec.



~~Figure 3: Rapid Initialization of DCH for packet data transfer over the DSCH~~



~~Figure 4: Rapid initialization of the DCH for transfer of uplink packet data~~



~~Figure 5: Resumption of the DCH for transmission of downlink packet data~~