

Agenda Item:

Source: SK Telecom

Title: CR for TAB structure and timing relation for USTS in 25.211

Document for: Discussion

1. Introduction

The procedure for Uplink Synchronous Transmission Scheme (USTS) was accepted in text (in section 9 of TS25.214) at the last Kyongju meeting [1]. However it is required to elaborate the specification related to USTS. Therefore 'Time Alignment Bit (TAB)' structure for USTS should be included in section 5.3.2 of TS25.211 which is the section for downlink dedicated physical channel. Timing issue for USTS should be also included in section 7.6.3 of TS25.211 which is the section related to uplink/downlink DPCH timing at UE. This document have CR for change in TS25.211 for USTS.

2. References

[1] SK Telecom, "Uplink Synchronous Transmission Scheme," TSGR1#7 (99)e68

CHANGE REQUEST

Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.

25.211

CR 016

Current Version: **3.0.0**

GSM (AA.BB) or 3G (AA.BBB) specification number ↑

↑ CR number as allocated by MCC support team

For submission to: **TSG-RAN #6**

list expected approval meeting # here ↑

for approval
 for information

Strategic
 non-strategic (for SMG use only)

Form: CR cover sheet, version 2 for 3GPP and SMG The latest version of this form is available from: <ftp://ftp.3gpp.org/Information/CR-Form-v2.doc>

Proposed change affects: (U)SIM ME UTRAN / Radio Core Network
 (at least one should be marked with an X)

Source: SK Telecom **Date:** 1999-11-26

Subject: Timing Control for USTS

Work item:

Category:	F Correction	<input type="checkbox"/>	Release:	Phase 2	<input type="checkbox"/>
	A Corresponds to a correction in an earlier release	<input type="checkbox"/>		Release 96	<input type="checkbox"/>
(only one category shall be marked with an X)	B Addition of feature	<input type="checkbox"/>		Release 97	<input type="checkbox"/>
	C Functional modification of feature	<input checked="" type="checkbox"/>		Release 98	<input type="checkbox"/>
	D Editorial modification	<input type="checkbox"/>		Release 99	<input checked="" type="checkbox"/>
				Release 00	<input type="checkbox"/>

Reason for change: The additional descriptions are required to support the timing information for Initial synchronization and tracking of USTS.

Clauses affected: 5.3.2, 7.6.3

Other specs affected:	Other 3G core specifications	<input type="checkbox"/>	→ List of CRs:	
	Other GSM core specifications	<input type="checkbox"/>	→ List of CRs:	
	MS test specifications	<input type="checkbox"/>	→ List of CRs:	
	BSS test specifications	<input type="checkbox"/>	→ List of CRs:	
	O&M specifications	<input type="checkbox"/>	→ List of CRs:	

Other comments:

5.3.2 Dedicated downlink physical channels

There is only one type of downlink dedicated physical channel, the Downlink Dedicated Physical Channel (downlink DPCH).

Within one downlink DPCH, dedicated data generated at Layer 2 and above, i.e. the dedicated transport channel (DCH), is transmitted in time-multiplex with control information generated at Layer 1 (known pilot bits, TPC commands, and an optional TFCI). The downlink DPCH can thus be seen as a time multiplex of a downlink DPDCH and a downlink DPCCH, compare Section 5.2.1. It is the UTRAN that determines if a TFCI should be transmitted, hence making it mandatory for all UEs to support the use of TFCI in the downlink. [In case of USTS, the TPC bits in slot #14 in frames with CFN mod 2 = 0 are replaced by Time Alignment Bits \(TABs\) as described in section 9.3 of TS 25.214.](#)

Figure 10 shows the frame structure of the downlink DPCH. Each frame of length 10 ms is split into 15 slots, each of length $T_{\text{slot}} = 2560$ chips, corresponding to one power-control period. A super frame corresponds to 72 consecutive frames, i.e. the super-frame length is 720 ms.

(snip) -----

7.6.3 Uplink/downlink timing at UE

At the UE, the uplink DPCCH/DPDCH frame transmission takes place approximately T_0 chips after the reception of the first significant path of the corresponding downlink DPCCH/DPDCH frame. T_0 is a constant defined to be 1024 chips. More information about the uplink/downlink timing relation and meaning of T_0 can be found in [5], section 4.5.

[In case of USTS, the uplink DPCCH/DPDCH frame transmission takes place \$T_{INIT_SYNC} + t_{RACH,n} - t_{p-a} - t_{DPCH,n}\$ after the reception of the first significant path of the corresponding downlink DPCCH/DPDCH frame. \$T_{INIT_SYNC} + t_{RACH,n} - t_{p-a} - t_{DPCH,n}\$ is the amount of timing control for initial synchronization determined by the synchronization process for USTS. More information about \$T_{INIT_SYNC}\$ can be found in section 5.2.8 of TS25.215.](#)