TSG-RAN Working Group 1 meeting #9 ***TSGR1#9(99)j82***
Dresden, Germany, Nov. 30 – Dec. 3, 1999

Agenda Item:
Source: **SK Telecom**
Title: **Code Allocation and Timing Control for USTS**
Document for: **Discussion**

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1. Introduction

The procedure for Uplink Synchronous Transmission Scheme (USTS) was accepted in text (in section 9 of TS25.214) at the last Kyongju meeting [1]. This document have more information about code allocation method and timing control for USTS.

2. Code Allocation and Timing Control for USTS

2.1 Code allocation:

1) Scrambling code:

Basically the same scrambling code is allocated to all UE in a cell for USTS. However additional scrambling codes may be allocated if all channelisation codes are occupied. In conclusion, the network may allocate the same scrambling code to more than one UE.

-May the network not use USTS together with short codes?

We can use either long or short scrambling code for USTS. The reason for choosing the long code is that the effects of multi-user detector and USTS is similar and if multi-user detector is adopted, the effect of USTS seems to be little (In some algorithm of multi-user detection, the timing control algorithm of USTS may give some advantages). The another reason is that the long scrambling code has better interference averaging properties. But, anyway, it is possible to use either long or short scrambling code for USTS.

2) Channelization code:

In case of USTS, UTRAN allocates the channelization codes to UEs. The channelization codes for a UE are chosen among unoccupied OVSF codes by other UEs and the channelization codes for DPDCH and DPCCH in a UE are chosen from either upper half part or lower half part of OVSF code tree. Because the allocation of channelization codes have impact on WG2/WG3 specs, we are currently proposing the document into WG2/WG3.

2.2 Timing control:

The transmission time control consists of two steps: initial synchronization and tracking.

1) Initial synchronization:

The amount of timing adjustment for Initial synchronisation is delivered through the message of higher layer. The unit of timing control is the minimum resolution which is dependent on oversampling rate for system or UE implementation, e.g., the unit of timing control step is 1/8chip for 8 times oversampling per chip.

The amount of timing control for initial synchronization (T_{INIT_SYNC}) is equal to the difference in time between the reference time of Node B and the time of recepteion of RACH as shown in Fig. 1.

The reference to the timing control for initial synchronization in UE is the time of reception of DPCH from Node B.

There are several offset times ($\tau_{DPCH,n}$) when Node B transmits DPCHs as shown in Fig. 2. Thus, the timing control for initial synchronization is practically carried out by $T_0 + \Delta T$ as shown in Fig. 2. and this value can be obtained with T_{INIT_SYNC}.

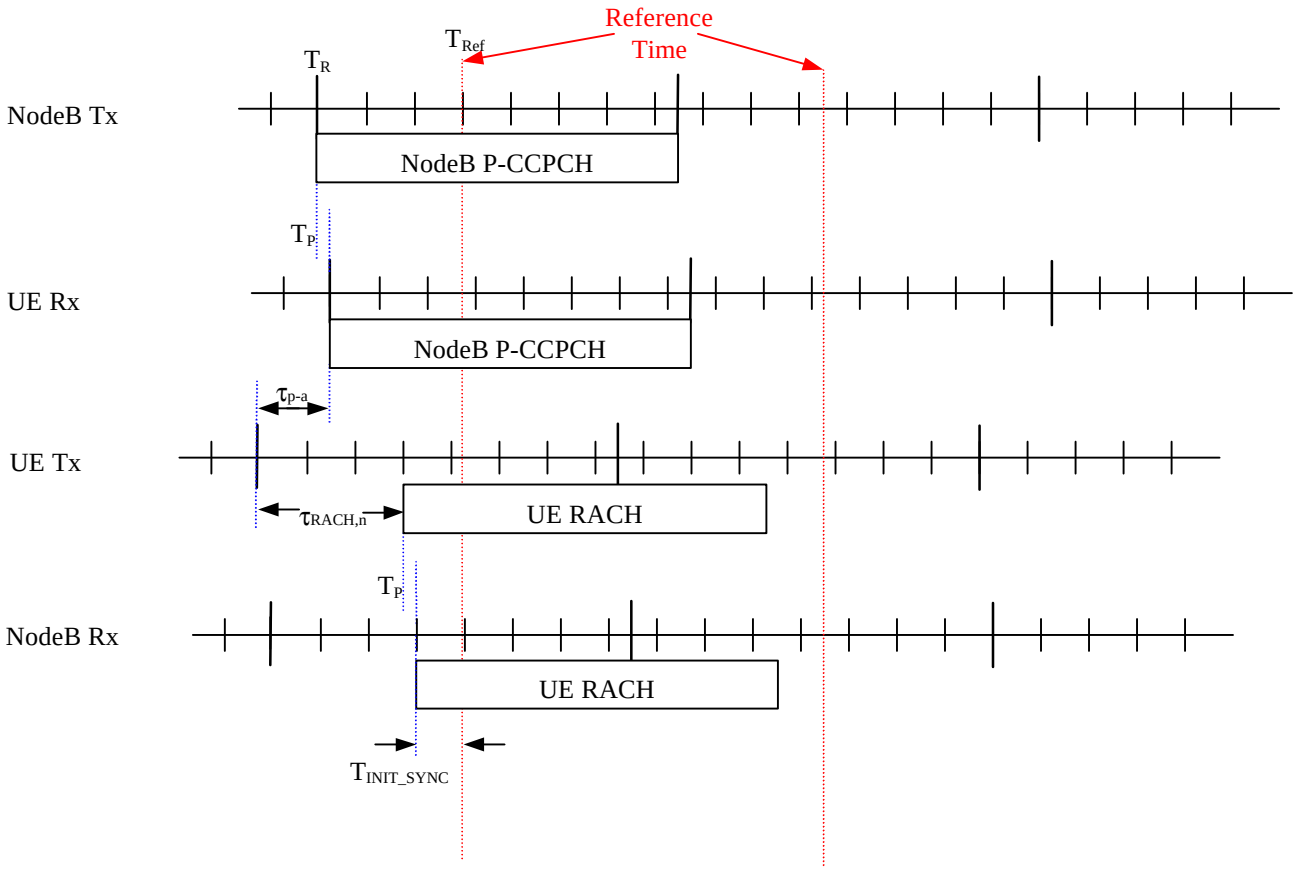

Fig. 1. The Initial Synchronization Time

- When AICH_Transmission_Timing is set to 0, then $\tau_{p\text{-}a}$ = 7680 chips
- When AICH_Transmission_Timing is set to 1, then $\tau_{p\text{-}a}$ = 12800 chips
- $\tau_{RACH,n}$: the difference in time between the start timing of #0 slot and that of selected access slot number

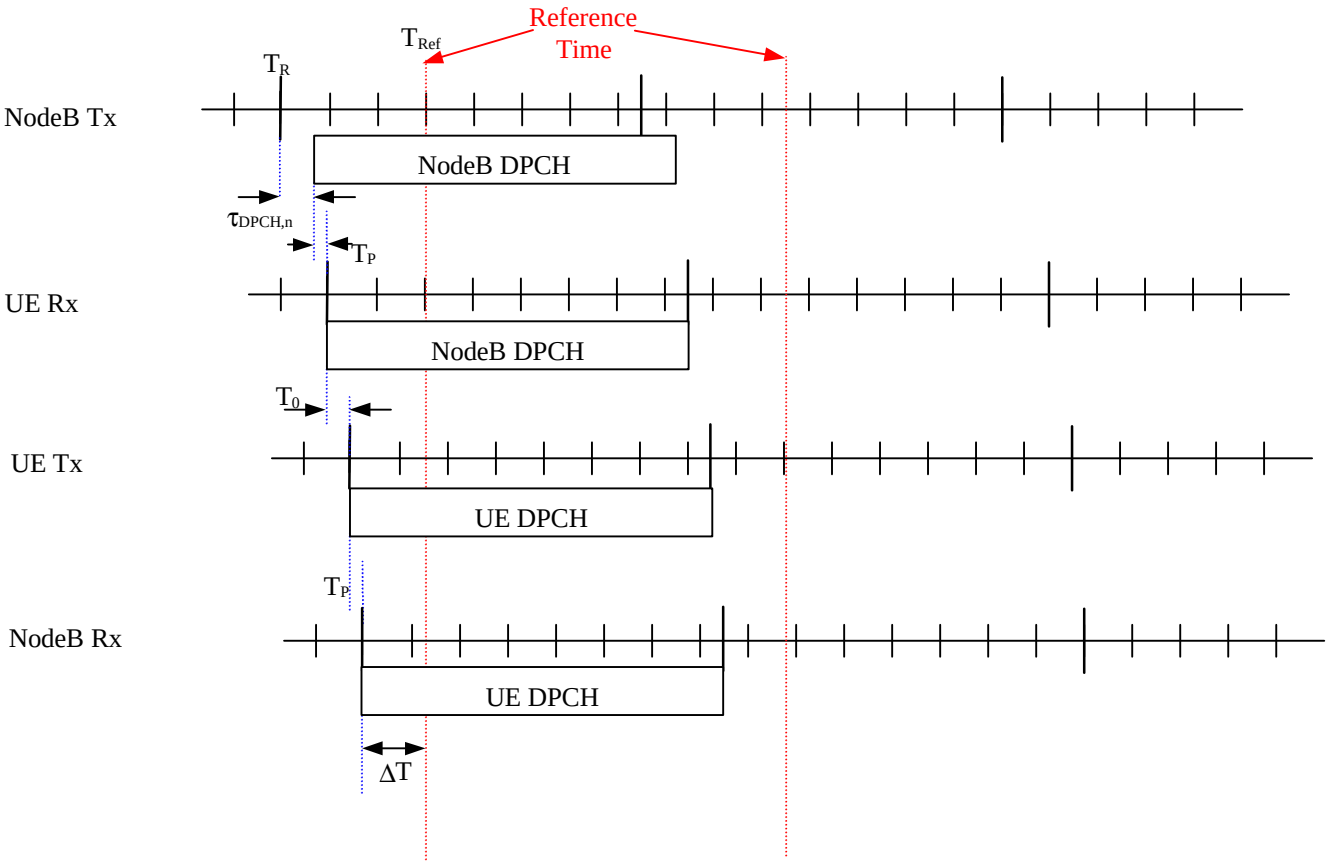

Fig 2. The timing control for Initial Synchronization

- The DPCH timing may be different for different DPCHs, but the offset from the P-CCPCH frame timing is a multiple of 256 chips, i.e. $\tau_{DPCH,n} = T_n \times 256$ chip, $T_n \in \{0, 1, \ldots, 149\}$.
- At the UE, the uplink DPCCH/DPDCH frame transmission takes place approximately T_0 chips after the reception of the first significant path of the corresponding downlink DPCCH/DPDCH frame. T_0 is a constant defined to be 1024 chips.

The time of transmission of the beginning of a uplink DPCH frame from a UE($T_{DPCH,Tx,UE}$) is written by

$$T_{DPCH,Tx,UE} = T_{DPCH,Rx,UE} + T_0 + \Delta T$$

From Fig. 1,

$$T_{INIT\_SYNC} = T_{Ref} - T_{RACH,Rx,NodeB}$$
$$= T_{Ref} - (T_R + 2T_p - t_{p-a} + t_{RACH,n}) \quad (1)$$

From Fig.2, $\Delta = T_{Ref} - (T_R + t_{DPCH,n} + {}_0 + 2T_p)$ (2)

In equation (2),

$$\Delta T + T_0 = T_{Ref} - (T_R + 2T_p + t_{DPCH,n})$$

and T_{ref}-(T_R+$2T_p$) is equal to T_{INIT_SYNC} +$\tau_{RACH,n}$ - τ_{p-a} from equation(1)

Thus, the transmitting timing is given by

$$T_{DPCH\ Tx,} = T_{DPCH,Rx} + \tau_0 +$$
$$= T_{DPCH,Rx} + T_{INIT\_SYNC} \quad t \quad_{,n} - t_{p-} - t_{DPCH\ n}$$

where, $\tau_{RACH,n}$, τ_{p-a} and $\tau_{DPCH,n}$ are known values.

As a results, the UE sets the reference time($T_{DPCH,Rx,UE}$) at the time of reception of the beginning of a downlink DPCH frame from Node B and the amount of time offset for initial synchronization is equal to $T_{INIT\_SYNC} + t_{RACH,n} - \quad_{p-a} - t_{DPCH,n}$. The transmitting timing of DPCH from UE is

$$T_{DPCH,Tx,UE} = T_{DPCH,Rx,UE} + T_{INIT\_SYNC} + t_{RACH,n} - t_{p-a} - t_{DPCH,n}$$

2) Tracking:
For tracking, UE may control the transmission time once per 2 frames. For this, TAB replaces the TPC in slot #14 in frames with CFN mod 2 = 0.
-What is the UE behavior to the TAB?
We think this is implementation issue. One of possible timing control method is UE may control (delay or advance) the transmission time by interrupting just after reading TAB. Another example of timing control method is UE may control the transmission time at the beginning of the next slot after UE reads the TAB.

2.3 Other issues:

-How does USTS work together with other schemes, such as DPC_MODE=1 for downlink power control?
Basically USTS is applicable to UEs with low mobility. Therefore we assume that there is no (soft) handover between cells. If a handover is required in USTS, hard handover may be provided by UTRAN. Regardless of DPC_MODE value, TAB replaces TPC symbol in the last slot of odd frames and UE control the transmission time according to the TAB.

3. References

[1] SK Telecom, “Uplink Synchronous Transmission Scheme,” TSGR1#7 (99)e68