TSG-RAN Working Group 1 meeting #9   **TSGR1#9(99)j05**
Dresden, Germany

Agenda item:

Source: NEC

Title: Modification of the STTD encoding scheme on DL DPCH with SF 512

Document for: Decision

Through e-mail discussions, it seems to be agreed to change the downlink slot format for SF 512 as follows;

- the field order is Data1, TPC, TFCI, Data2, and Pilot; and

- the number of bits in the Data1 field is always zero.

This modification has already been included in the CR007 of TS 25.211, "Compressed mode by higher layer scheduling". After introducing this modification, transmission power control with one-slot delay (TPC-1SD) could be possible in SF 512, if STTD encoding is not applied. If STTD encoding is applied, TPC-1SD is still impossible even with the modified slot format. This is because the TPC bits in an odd numbered slot are STTD encoded with the last two bits of the Data2 field in the previous slot. It is impossible to reflect uplink SIR measurements to such downlink TPC bits.

In the CR attached, modifications of STTD encoding for SF 512 is proposed to achieve TPC-1SD. The modifications consist of two points;

- TPC bits in each slot is not STTD encoded, and the same bits are transmitted with an equal power from the antennas.

- TFCI and Data2 bits are STTD encoded.

When introducing these modifications, the STTD encoding does not span slot boundaries anymore.

CHANGE REQUEST

Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.

| **25.211** | **CR** | | Current Version: | 3.0.0 |

GSM (AA.BB) or 3G (AA.BBB) specification number ↑   *↑ CR number as allocated by MCC support team*

For submission to: TSG RAN #6   for approval   **X**   strategic   [ ]   *(for SMG use only)*
list expected approval meeting # here ↑   for information [ ]   non-strategic [ ]

Form: CR cover sheet, version 2 for 3GPP and SMG   The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc

Proposed change affects: (U)SIM [ ]   ME **X**   UTRAN / Radio **X**   Core Network [ ]
(at least one should be marked with an X)

| **Source:** | NEC | **Date:** | 1999-11-30 |

| **Subject:** | Modification of the STTD encoding scheme on DL DPCH with SF 512 |

| **Work item:** | |

Category:
F Correction
A Corresponds to a correction in an earlier release
B Addition of feature
C Functional modification of feature   **X**
D Editorial modification

(only one category shall be marked with an X)

Release:
Phase 2   [ ]
Release 96   [ ]
Release 97   [ ]
Release 98   [ ]
Release 99   **X**
Release 00   [ ]

| **Reason for change:** | To avoid STTD-encoding the TPC bits with bits from other fields. |

| **Clauses affected:** | 5.3.2.1 |

Other specs affected:

Other 3G core specifications	**X**	→ List of CRs:	25.211-CR008
Other GSM core specifications	[ ]	→ List of CRs:	
MS test specifications	[ ]	→ List of CRs:	
BSS test specifications	[ ]	→ List of CRs:	
O&M specifications	[ ]	→ List of CRs:	

| **Other comments:** | |

5.3.2.1 STTD for DPCH

The block diagrams shown in figure 7 and figure 8 are used to STTD encode the DPDCH, TPC and TFCI symbols. The pilot symbol pattern for the DPCH channel transmitted on the diversity antenna is given in table 14. In the SF=~~512~~256 DPCH, if there is only one dedicated pilot symbol, it is STTD encoded together with the last symbol (data or DTX) of the second data field (data2) of the slot. For the SF=512 DPCH ~~the last odd data symbol in every radio frame is~~, the first two bits in each slot, i.e. TPC bits, are not STTD encoded and the same ~~symbol is~~bits are transmitted with equal power from the two antennas. The following four bits are STTD encoded.

Table 14: Pilot pattern of the DPCH channel for the diversity antenna using STTD

	Npilot = 2	Npilot = 4		Npilot = 8				Npilot = 16							
Symbol #	0	0	1	0	1	2	3	0	1	2	3	4	5	6	7
Slot #0	01	01	10	11	00	00	10	11	00	00	10	11	00	00	10
1	10	10	10	11	00	00	01	11	00	00	01	11	10	00	10
2	11	11	10	11	11	00	00	11	11	00	00	11	10	00	11
3	10	10	10	11	10	00	01	11	10	00	01	11	00	00	00
4	00	00	10	11	11	00	11	11	11	00	11	11	01	00	10
5	01	01	10	11	00	00	10	11	00	00	10	11	11	00	00
6	01	01	10	11	10	00	10	11	10	00	10	11	01	00	11
7	00	00	10	11	10	00	11	11	10	00	11	11	10	00	11
8	11	11	10	11	00	00	00	11	00	00	00	11	01	00	01
9	01	01	10	11	01	00	10	11	01	00	10	11	01	00	01
10	11	11	10	11	11	00	00	11	11	00	00	11	00	00	10
11	00	00	10	11	01	00	11	11	01	00	11	11	00	00	01
12	00	00	10	11	10	00	11	11	10	00	11	11	11	00	00
13	10	10	10	11	01	00	01	11	01	00	01	11	10	00	01
14	10	10	10	11	01	00	01	11	01	00	01	11	11	00	11