3GPP TSG-RAN WG1 (Radio) Meeting #9 ***Document*** ***R1-99I90***

Dresden, Germany, 30 Nov- 3 Dec 1999

3G CHANGE REQUEST

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25.222 **CR** **005** Current Version: 3.0.0

3G specification number ↑ *↑ CR number as allocated by 3G support team*

For submision to TSG RAN #6 *list TSG meeting no. here ↑*

for approval [X]
for information [ ]

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Proposed change affects: *(at least one should be marked with an X)* USIM [ ] ME [X] UTRAN [X] Core Network [ ]

Source: Siemens AG **Date:** 18th November 99

Subject: Editorial Changes

3G Work item: TS25.222 V3.0.0

Category: *(only one category shall be marked with an X)*

F	Correction	
A	Corresponds to a correction in a 2G specification	
B	Addition of feature	
C	Functional modification of feature	
D	Editorial modification	X

Reason for change: Due to recent editorial changes in TS25.212 for FDD the TDD specification is to be updated to harmonise FDD and TDD. Further, the list of abbreviations has been updated.

Clauses affected: 2, 3.2, 4.2.3.2.1, 4.2.3.2.3, 4.2.3.2.3.1, 4.2.5, 4.2.6, 4.2.8

Other specs affected:

Other 3G core specifications	[ ]	→ List of CRs:
Other 2G core specifications	[ ]	→ List of CRs:
MS test specifications	[ ]	→ List of CRs:
BSS test specifications	[ ]	→ List of CRs:
O&M specifications	[ ]	→ List of CRs:

Other comments:

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1 Scope

This 3GPP Report describes multiplexing, channel coding and interleaving for UTRA Physical Layer TDD mode.

Text without revision marks has been approved in the previous TSG-RAN WG1 meetings, while text with revision marks is subject to approval.

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.
- For a specific reference, subsequent revisions do not apply.
- For a non-specific reference, the latest version applies.

[1] TS 25.202 ~~(V1.0.0)~~: "UE capabilities"

[2] TS 25.211 ~~(V1.0.0)~~: "Transport channels and physical channels (FDD)"

[3] TS 25.212 ~~(V1.0.0)~~: "Multiplexing and channel coding (FDD)"

[4] TS 25.213 ~~(V1.0.0)~~: "Spreading and modulation (FDD)"

[5] TS 25.214 ~~(V1.0.0)~~: "Physical layer procedures (FDD)"

[6] TS 25.215: "Physical layer – Measurements (FDD)"

[7] TS 25.221 ~~(V1.0.0)~~: "Transport channels and physical channels (TDD)"

[8] TS 25.222 ~~(V1.0.0)~~: "Multiplexing and channel coding (TDD)"

[9] TS 25.223 ~~(V1.0.0)~~: "Spreading and modulation (TDD)"

[10] TS 25.224 ~~(V1.0.0)~~: "Physical layer procedures (TDD)"

[11] TS 25.231 ~~(V1.0.0)~~: "Measurements"

[12] TS S2.01 ~~(V1.0.0)~~: "Radio Interface Protocol Architecture"

3 Symbols and abbreviations

3.1 Symbols

For the purposes of the present document, the following symbols apply:

éxù	round towards ¥, i.e. integer such that $x \leq éxù < x+1$
ëxû	round towards -¥, i.e. integer such that $x-1 < ëxû \leq x$
çxç	absolute value of *x*

Unless otherwise is explicitly stated when the symbol is used, the meaning of the following symbols are:

i	TrCH number
j	TFC number
k	Bit number
l	TF number
m	Transport block number
n	Radio frame number
p	PhCH number
r	Code block number
I	Number of TrCHs in a CCTrCH.
C_i	Number of code blocks in one TTI of TrCH *i*.
F_i	Number of radio frames in one TTI of TrCH *i*.
M_i	Number of transport blocks in one TTI of TrCH *i*.
P	Number of PhCHs used for one CCTrCH.
PL	Puncturing Limit for the uplink. Signalled from higher layers
RM_i	Rate Matching attribute for TrCH *i*. Signalled from higher layers.

Temporary variables, i.e. variables used in several (sub)sections with different meaning.

x, X
y, Y
z, Z

3.2 Abbreviations

ARQ	Automatic Repeat on Request
BCH	Broadcast Channel
BER	Bit Error Rate
~~BPSK~~	~~Binary Phase Shift Keying~~
BS	Base Station
BSS	Base Station Subsystem
~~CA~~	~~Capacity Allocation~~
~~CAA~~	~~Capacity Allocation Acknowledgement~~
CBR	Constant Bit Rate
CCCH	Common Control Channel
CCTrCH	Coded Composite Transport Channel
~~CD~~	~~Capacity Deallocation~~
~~CDA~~	~~Capacity Deallocation Acknowledgement~~
CDMA	Code Division Multiple Access
~~CTDMA~~	~~Code Time Division Multiple Access~~
CRC	Cyclic Redundancy Check
DCA	Dynamic Channel Allocation
DCCH	Dedicated Control Channel
DCH	Dedicated Channel
DL	Downlink
DRX	Discontinuous Reception
DSCH	Downlink Shared Channel
DTX	Discontinuous Transmission
FACH	Forward Access Channel
FDD	Frequency Division Duplex
FDMA	Frequency Division Multiple Access
FEC	Forward Error Control
FER	Frame Error Rate
GF	Galois Field
~~HCS~~	~~Hierarchical Cell Structure~~
JD	Joint Detection
L1	Layer 1
L2	Layer 2
LLC	Logical Link Control

MA	Multiple Access
MAC	Medium Access Control
~~MAHO~~	~~Mobile Assisted Handover~~
~~MO~~	~~Mobile Originated~~
~~MOHO~~	~~Mobile Originated Handover~~
MS	Mobile Station
~~MT~~	~~Mobile Terminated~~
NRT	Non-Real Time
OVSF	Orthogonal Variable Spreading Factor
PC	Power Control
PCCC	Parallel Concatenated Convolutional Code
PCH	Paging Channel
PhCH	Physical Channel
PI	Paging Indicator
QoS	Quality of Service
QPSK	Quaternary Phase Shift Keying
RACH	Random Access Channel
RF	Radio Frequency
RLC	Radio Link Control
RRC	Radio Resource Control
RRM	Radio Resource Management
RSC	Recursive Systematic Coder
RT	Real Time
RU	Resource Unit
SCCC	Serial Concatenated Convolutional Code
SCH	Synchronization Channel
~~SDCCH~~	~~Stand-alone Dedicated Control Channel~~
~~SFN~~	~~System Frame Number~~
SNR	Signal to Noise Ratio
~~SP~~	~~Switching Point~~
TCH	Traffic channel
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
TFC	Transport Format Combination
TFCI	Transport Format Combination Indicator
TPC	Transmit Power Control
TrBk	Transport Block
TrCH	Transport Channel
TTI	Transmission Time Interval
UE	User Equipment
UL	Uplink
UMTS	Universal Mobile Telecommunications System
USCH	Uplink Shared Channel
UTRA	UMTS Terrestrial Radio Access
VBR	Variable Bit Rate

4 Multiplexing, channel coding and interleaving

4.1 General

Data stream from/to MAC and higher layers (Transport block / Transport block set) is encoded/decoded to offer transport services over the radio transmission link. Channel coding scheme is a combination of error detection, error correcting (including rate matching), and interleaving and transport channels mapping onto/splitting from physical channels.

In the UTRA-TDD mode, the total number of basic physical channels (a certain time slot one spreading code on a certain carrier frequency) per frame is given by the maximum number of time slots which is 15 and the maximum number of CDMA codes per time slot.

- The output from the convolutional coder shall be done in the order output0, output1,output2, output0, output1,…, output2. (When coding rate is 1/2, output is done up to output 1).
- The initial value of the shift register of the coder shall be "all 0".
- K-1 tail bits (value 0) shall be added to the end of the code block before encoding.

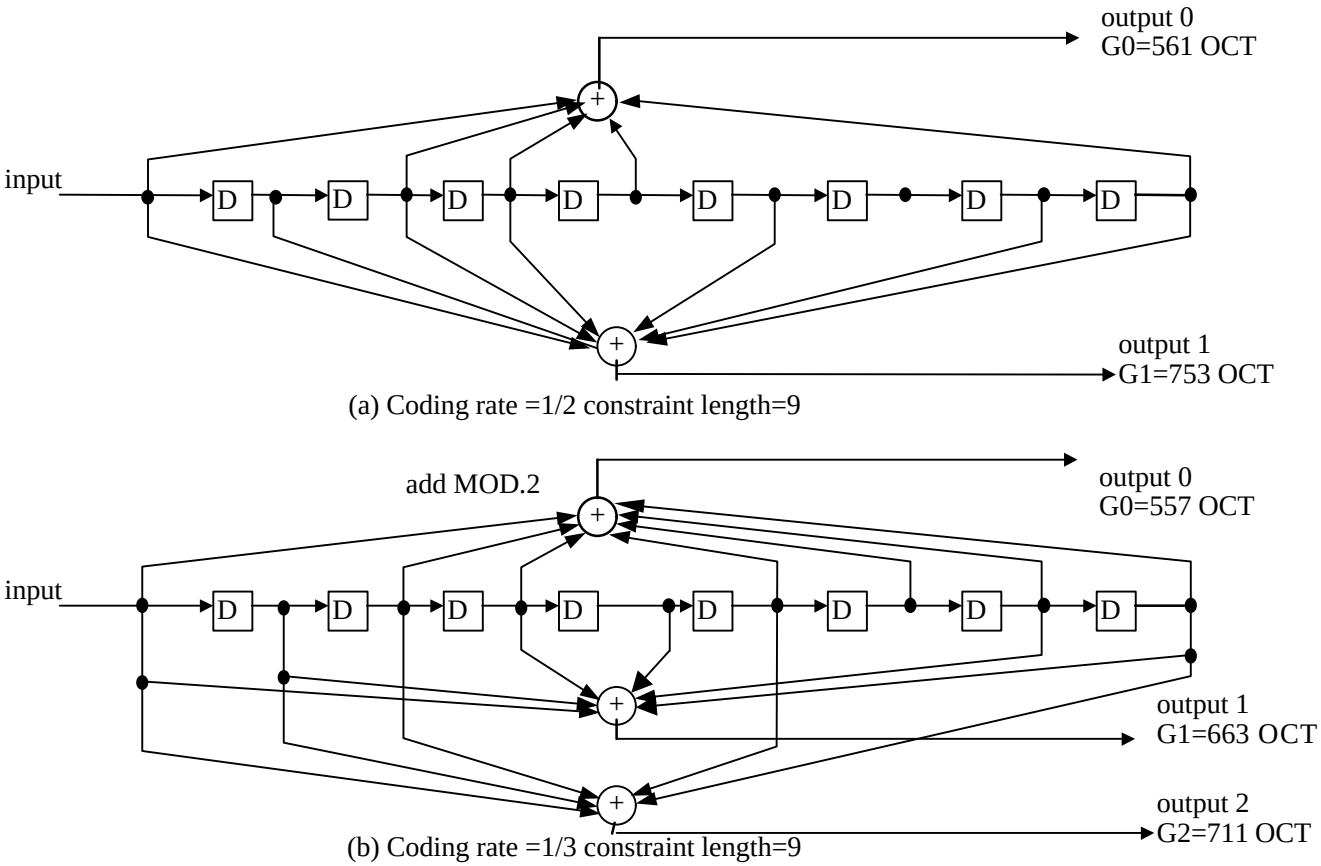

Figure 4-2: Convolutional Coder

4.2.3.2 Turbo coding

4.2.3.2.1 Turbo coder

For data services requiring quality of service between 10^{-3} and 10^{-6} BER inclusive, parallel concatenated convolutional code (PCCC) with 8-state constituent encoders is used.

The transfer function of the 8-state constituent code for PCCC is

$$G(D)=\left[1, \frac{n(D)}{d(D)}\right]$$

where,

$d(D)=1+D^2+D^3$

$n(D)=1+D+D^3$.

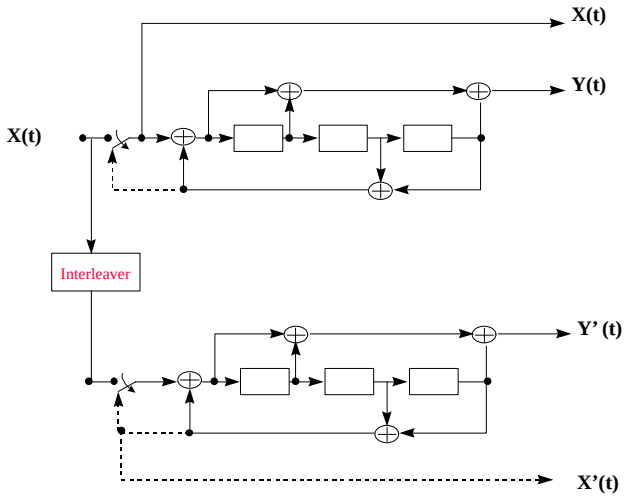

Figure 4-3: Structure of the 8-state PCCC encoder (dotted lines effective for trellis termination only)

The initial value of the shift registers of the PCCC encoder shall be all zeros.

The output of the PCCC encoder is punctured to produce coded bits corresponding to the desired code rate ~~1/3~~. For rate 1/3, none of the systematic or parity bits are punctured, and the output sequence is X(0), Y(0), Y'(0), X(1), Y(1),

4.2.3.2.2 Trellis termination in turbo code

Trellis termination is performed by taking the tail bits from the shift register feedback after all information bits are encoded. Tail bits are added after the encoding of information bits.

The first three tail bits shall be used to terminate the first constituent encoder (upper switch of figure 4-3 in lower position) while the second constituent encoder is disabled. The last three tail bits shall be used to terminate the second constituent encoder (lower switch of figure 4-3 in lower position) while the first constituent encoder is disabled.

The transmitted bits for trellis termination shall then be

X(t) Y(t) X(t+1) Y(t+1) X(t+2) Y(t+2) X'(t) Y'(t) X'(t+1) Y'(t+1) X'(t+2) Y'(t+2).

4.2.3.2.3 Turbo code internal interleaver

Figure 4-4 depicts the overall 8-State PCCC Turbo coding scheme including Turbo code internal interleaver. The Turbo code internal interleaver consists of mother interleaver generation and pruning. For arbitrary given block length K, one mother interleaver is selected from the 134 mother interleavers set. The generation scheme of mother interleaver is described in section 4.2.3.2.3.1. After the mother interleaver generation, *l*-bits are pruned in order to adjust the mother interleaver to the block length K. Tail bits T_1 and T_2 are added for constituent encoders RSC1 and RSC2 respectively. The definition of *l* is shown in section 4.2.3.2.3.2..

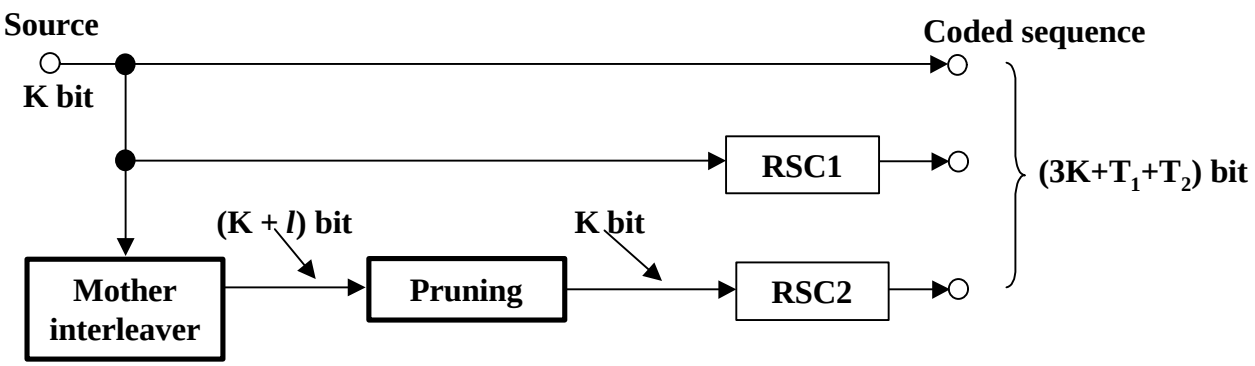

Figure 4-4: Overall 8 State PCCC Turbo Coding

4.2.3.2.3.1 Mother interleaver generation

The interleaving consists of three stages. In first stage, the input sequence is written into the rectangular matrix row by row. The second stage is intra-row permutation. The third stage is inter-row permutation. The three-stage permutations are described as follows, the input block length is assumed to be K (320 to 5114 bits).

First Stage:

(1) Determine ~~a row number~~the number of rows R such that

R=10 (K = 481 to 530 bits; Case-1)

R=20 (K = any other block length except 481 to 530 bits; Case-2)

(2) Determine ~~a column number~~the number of columns C such that

Case-1; C = p = 53

Case-2;

(i) find minimum prime p such that,

0 =< (p+1)-K/R

(ii) if (0 =< p-K/R) then go to (iii)

else C = p+1.

(iii) if (0 =< p-1-K/R) then C=p-1.

Else C = p.

(3) The input sequence of the interleaver is written into the RxC rectangular matrix row by row starting from row 0.

Second Stage:

A. If C = p

(A-1) Select a primitive root g_0 from table 4.2.2-2.

(A-2) Construct the base sequence c(i) for intra-row permutation as:

$c(i) = [g_0 \times c(i-1)] \bmod p$, i =1,2,…(p-2)., c(0) = 1.

(A-3) Select the minimum prime integer set $\{q_j\}$ (j=1,2,…R-1) such that

g.c.d$\{q_j, p\text{-}1\}$ =1

$q_j > 6$

$q_j > q_{(j-1)}$

where g.c.d. is greatest common divider. And $q_0 = 1$.

(A-4) The set $\{q_j\}$ is permuted to make a new set $\{p_j\}$ such that

$p_{P(j)} = q_j$, j = 0, 1, …. R-1,

where P(j) is the inter-row permutation pattern defined in the third stage.

(A-5) Perform the j-th (j = 0,1, 2, …, C-1) intra-row permutation as:

$c_j(i) = c([i \times p_j] \bmod (p-1))$, i =0,1,2,…, (p-2)., and $c_j(p\text{-}1) = 0$,

where c_j(i) is the input bit position of i-th output after the permutation of j-th row.

If C = p+1

(B-1) Same as case A-1.

(B-2) Same as case A-2.

(B-3) Same as case A-3.

(B-4) Same as case A-4.

(B-5) Perform the j-th (j = 0,1, 2, …, R-1) intra-row permutation as:

$$c_j(i) = c([i \times p_j] \bmod(p-1)), \quad i = 0,1,2,\ldots,(p\text{-}2)., \; c_j(p\text{-}1) = 0, \text{ and } c_j(p) = p,$$

where $c_j(i)$ is the input bit position of i-th output after the permutation of j-th row.

(B-6) If (K = C x R) then exhange $c_{R-1}(p)$ with $c_{R-1}(0)$.

If C = p-1

(C-1) Same as case A-1.

(C-2) Same as case A-2.

(C-3) Same as case A-3.

(C-4) Same as case A-4.

(C-5) Perform the j-th (j = 0,1, 2, …, R-1) intra-row permutation as:

$$c_j(i) = c([i \times p_j] \bmod(p-1)) \text{ -1}, \quad i = 0,1,2,\ldots,(p\text{-}2).,$$

where $c_j(i)$ is the input bit position of i-th output after the permutation of j-th row.

Third Stage:

Perform the inter-row permutation based on the following P(j) (j=0,1, …, R-1) patterns, where P(j) is the original row position of the j-th permuted row.

P_A: {19, 9, 14, 4, 0, 2, 5, 7, 12, 18, 10, 8, 13, 17, 3, 1, 16, 6, 15, 11} for R=20

P_B: {19, 9, 14, 4, 0, 2, 5, 7, 12, 18, 16, 13, 17, 15, 3, 1, 6, 11, 8, 10} for R=20

P_C: {9, 8, 7, 6, 5, 4, 3, 2, 1, 0} for R=10

The usage of these patterns is as follows:

Block length K: P(j)

320 to 480-bit: P_A

481 to 530-bit: P_C

531 to 2280-bit: P_A

2281 to 2480-bit: P_B

2481 to 3160-bit: P_A

3161 to 3210-bit: P_B

3211 to 5114-bit: P_A

(2) The output of the mother interleaver is the sequence read out column by column from the permuted R × C matrix starting from column 0.

Table 4.2.3-2: Table of prime p and associated primitive root

p	g_o	~~P~~p	g_o	p	g_o	~~P~~p	g_o	p	g_o
17	3	59	2	103	5	157	5	211	2
19	2	61	2	107	2	163	2	223	3
23	5	67	2	109	6	167	5	227	2
29	2	71	7	113	3	173	2	229	6
31	3	73	5	127	3	179	2	233	3
37	2	79	3	131	2	181	2	239	7
41	6	83	2	137	3	191	19	241	7
43	3	89	3	139	2	193	5	251	6
47	5	97	5	149	2	197	2	257	3
53	2	101	2	151	6	199	3		

4.2.3.2.3.2 Definition of the number of pruning bits

The output of the mother interleaver is pruned by deleting the *l*-bits in order to adjust the mother interleaver to the block length K, where the deleted bits are non-existent bits in the input sequence. The pruning bits number *l* is defined as:

$l = R \times C - K$,

where R is the row number and C is the column number defined in section 4.2.3.2.3.1.

4.2.4 Radio frame size equalisation

Radio frame size equalisation is padding the input bit sequence in order to ensure that the output can be segmented in F_i data segments of same size as described in the section 4.2.6.

The input bit sequence to the radio frame size equalisation is denoted by $c_{i1}, c_{i2}, c_{i3}, \ldots, c_{iE_i}$, where i is TrCH number and E_i the number of bits. The output bit sequence is denoted by $t_{i1}, t_{i2}, t_{i3}, \ldots, t_{iT_i}$, where T_i is the number of bits. The output bit sequence is derived as follows:

$t_{ik} = c_{ik,}$ for k = 1… E_i and

$t_{ik} = \{0 \mid 1\}$ for k= E_i +1… T_i, if $E_i < T_i$

where

$T_i = F_i * N_i$ and

$N_i = \lfloor (E_i - 1) / F_i \rfloor + 1$ is the number of bits per segment after size equalisation.

4.2.5 1st interleaving

The 1st interleaving is a block interleaver with inter-column permutations. The input bit sequence to the 1st interleaver is denoted by $x_{i1}, x_{i2}, x_{i3}, \ldots, x_{iX_i}$, where i is TrCH number and X_i the number of bits (at this stage X_i is assumed and guaranteed to be an integer multiple of TTI). The output bit sequence is derived as follows:

1) Select the number of columns C_I from table 4.2.5-1.
2) Determine the number of rows R_I defined as $R_I = X_i/C_I$
3) Write the input bit sequence into the $R_I \times C_I$ rectangular matrix row by row starting with bit $x_{i,1}$ in the first column of the first row and ending with bit $x_{i,(R_I C_I)}$ in column C_I of row R_I:

$$\begin{bmatrix} x_{i1} & x_{i2} & x_{i3} & \dots & x_{iC_I} \\ x_{i,(C_I+1)} & x_{i,(C_I+2)} & x_{i,(C_I+3)} & \dots & x_{i,(2C_I)} \\ \vdots & \vdots & \vdots & \dots & \vdots \\ x_{i,((R_I-1)C_I+1)} & x_{i,((R_I-1)C_I+2)} & x_{i,((R_I-1)C_I+3)} & \dots & x_{i,(R_IC_I)} \end{bmatrix}$$

4) Perform the inter-column permutation based on the pattern $\{P_1(j)\}$ (j=0,1, …, C-1) shown in table 4.2.5-1, where $P_1(j)$ is the original column position of the j-th permuted column. After permutation of the columns, the bits are denoted by y_{ik}:

$$\begin{bmatrix} y_{i1} & y_{i,(R_I+1)} & y_{i,(2R_I+1)} & \dots & y_{i,((C_I-1)R_I+1)} \\ y_{i2} & y_{i,(R_I+2)} & y_{i,(2R_I+2)} & \dots & y_{i,((C_I-1)R_I+2)} \\ \vdots & \vdots & \vdots & \dots & \vdots \\ y_{iR_I} & y_{i,(2R_I)} & y_{i,(3R_I)} & \dots & y_{i,(C_IR_I)} \end{bmatrix}$$

5) Read the output bit sequence $y_{i1}, y_{i2}, y_{i3}, \dots, y_{i,(C_IR_I)}$ of the 1st interleaving column by column from the inter-column permuted $R_I \times C_I$ matrix. Bit $y_{i,1}$ corresponds to the first row of the first column and bit $y_{i,(R_IC_I)}$ corresponds to row R_I of column C_I.

The bits input to the 1st interleaving are denoted by $t_{i1}, t_{i2}, t_{i3}, \dots, t_{iT_i}$, where i is the TrCH number and ~~E_i~~ T_i the number of bits. Hence, $x_{ik} = t_{ik}$ and $X_i = T_i$.

The bits output from the 1st interleaving are denoted by $d_{i1}, d_{i2}, d_{i3}, \dots, d_{iT_i}$, and $d_{ik} = y_{ik}$.

Table 4.2.5-1

TTI	Number of columns C_1	Inter-column permutation patterns
10 ms	1	{0}
20 ms	2	{0,1}
40 ms	4	{0,2,1,3}
80 ms	8	{0,4,2,6,1,5,3,7}

4.2.6 Radio frame segmentation

When the transmission time interval is longer than 10 ms, the input bit sequence is segmented and mapped onto consecutive radio frames. Following radio frame size equalisation the input bit sequence length is guaranteed to be an integer multiple of F_i.

The input bit sequence is denoted by $x_{i1}, x_{i2}, x_{i3}, \dots, x_{iX_i}$ where i is the TrCH number and X_i is the number bits. The Fi output bit sequences per TTI are denoted by $y_{i,n_i1}, y_{i,n_i2}, y_{i,n_i3}, \dots, y_{i,n_iY_i}$ where n_i is the radio frame number in current TTI and Y_i is the number of bits per radio frame for TrCH i. The output sequences are defined as follows:

$y_{i,n_ik} = x_{i,((n_i-1)Y_i)+k}$, $n_i = 1 \dots F_i$, ~~j~~ $k = 1 \dots Y_i$

where

$Y_i = (X_i / F_i)$ is the number of bits per segment,

x_{ik} is the k[th] bit of the input bit sequence and

y_{i,n_ik} is the k[th] bit of the output bit sequence corresponding to the n[th] radio frame

The n_i –th segment is mapped to the n_i –th radio frame of the transmission time interval.

4.2.8 TrCH multiplexing

Every 10 ms, one radio frame from each TrCH is delivered to the TrCH multiplexing. These radio frames are serially multiplexed into a coded composite transport channel (CCTrCH). The Transport channels are multiplexed to the frame in ascending order of DCH ID's. These DCH ID's are assigned to L1 by L2.

The bits input to the TrCH multiplexing are denoted by $f_{i1}, f_{i2}, f_{i3}, \ldots, f_{iV_i}$, where i is the TrCH number and V_i is the number of bits in the radio frame of TrCH i. The number of TrCHs is denoted by I. The bits output from TrCH multiplexing are denoted by $s_1, s_2, s_3, \ldots, s_S$, where S is the number of bits, i.e. $S = \sum_i V_i$. The TrCH multiplexing is defined by the following relations:

$s_k = f_{1k}$ $k = 1, 2, ,.V_1$

$s_k = f_{2,(k-V_1)}$ $k = V_1+1, V_1+2, ,.V_1+V_2$

$s_k = f_{3,(k-(V_1+V_2))}$ $k = (V_1+V_2)+1, (V_1+V_2)+2, ,.(V_1+V_2)+V_3$

…

$s_k = f_{I,(k-(V_1+V_2+\ldots+V_{I-1}))}$ $k = (V_1+V_2+.:.V_{I-1})+1, (V_1+V_2+.:.V_{I-1})+2, ,.(V_1+V_2+.:.V_{I-1})+V_I$

4.2.9 Physical channel segmentation

When more than one PhCH is used, physical channel segmentation divides the bits among the different PhCHs. The bits input to the physical channel segmentation are denoted by $s_1, s_2, s_3, \ldots, s_S$, where S is the number of bits input to the physical channel segmentation block. The number of PhCHs is denoted by P.

The bits after physical channel segmentation are denoted $u_{p1}, u_{p2}, u_{p3}, \ldots, u_{pU_p}$, where p is PhCH number and U_p is the in general variable number of bits in the respective radio frame for each PhCH. The relation between s_k and u_{pk} is given below.

Bits on first PhCH after physical channel segmentation:

$u_{1k} = s_k$ $k = 1, 2 , \ldots, U_1$

Bits on second PhCH after physical channel segmentation:

$u_{2k} = s_{(k+U_1)}$ $k = 1, 2 , \ldots, U_2$

…

Bits on the P^{th} PhCH after physical channel segmentation:

$u_{Pk} = s_{(k+U_1+\ldots+U_{P-1})}$ $k = 1, 2 , \ldots, U_P$

4.2.10 2nd interleaving

The 2nd interleaving can be applied jointly to all data bits transmitted during one frame, or separately within each timeslot, on which the CCTrCH is mapped. The selection of the 2nd interleaving scheme is controlled by higher layer.