

Agenda Item : **ad-hoc 4**

Source : **Nortel Networks**

Title : **Proposal for channel coding scheme for small block sizes**

Document for : **Decision**

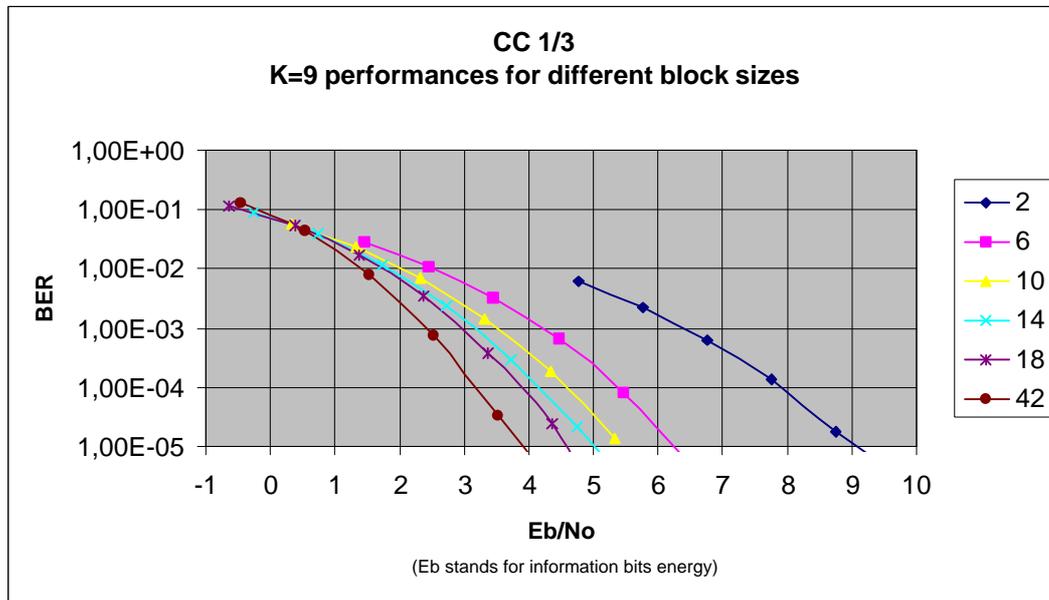
1. Introduction

Currently, three channel coding schemes have been defined in UTRA : no coding, convolutional coding (K=9), Turbo codes 8PCCC. WG1 had to provide scheme for encoding blocks between 1 and 5000 bits. However, neither 8PCCC nor convolutional codes are adapted to encode very short blocks (typically between 1 and 10bits). Thus there is a need to introduce such coding scheme. In particular it has been identified by WG2 that AMR commands would come in a separate TrCh and this provides an example of short blocks to be encoded in each TTI. In this document we propose to use the same code as the one used to encode TFCI to code blocks between 1 and 10 bits, since performance evaluation have already shown that it has good performance, and this has the advantage of adding no extra complexity in UTRA scheme.

2. Limit of convolutional coding in terms of coding block size

WG1 is supposed to provide channel coding schemes that cover encoding block sizes from 1 to 5000 bits. However, looking at the convolutional coding performance in terms of BER and FER when encoding block size decreases, there seems to be a limit where convolutional coding is not a efficient solution. At a 10⁻³ BER, the loss between a 2 bits and a 42 bits block size is 4dB. Between a 10 bits block and 42 bits block, the loss is 1 dB. This is shown on figure 1 that represents the BER versus Eb/No for different block sizes. Thus WG1 should define a new coding scheme which would code efficiently blocks of size between 1 and 10 bits.

In particular, it has been identified by WG2 that AMR mode commands would be transmitted in a separate Transport Channel. Given the amount of bits per TTI this represents, there is today a concrete need for definition of such coding scheme.



Simulation conditions :

- Convolutional Coding, rate 1/3, K=9
- No rate Matching (dummy bits inserted)
- Spreading Factor 256
- No power control
- Uplink channel
- 6 pilot bits
- One user

3. Proposal for coding scheme for coding blocks of 1 to 10 bits

The aim here is to find a coding scheme to encode blocks of 1 to 10 bits. It can be noted that the code for TFCI encodes from 6 to 10 bits into 30, and 1 to 5 bits into 15 in an efficient way. One simple solution would then be to use the same coding scheme for our purpose.

This would result in the following code definition.

3.1 Coding scheme for blocks of size 6 to 10 bits

The bits are encoded using (30, 10) punctured sub-code of the second order Reed-Muller code. The coding procedure is as shown in Figure 1.

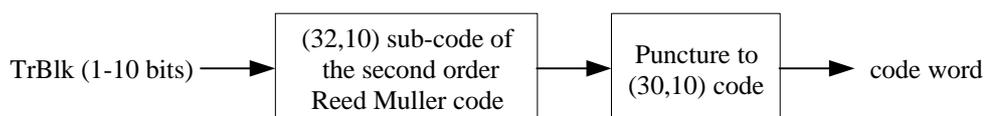


Figure 1: Channel coding bits

If the block consist of 6 to 9 bits, it is padded with zeros to 10 bits, by setting the most significant bits to zero. The receiver can use the information that not all 10 bits are used for this block, thereby reducing the error rate in the decoder.

Firstly, the block is encoded by the (32,10) sub-code of second order Reed-Muller code. The code words of the (32,10) sub-code of second order Reed-Muller code are linear combination of 10 basis sequences: all 1's, 5 OVFSF codes ($C_{32,1}$, $C_{32,2}$, $C_{32,4}$, $C_{32,8}$, $C_{32,16}$), and 4 masks (Mask1, Mask2, Mask3, Mask4). The 4 mask sequences are as following Table 1.

Table 1: Mask sequences

Mask 1	00101000011000111111000001110111
Mask 2	00000001110011010110110111000111
Mask 3	00001010111110010001101100101011
Mask 4	00011100001101110010111101010001

For information bits $a_0, a_1, a_2, a_3, a_4, a_5, a_6, a_7, a_8, a_9$ (a_0 is LSB and a_9 is MSB), the encoder structure is as following Figure 2.

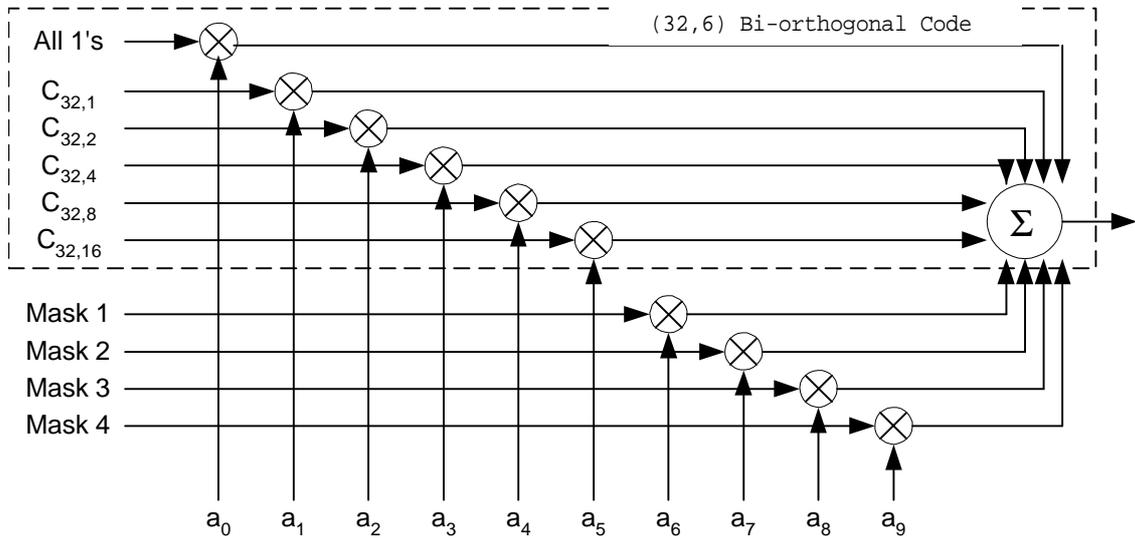


Figure 2: Encoder structure for (32,10) sub-code of second order Reed-Muller code

Then, the code words of the (32,10) sub-code of second order Reed-Muller code are punctured into length 30 by puncturing 1st and 17th bits.

Since the channel coding parameter is currently a static parameter for a TrCh, this code could be defined to encode from 1 to 10, to be able to be used for a TrCH whose rate vary within 1 to 10 bits per TTI.

3.2 Coding scheme for blocks of size 1 to 5 bits

If the block consist of 1 to 4 bits, it is padded with zeros to 5 bits, by setting the most significant bits to zero. The receiver can use the information that not all 5 bits are used for this block, thereby reducing the error rate in the decoder.

Blocks are encoded by biorthogonal (16, 5) block code. The code words of the biorthogonal (16, 5) code are from two mutually biorthogonal sets, $S_{C_{16}} = \{C_{16,0}, C_{16,1}, \dots, C_{16,15}\}$ and its binary complement,

$\bar{S}_{C_{16}} = \{\bar{C}_{16,0}, \bar{C}_{16,1}, \dots, \bar{C}_{16,15}\}$. Code words of set $S_{C_{16}}$ are from the level 16 of the code three of OVSF codes defined in document TS 25.213. The mapping of information bits to code words is shown in the Table 2.

Table 2: Mapping of information bits to code words for biorthogonal (16, 5) code

Information bits	Code word
00000	$C_{16,0}$
00001	$\bar{C}_{16,0}$
00010	$C_{16,1}$
...	...
11101	$\bar{C}_{16,14}$
11110	$C_{16,15}$
11111	$\bar{C}_{16,15}$

Biorthogonal code words, $C_{16,i}$ is then punctured into length 15 by puncturing the 1st bit.

4. Rationale for using the same code as the one used for TFCI

The ideas with proposing to use the same code as for TFCI are the following.

- First, this code has been chosen for its good performance among others. Some evaluations have already been performed on it, proving its performance.
- Second, since it is already used for TFCI, there is no complexity added to the system by using it also for regular channel coding scheme.

It might need to be studied further whether a coding scheme with less output bits would be needed, in which case the code proposed could be punctured at the expense of a performance degradation.

5. Conclusions

Nortel proposes to adopt the channel coding scheme already defined for TFCI coding, as a new additional coding scheme for UTRA. This would allow to cover the case of encoding blocks between 1 and 10 bits with reasonable quality and overhead, without adding any complexity to the system.