TSG-RAN Working Group 1(Radio) meeting #8 ***TSGR1#7(99)g31***
New York, USA, 12-15 Oct., 1999

Agenda Item: **Ad Hoc 10**

Source: **LG Information & Communications, Ltd.**

Title: **Questions and Answers about Time Delay between Physical Channels of Different Scrambling Codes**

Document for: **Decision**

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1. Introduction

The improved modulation scheme for Secondary Scrambling Code (SSC) named “Time Delay between Physical Channels for Different Scrambling Codes” was discussed during the TSG-RAN WG1 meeting #7 (30 Aug. – 3 Sep., 1999, Hannover, Germany) [1]. This document is the response to the questions raised by others companies [2].

The questions can be divided into two classes. Some questions are complexity issues and the others are performance issues. As the complexity issues, the structures of the transmitter and the receiver for the proposed method are described in Section 2, and the complexity increase due to the proposed method is summarized. The other questions about the structures of the transmitter and the receiver for the proposed method are also mentioned in Section 2.

2. Complexity Issues

2.1. Complexity increase in modulator

Figs. 1-2 show the modulator of the current method and the proposed method, respectively. In Figs. 1-2, L is the over-sampling ratio which is defined as the sampling ratio divided by chip rate and M is the number of SSC. In the proposed method, the output of spreader on SSC is delayed for a zero time interval or a half chip duration time interval. The delay interval for each SSC is set by the pre-defined manner or the signalling manner.

Now, we describe the increase of the complexity in transmitter due to the proposed method. One over-sampling unit and one delay unit are necessary for each spreader in order to delay the output of spreader as we can see from Fig 2. The adder operation rate increases from 1 operation/(chip duration) to 2 operations/(chip duration). Table 1 summarizes the transmitter complexity increase of the proposed method compared to the current method.

The implementation burden of over-sampler and delay unit is very small. And, the increase of adder operation due to the proposed method (1 additional operation per chip duration) is also very small compared to the total operations of modulator.

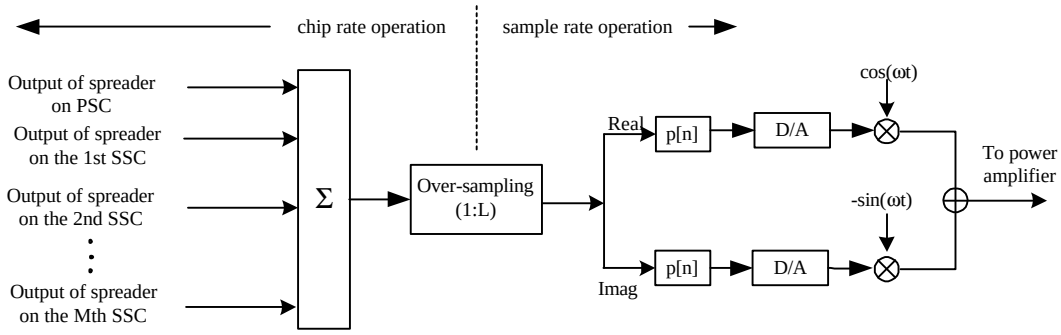

Figure 1. Modulator of the current method

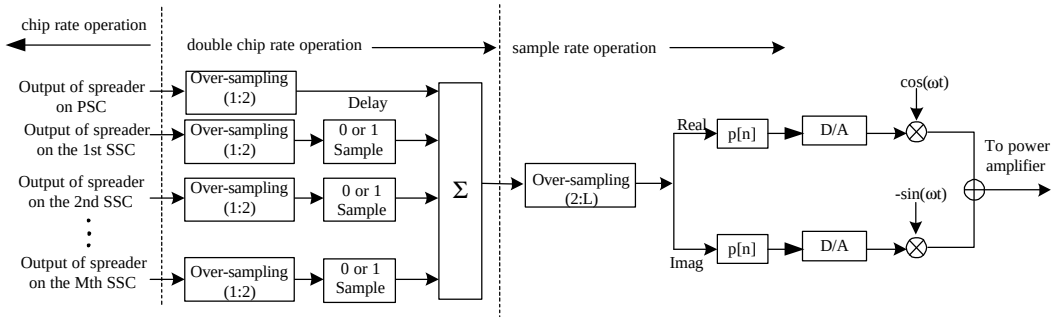

Figure 2. Modulator of the proposed method (implementation example)

Table 1. Complexity increase in modulator

Complexity	Currnet Method	Proposed Method
Over-sampler	1 unit	(M+2) units
Delay unit	•	M units
Adder operation per chip duration	1 operation	2 operations

2.2. Complexity in demodulator

Fig. 3 shows the demodulator of the current method. The operation of the under-sampling unit is decimation, i.e., the selection of one sample out of the successive L samples, and the decimation should maximize the desired user' signal energy. Assuming that x[n], n = 0,1,2,…, is the input sequence of the under-sampling unit, and y[n], n=0,1,2,…, is the output sequence of the under-sampling unit. Then, y[n] = x[L*n + j], n=0,1,2,…, where $0 \leq j < L$. The value of j should be set to maximize the desired user' signal energy.

In the current method, all signals from the same cell are transmitted with chip-synchronously. The under-sampling point that maximizes the signals from the desired cell is described as follows. Fig. 4 show the impulse response of the raised cosine filter with L = 4. In order to maximize the signal energy, the value of j should be set to be 0 since the maximum of the impulse response of the raised cosine filter is x[48 = 4*12 + 0].

In the proposed method, two kind signals exist even from the same cell. The one is the signal with zero time delay, and the other is the signal with a half chip duration time delay. For M = 1, the signal with zero time delay is the signal on Primary Scrambling Code (PSC), and the signal with a half chip duration time delay is the signal on SSC. Compared to the impulse response of the raised cosine filter due to the signal with zero time delay, the impulse response of the raised cosine filter due to the signal with a half chip duration time delay is also delayed for a half chip duration. It can be seen from Fig. 5. Therefore, if we assume that $y_1[n] = x[L*n]$ is the output sequence which maximizes the signal energy with zero time delay, then the output sequence, $y_2[n]$, which maximizes the signal energy with a half chip duration time delay is $y_2[n] = x[L*n + L/2]$.

The advantage of the proposed method is the reduction of interference power due to the signals with different time delay. At the output sequence, $y_1[n] = x[L*n]$, the component due to the signals with a zero time delay is maximized; but, the component due to the signals with a half chip duration time delay is not maximized. In the viewpoint of the signals with a zero time delay, the signals with a half chip duration time delay are only interference. So, the reduction of signal energy with a half chip duration time delay means the reduction of interference power due to the signals with a half chip duration time delay. This reduction of interference power can be achieved only by the proposed method. So, the reduction of interference power at the signals with a zero time delay (i.e., signals on PSC) is achieved in the proposed method. The above phenomena is also true for the output sequence $y_2[n] = x[L*n + L/2]$. So, the reduction of interference at the signals with a half time delay (i.e., signals on SSC) is achieved in the proposed method.

The implementation of the proposed method is very simple. The demodulator of the proposed method is shown in Fig. 6. We don't need to find the two under-sampling points separately. The under-sampling points for the signals with a half chip duration time delay is exactly L/2 samples later than the under-sampling points for the signals with a zero time delay. So, no other device for deciding the under-sampling points for the signals with a half chip duration time delay is required. Compared to the demodulator of the current method, only one unit (serial-to-parallel converter) is added in the demodulator of the proposed method as denoted in Table 2.

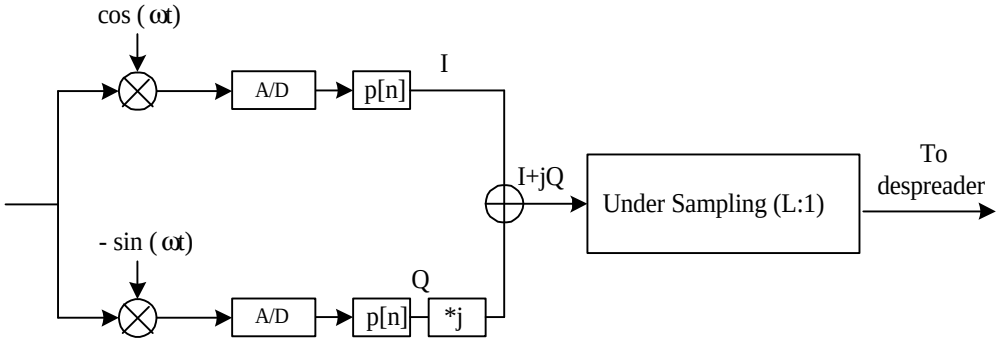

Figure 3. Demodulator of the current method

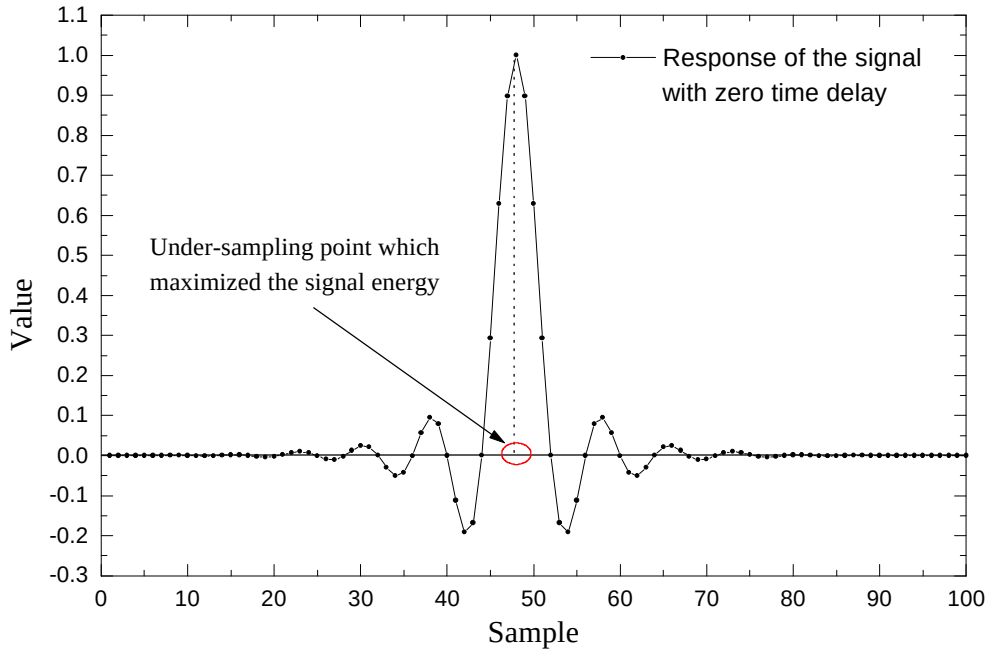

Figure 4. The response of the raised cosine filter

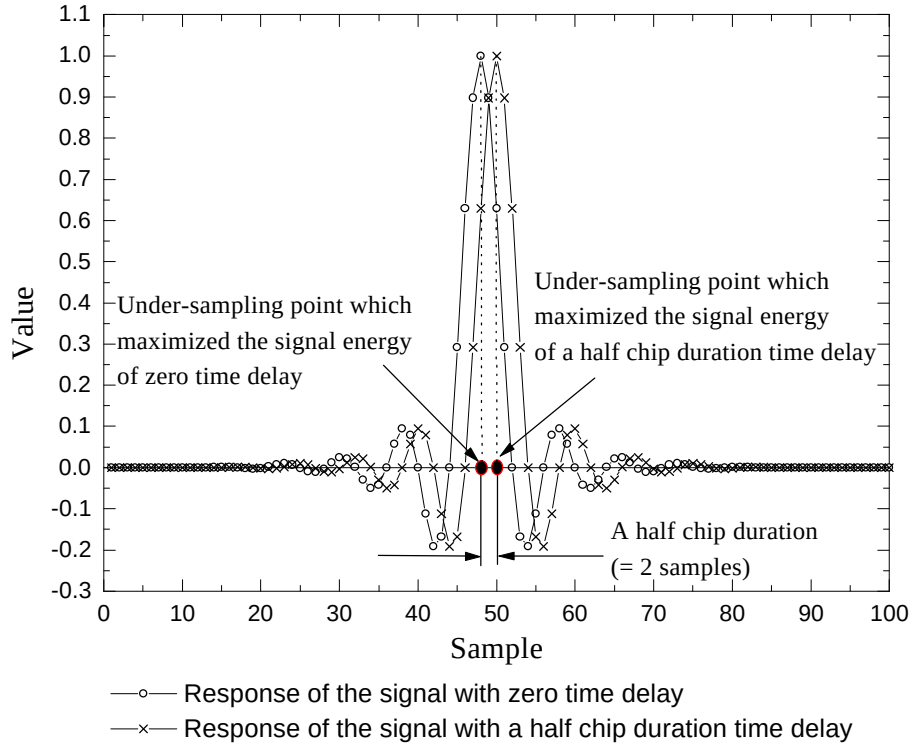

Figure 5. The response of the raised cosine filter (for two kinds signals)

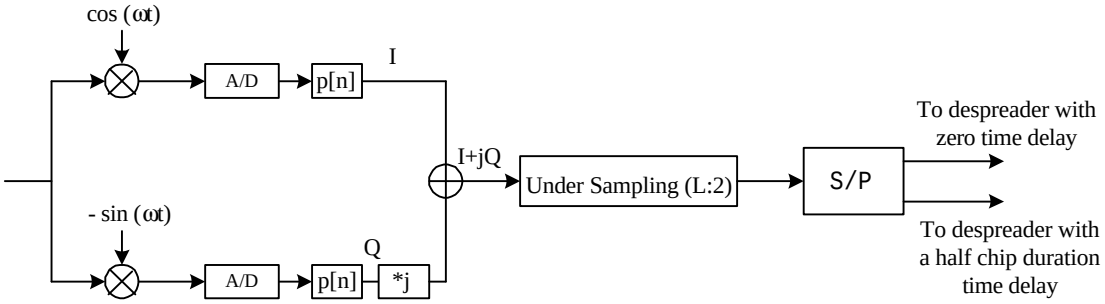

Figure 6. Demodulator of the proposed method (implementation example)

Table 2. Complexity increase in demodulator

Complexity	Current Method	Proposed Method
S/P	•	1 unit

2.3. Two concerns denoted in Ad Hoc 10 report.

Two concerns about this proposed method are denoted in Ad Hoc 10 report [2].

2.3.1. Timing management for secondary scrambling code

One concern is that “Timing management for the primary scrambling code and the secondary scrambling code may generate some issues for MS implementation and frame timing measurement function.”

We asked the meaning of “timing management” and “frame timing measurement function” to the questioner. His answer was as follows.

> MS should know the timing of PSC and SSC. I call this "Timing Management".
> Of course, I know that the timing between PSC and SSC is fixed value.
> MS should measure the frame timing difference between that of BTS1 which he belongs to and that of the neighboring BTS2 and report it to the BTS1 which transfers it to BTS2 in order to calculate the uplink spreading code timing by BTS2. I call this " frame timing measurement function".
> I think there may be no issues since timing relation between PSC and SSC is pre-designed and known one.

BTS give information of the timing of PSC and SSC to MS via pre-defined manner or signalling manner. The implementation example at MS regarding this timing management is shown in Fig. 6. If MS measure the frame timing difference based on the frame on PSC, there is no difference between the current method and proposed method.

2.3.2. Constellation of modulated signal

Another concern in [1] is that “The constellation of modulated signal at BTS may distort and modulation accuracy may be degraded when there is imbalance between PSC and SSC in terms of users.”

If we consider the signals with a zero time delay alone or the signals with a half chip duration time delay alone, there is no change in modulation process. The affect of the signals with a zero time delay (i.e., the signals on PSC) on the signals with a half chip duration time delay (i.e., the signals on SSC), is only multiple-access interference for both current and proposed methods. It also true for the affect of the signals with a half chip duration time delay. So, there is no cause for occurring problem in the constellation of modulated signal and modulation accuracy.

2.4. Other concern: Is there any change in Spectrum?

During the TSG-RAN WG1 meeting #7, a company raised the concern about the radio spectrum bandwidth of the proposed method. The concern was that the radio spectrum bandwidth of the proposed method become two times chip rate. The reason of this concern is that the data rate of input sequence of the pulse shaping filter is two times chip rate due to the proposed method. However, in fact, the data rate of the input sequence of the pulse shaping filter become L times chip rate due to the over-sampling, and L is always greater than or equal to 2 for both current and proposed method. So, there is no additional rate increase in input sequence of the pulse shaping filter due to the proposed method, and there is no increase in spectrum bandwidth.

Furthermore, the proposed method does not affect on the spectrum shape since the pulse shaping filter is linear system. The spectrum shape of the output sequence from linear system does not affected by the delay of input sequence.

3. Summary

The complexity increase due to the proposed method in transmitter and receiver is negligibly small (See Table 1,2).

4. References

[1] LGIC, “Time delay between physical channels of different scrambling codes,” TSGR1#7(99)b53, Hannover, Germany, Aug. 30-Sep. 3, 1999.

[2] AdHoc 10, “AdHOc 10 Report,” TSGR1#7(99)d29, Hannover, Germany, Aug. 30-Sep. 3, 1999.

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