TSG-RAN Working Group 1 meeting#7bis
Kyoungju, Korea, Oct. 4-5, 1999

TSG R1(99)F36

Agenda Item:

Source: CWTS WG1

Title: The Value of 1.28Mcps for Low Chip Rate TDD

Document for: Decision

1.Introduction

Based on the requirement from OHG meeting, the chip rate for 3GPP low chip rate TDD is decided as 1.28Mcps. Based on the simulation of 1.28Mcps and in view of the vendors and operators' benefits, the value of 1.28Mcps as the low chip rate in TDD mode is proposed in this proposal. The whole physical layer package of 1.28Mcps submit to RAN/WG1 is listed in Table 1 for consideration.

Table 1

Doc. Number	Doc. Name
R1-99f36	The value of 1.28Mcps for low chip rateTDD
R1-99f37	CWTS Specification TS C101
R1-99f38	CWTS Specification TS C102
R1-99f39	CWTS Specification TS C103
R1-99f40	CWTS Specification TS C104
R1-99f41	CWTS Specification TS C105
RP-99511	CWTS Specification TS C401
RP-99512	CWTS Specification TS C402

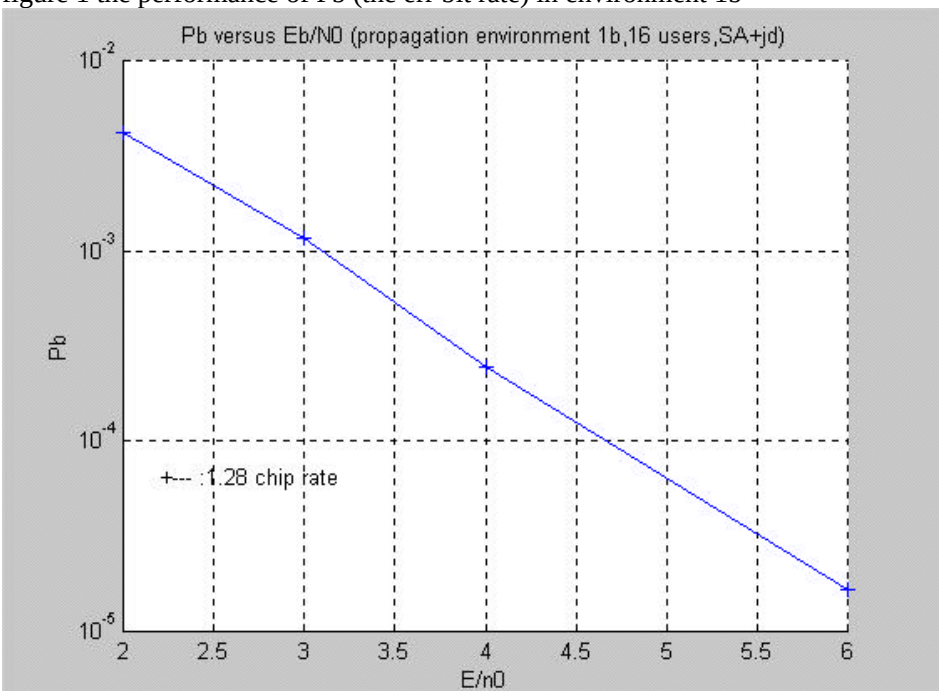
2.Result of Simulation

Based on the technologies of smart antenna, joint detection, synchronous CDMA and the new chip rate of 1.28Mcps, the link level simulation has been done with 16 users in active in any one time slot and without channel coding and interleaving. The simulation environments based on ITU M.1225: indoor (1b), outdoor to indoor(2b), vehicular (3a,3b).

The simulation results as follows show that the low chip rate TDD mode can provide high capacity.

a.indoor environment (1b)

figure 1 the performance of Pb (the err bit rate) in environment 1b



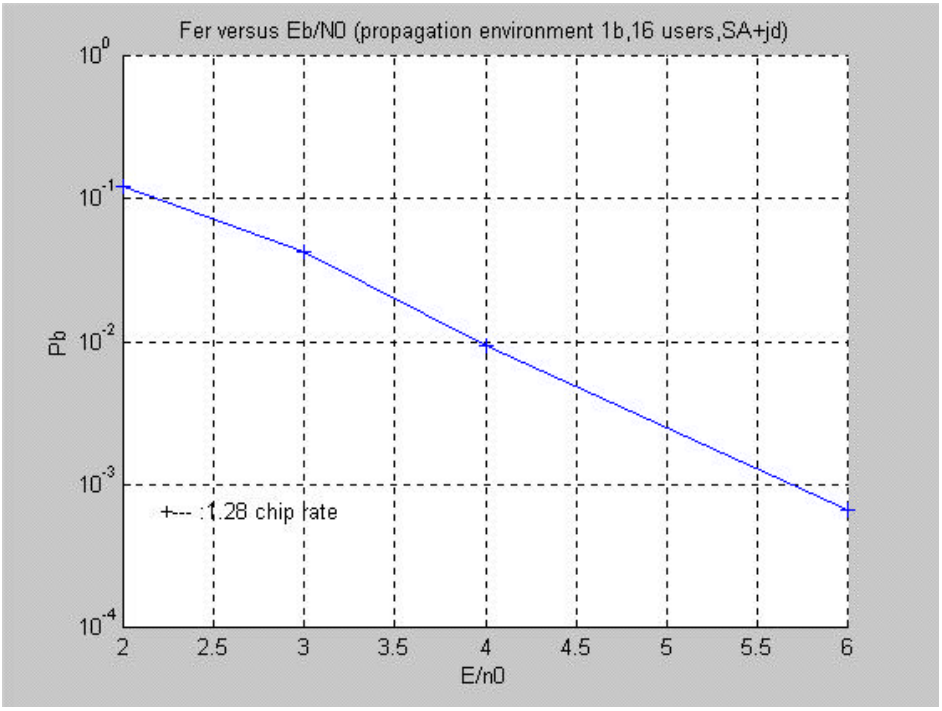


Figure 2 the performance of Fer (err frame rate) in environment 1b

b. indoor to out door and pedestrian

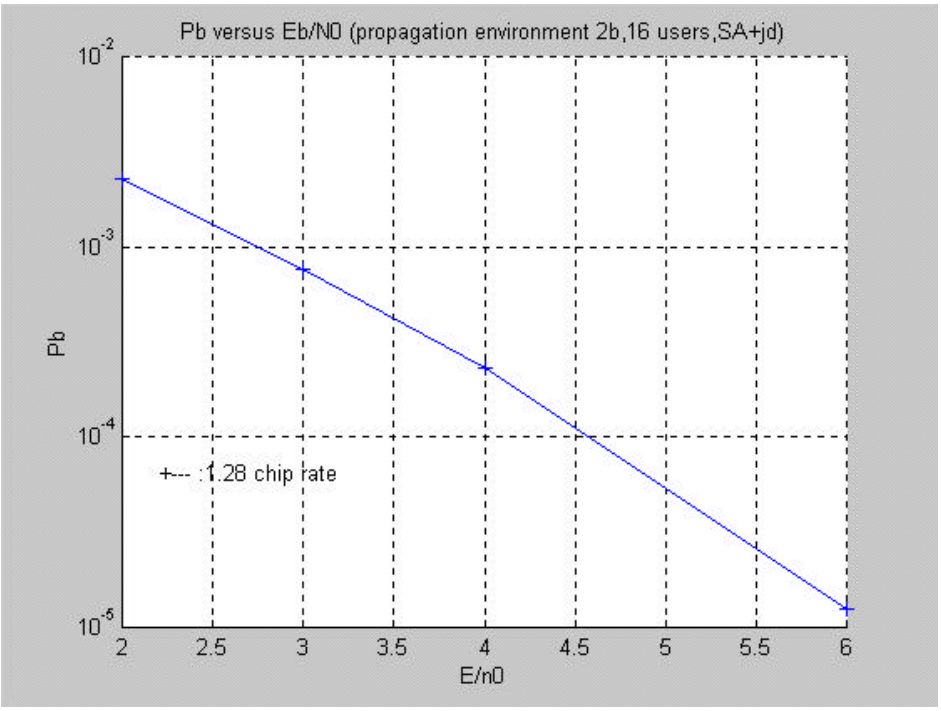


figure 3 the performance of Pb (the err bit rate) in environment 2b

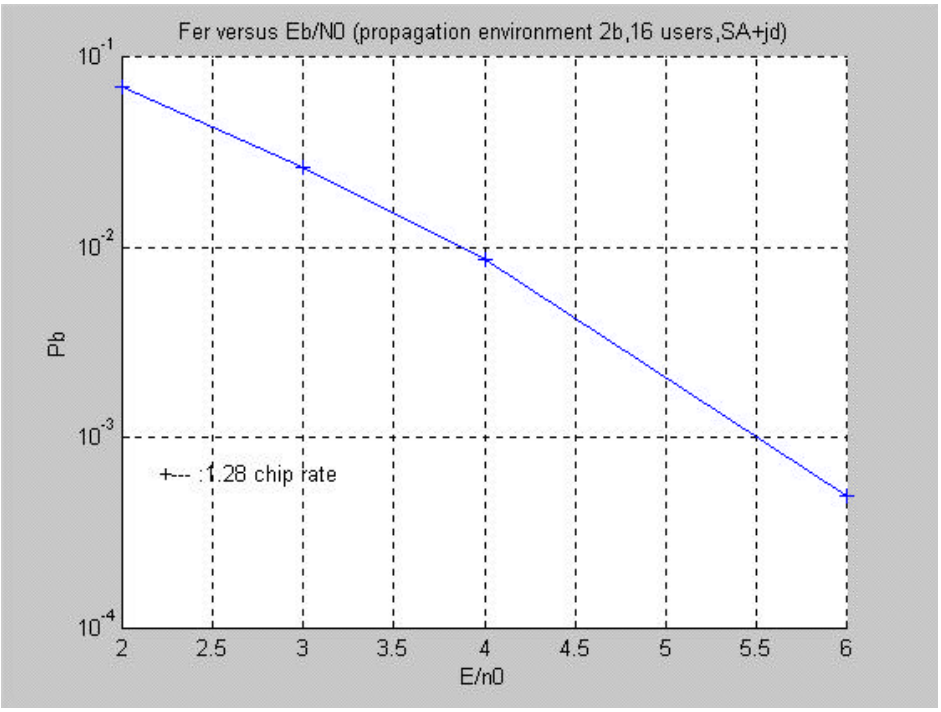


figure 4 the performance of Fer (err frame rate) in environment 2b

c.vehicle (3a,speed:50km/h)

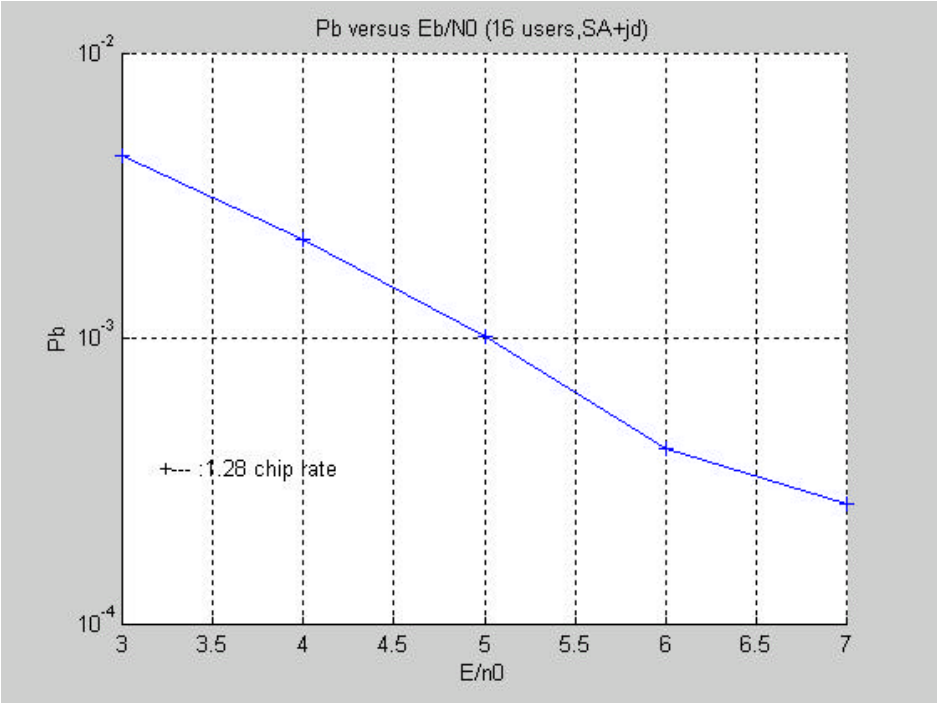


figure 5 the performance of Pb (the err bit rate) in environment 3a

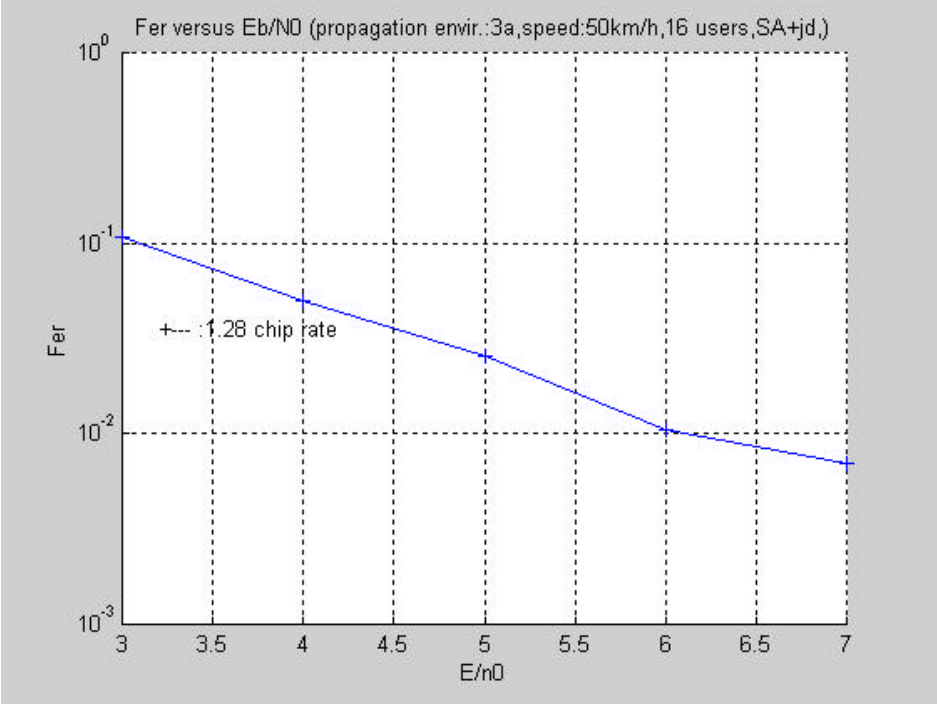


figure 6 the performance of Fer (err frame rate) in environment 3a

d. vehicle (3b,speed:120km/h)

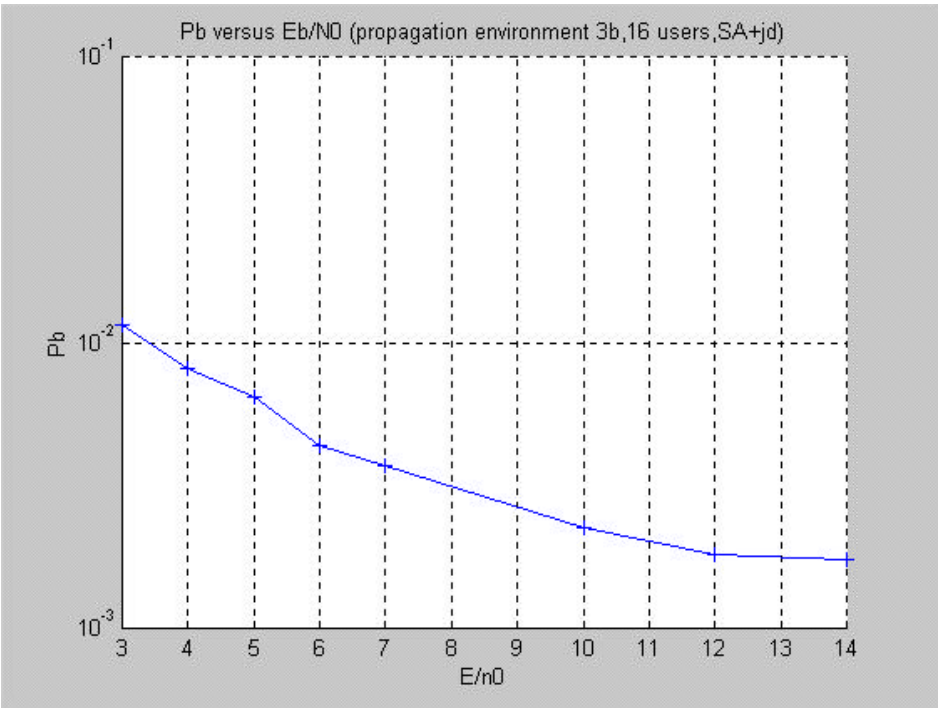


figure 7 the performance of Pb (the err bit rate) in environment 3b

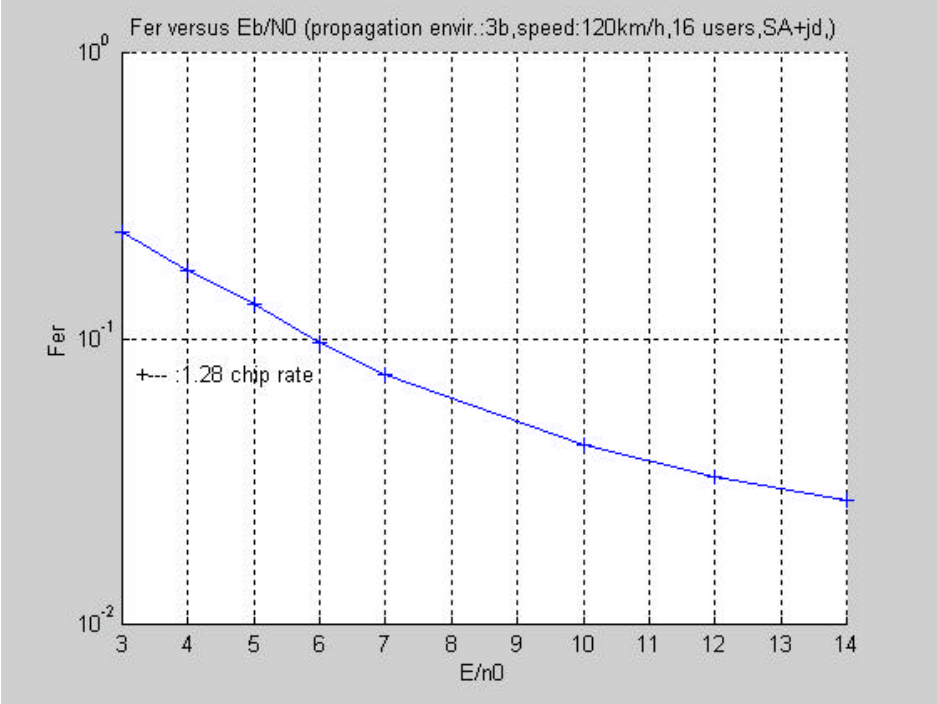


figure 8 the performance of Fer (err frame rate) in environment 3b

3. Conclusion

As the conclusion, CWTS propose to use 1.28Mcps as the value of low chip rate in UTRA TDD mode.