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Agenda Item: AH04
Source: Silicon Automation Systems Ltd.
Title: Text Proposal for 2nd interleaving
Document for: Decision

Introduction

This document proposes to modify 2nd interleaving. Due to reducing of the chip rate to 3.84Mcps, the number of slots per frame has changed to 15. In the present working assumption for 2nd interleaver, the number of columns of the rectangular matrix into which input sequence is written is 32. This was suitable for 16-slot structure. We propose to change the number of columns to 30 and the inter-column permutation pattern is changed accordingly without any change in complexity or degradation of performance.

Proposed Modifications

In the last WG1 meeting Inter-column permuting interleaver was chosen since it can reuse the same hardware as the 1st interleaver and also since there was no degradation in performance compared to the earlier MIL interleaver. Number of columns for the rectangular matrix was fixed to 32. The corresponding Inter-column permutation pattern was

{0, 16, 8, 24, 4, 20, 12, 28, 18, 2, 26, 10, 22, 6, 30, 14, 17, 1, 25, 9, 21, 5, 29, 13, 3, 19, 11, 27, 7, 23,15,31}

Since the number of slots was equal to 16, data bits from successive 2 columns will be mapped into one slot in the Physical Channel Mapping stage (assuming that the number of data bits exactly fits into all 32 columns).
Now since the number of slots have been changed to 15 because of change in chip rate, we propose that the number of columns for the rectangular matrix be changed to 30. The Inter-column permutation pattern has to be changed to
{0, 16, 8, 24, 4, 20, 12, 28, 18, 2, 26, 10, 22, 6, 14, 17, 1, 25, 9, 21, 5, 29, 13, 3, 19, 11, 27, 7, 23,15}

In the general case, even if the data bits do not fit fully into all columns, the change in number of columns does not affect the performance.

Text proposal for section 4.2.10 in TS 25.212

2nd interleaving

The 2nd interleaving of channel interleaving consists of two stage operations. In first stage, the input sequence is written into rectangular matrix row by row. The second stage is inter-column permutation. The two-stage operations are described as follows, the input block length is assumed to be K_2.

First Stage:

(1) Set a column number C_2 = ~~32~~30.
(2) Determine a row number R_2 by finding minimum integer R_2 such that,

$$K_2 <= R_2 \times C_2.$$

(3) The input sequence of the 2nd interleaving is written into the $R_2 \times C_2$ rectangular matrix row by row.

Second Stage:

(1) Perform the inter-column permutation based on the pattern $\{P_2(j)\}$ (j=0,1, ..., C-1) that is shown in Table 1where $P_2(j)$ is the original column position of the j-th permuted column.

(2) The output of the 2nd interleaving is the sequence read out column by column from the inter-column permuted $R_2 \times C_2$ matrix and the output is pruned by deleting the non-existence bits in the input sequence, where the deleting bits number l_2 is defined as:

$$l_2 = R_2 \times C_2 - K_2.$$

Table 1

Column number C_2	Inter-column permutation patterns
30	{0, 16, 8, 24, 4, 20, 12, 28, 18, 2, 26, 10, 22, 6, ~~30,~~ 14, 17, 1, 25, 9, 21, 5, 29, 13, 3, 19, 11, 27, 7, 23, 15, ~~31~~}

----------End of Text Proposal----------

NOTE: proper table numbering has to be given.

Reference

1. TS 25.212 V1.1.0 (1999-06) Multiplexing and channel coding (FDD).