

Agenda Item: AH15, AH03

Source: Panasonic (Matsushita Communication Industrial Co., Ltd.)

Title: Text Proposal for Timing relation of PRACH and AICH  
(25.211 7)

Document for: Discussion & Decision

### 1.Introduction

This document proposes to modify the timing relation between PRACH and AICH. Due to reducing of the chip rate to 3.84[Mcps], the length of a slot was extended to 0.666[ms]. The length of access slot should also be modified, and it is necessary that the timing relation of PRACH and AICH will be revised. Currently there are two candidates of access slot structure (7 access slots within 1 frame and 15 access slots within 2 frames) on the reflector. Therefore this document gives two text proposal correspond to the two candidates.

### 2.Proposed Modifications

Currently the timing offset between PRACH and AICH ( $T_a$ ) has been defined to 0.5ms. From implementation point of view, the value of 0.5ms is not reasonable. Because it is not directly related to slot period and frame period. And there is no strong reason to persist in 0.5ms. On these reasons, this document proposes to change  $T_a$  to 1 slot duration ( $=0.666$ ms). And the other time parameters should also be modified to fit new access slot structure. At present there are two candidates of access slot structure which are 15 access slots within 2 frames and 7 access slots within 1 frame. Fig.1 and Fig.2 are shown the former as example. In the later, some of the time parameters will be extended for 1 time slot duration at frame boundary. But in the both candidates, all of time parameters( $T_a$ ,  $\tau_{p-p}$ ,  $\tau_{p-m}$ ,  $\tau_{p-a}$  and  $\tau_{a-p}$ ) could be defined as multiple of time slot.

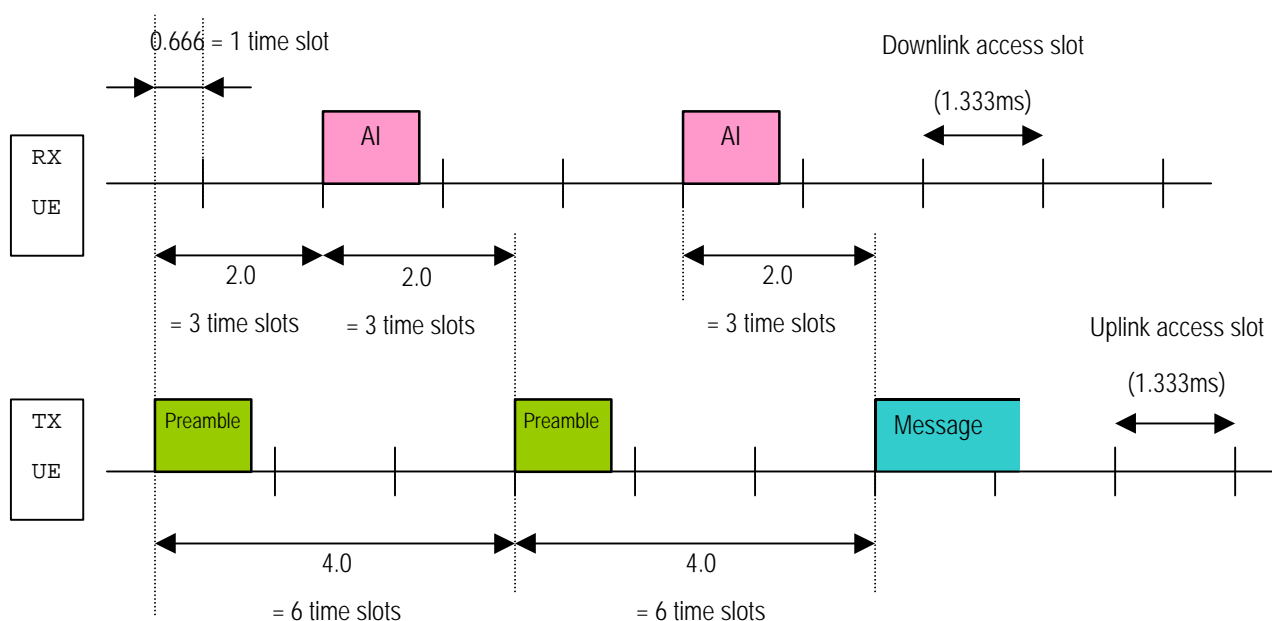
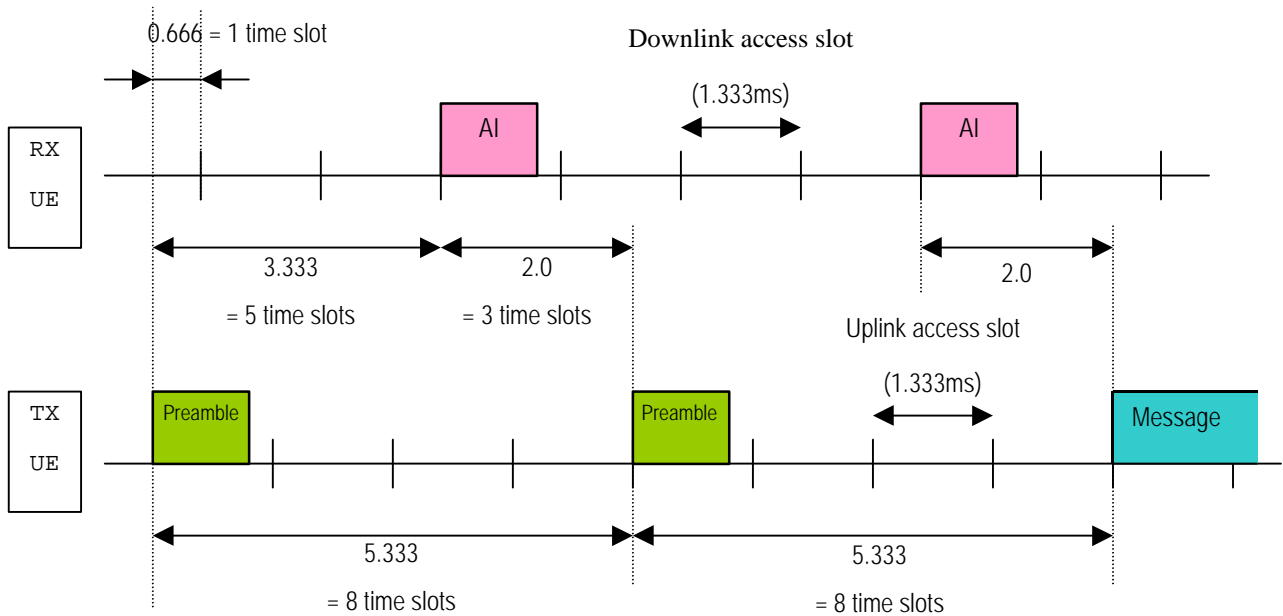


Fig.1 Timing of PRACH and AICH transmission in the case of 15 access slots within 2 frames as seen by the UE, with AICH transmission timing set to 0.



**Fig.2 Timing of PRACH and AICH transmission in the case of 15 access slots within 2 frames as seen by the UE, with AICH transmission timing set to 1.**

### 3.Text Proposal

Two text proposals of new timing relations of PRACH and AICH were prepared below. The former is the case of 7 access slots within 1 frame, and the later is the case of 15 access slots within 2 frames. Either one will be valid depending on the decision of access slot structure. Please note, following text proposals were edited only "PRACH/RACH timing relation:" part.

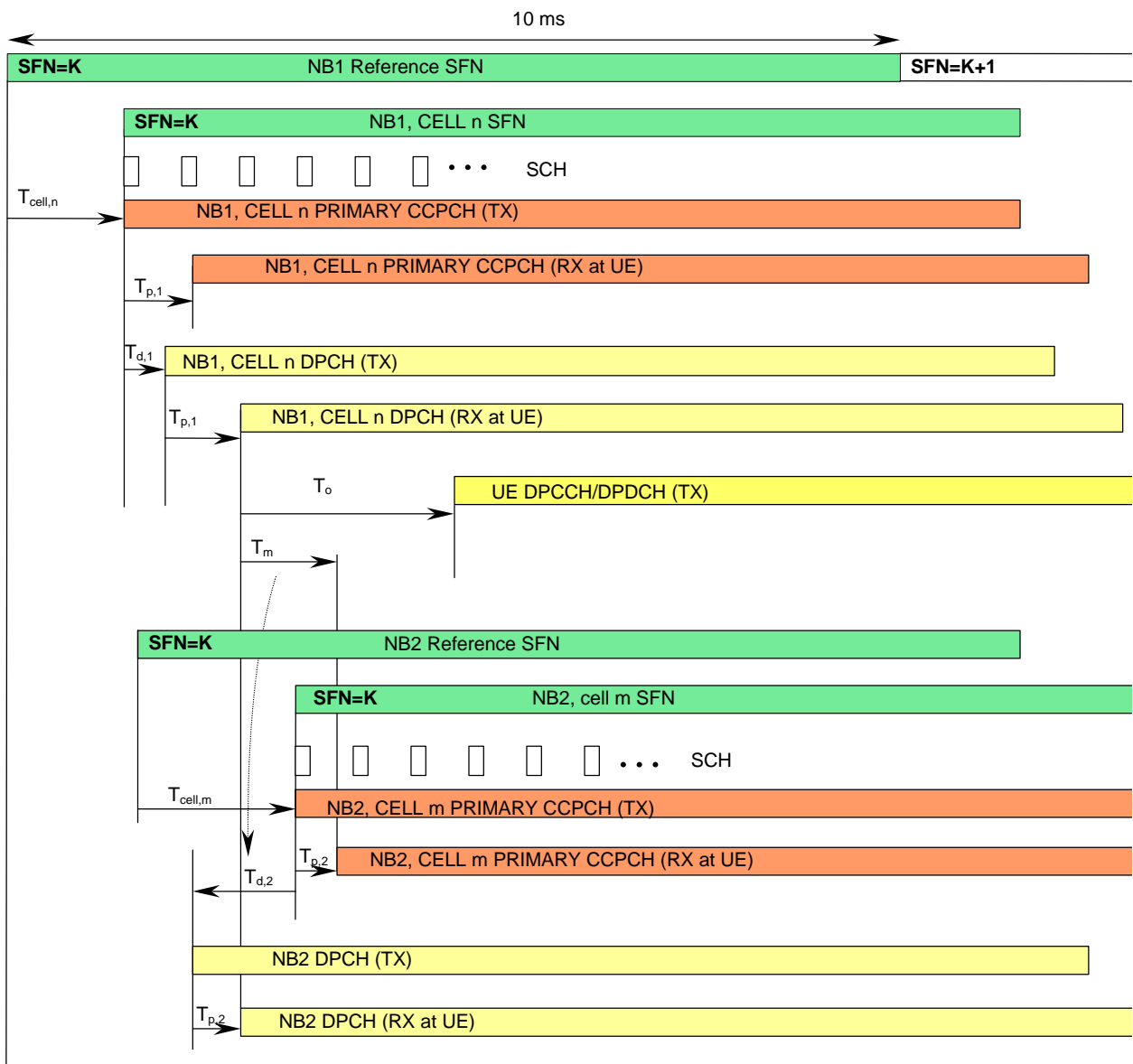
----- Modifications to TS25.211, Chapter 7 in the case of 7 access slots within 1 frame -----

## 7 Timing relationship between physical channels

<Editors note:  $M=36864=512*72$  needs to be confirmed.>

In general, a Node B covers  $N$  cells, where  $N \geq 1$ . Each Node B has a Reference System Frame Number (SFN), which counts from 0 to  $M-1$  in Radio Frame (10 ms) intervals.  $M$  is a multiple of the superframe (72), and is TBD. The purpose of the Reference SFN is to make sure that the correct frames are combined at soft handover. Each cell has a Cell SFN, which is broadcast on the BCH.

Figure 27 shows the proposed physical channel timing parameters in a soft handover situation including two Node Bs, NB1 and NB2. The timing parameters in Figure 27 refer to frame-timing.



**Figure 27: Physical channel timing relations.**

The parameters in Figure 27 are explained below:

- $T_p$ : Propagation delay between Node B and UE.
- $T_{cell}$ : This timing offset is used for the frame timing of SCH, Primary CCPCH and the starting phase of all downlink scrambling codes in a cell. The resolution is TBD and depends on the maximum expected time-dispersion. The range is one slot.  $T_{cell}$  is also the reference frame timing for the PRACH.  
<Editors note: Descriptive text: The main purpose of  $T_{cell}$  is to avoid overlapping SCHs in different cells belonging to the same Node B. The resolution affects the number of possible cells in a Node B.>
- $T_d$ : This timing offset is used for the frame timing of DPCHs and Secondary CCPCHs. It can be individually set up for each DPCH and Secondary CCPCH. The  $T_d$  values for the latter may be broadcast on the BCH, or known a-priori. The resolution is 256 chips in order to maintain downlink orthogonality and the range is TBD.  
<Editors note: Descriptive text: The purpose of  $T_d$  is:  
- In an originating/terminating cell, to distribute discontinuous transmission periods in time, and also to distribute Node B-RNC transmission traffic in time.  
- At soft handover, to synchronise downlink DPCHs to the same UE, in order to minimise the buffering requirements at the UE.>

- $T_o$ :** This constant timing offset is used to set up the transmission frame timing of an uplink DPCCCH/DPDCH in the UE. The value is TBD. The starting phase of the uplink scrambling code is synchronised with the uplink DPCCCH/DPDCH frame timing.  
 <Editors note: Descriptive text: The uplink DPCCCH/DPDCH transmission frame timing should be set to  $T_o$  seconds after the frame timing of the earliest received path of the downlink DPCH.  $T_o$  should be chosen to minimise the closed loop PC delay in as large cell-radii as possible.>
- $T_m$ :** This value is measured by the UE and reported to the RNC prior to soft handover. The RNC can then notify this value to the target cell, which then knows how to set  $T_d$  to achieve proper reception and transmission frame timing of the dedicated physical channel.  
 <Editors note: Descriptive text: Note that since the UE reports the value  $T_m$  as the time-difference between the received Primary CCPCH frame-timing from the target cell and the earliest received existing DPCH path, the propagation delay to the target cell is already compensated for in the setting of  $T_d$  at the target cell. The DPCH signal from the target cell will reach the UE at the same time as the earliest received existing DPCH path. The only remaining error, besides frequency-drift and UE mobility related errors, is due to a (known) rounding error at the target cell in order to maintain downlink orthogonality.>

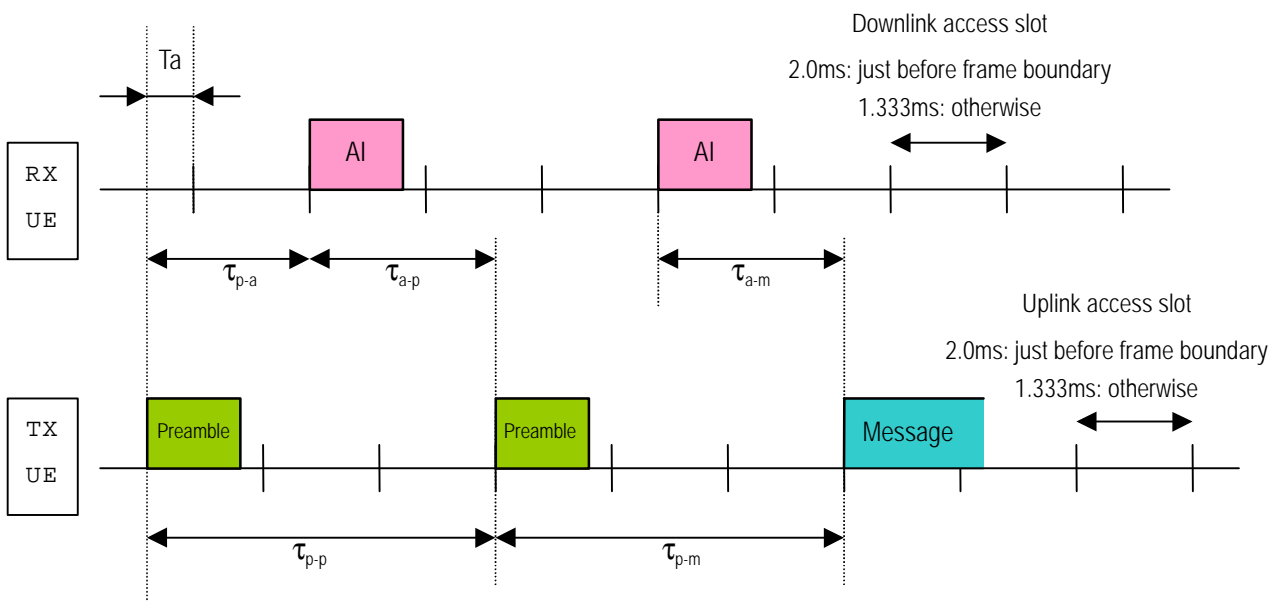
**DSCH timing:**

The relative timing between a DSCH and DCH is given as follows:

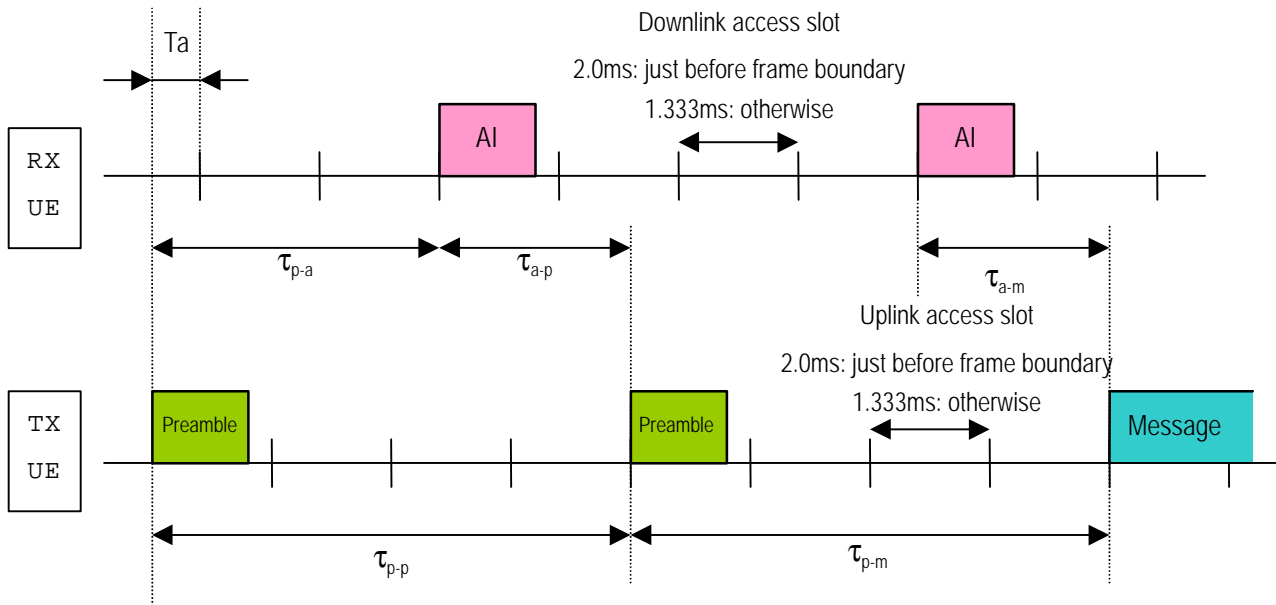
DSCH timing is identical to the cell primary CCPCH

DCH timing is asynchronous with max 1 slot (0.625 ms) ahead or max 15 slots (15 times 0.625 ms) behind. This determines explicitly which frame on DSCH carries the user data based on the TFCI or higher layer signaling on DCH.

**PRACH/RACH timing relation:**



**Figure 28: Timing of PRACH and AICH transmission as seen by the UE, with AICH transmission timing set to 0.**



**Figure 29: Timing of PRACH and AICH transmission as seen by the UE, with AICH transmission timing set to 1.**

Figure 28 and Figure 29 illustrate the timing relation between PRACH and AICH as seen by the UE, with AICH transmission timing set to 0 and 1, respectively. The timing figures define the case where all access slots are available. If not all access slots are available, Figure 28 and Figure 29 define the minimum values for  $\tau_{p-p}$ ,  $\tau_{p-m}$ ,  $\tau_{p-a}$  and  $\tau_{a-p}$ .

- Both uplink and downlink access slots of length 2.0ms just before frame boundary and otherwise 1.333ms are defined.
- For each downlink access slot there is a corresponding uplink access slot.
- The preambles are to be transmitted time aligned with the uplink access slots.
- The downlink access slots are transmitted time aligned with the PCCPCH frame boundary.
- An uplink access slot is transmitted a specified time  $\tau_{p-a}$  before the corresponding downlink access slot.
- Subsequent preambles can be transmitted either three or four access slots after the latest transmitted preambles ( $\tau_{p-p}$  is either 3 or 4 access slots), depending on the AICH transmission timing value.
- The message can be transmitted either three or four access slots after the latest transmitted preamble ( $\tau_{p-m}$  is either 3 or 4 access slots), depending on the AICH transmission timing value.

The timing offset ( $T_a$ ) between uplink and downlink access slots, as seen by the UE, is same with 1 slot duration of 0.666ms.

The timing of preamble-to-AICH ( $\tau_{p-a}$ ) has ~~four~~ two alternative values: 2.666ms when there is frame boundary during  $\tau_{p-a}$  and otherwise 2.0ms, or 4ms when there is frame boundary during  $\tau_{p-a}$  and otherwise 3.333ms, depending on the AICH transmission timing value.

The timing of AICH-to-preamble ( $\tau_{a-p}$ ) has ~~two~~ one alternative values: 2.666ms when the corresponding preamble belongs to the next frame, and otherwise 2ms.

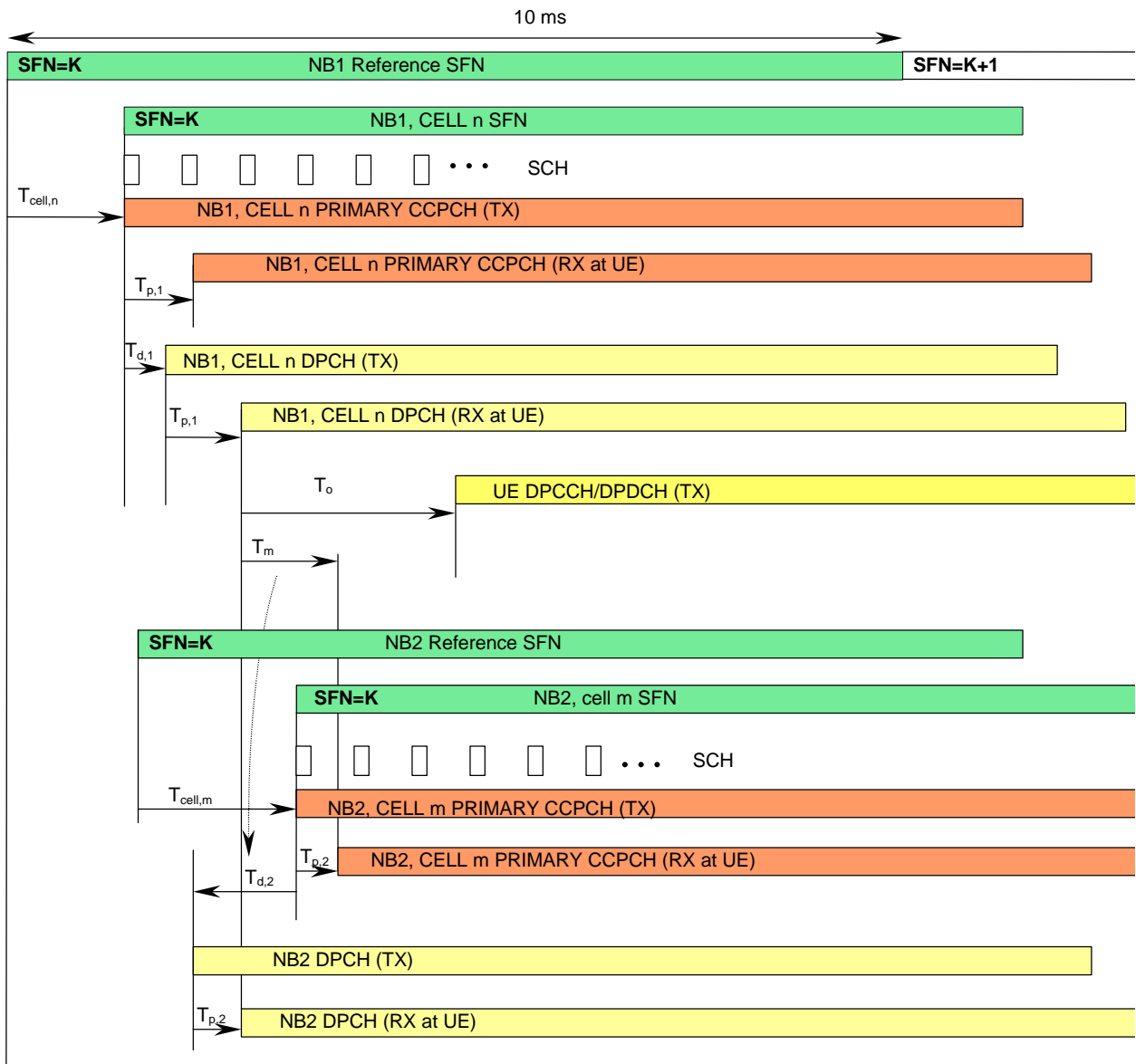
The timing of AICH-to-message ( $\tau_{a-m}$ ) has ~~two~~ one alternative values: 2.666ms when the corresponding message belongs to the next frame, and otherwise 2ms.

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- The message can be transmitted either three or four access slots after the latest transmitted preamble ( $\tau_{p-m}$  is either 3 or 4 access slots), depending on the AICH transmission timing value.

The timing offset ( $T_a$ ) between uplink and downlink access slots, as seen by the UE, is same with 1 slot duration of 0.6660.5ms

The timing of preamble-to-AICH ( $\tau_{p-a}$ ) has two alternative values: 2.0475ms or 3.3333ms, depending on the AICH transmission timing value.

The timing of AICH-to-preamble( $\tau_{a-p}$ ) has one value: 2ms.

The timing of AICH-to-message( $\tau_{a-m}$ ) has one value: 2ms.