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Agenda item: 16

Source: Ericsson

Title: Updated text proposal for Paging Structure

Document for: Decision

Introduction

This paper presents an updated text proposal for the Page Indicator Channel.

The original proposal for a modified paging structure [1] included the time multiplex of Acquisition Indicators and Page Indicators on an Indicator Channel (ICH). This proposal was motivated from the fact that there is already "spare" capacity on the AICH. Although the proposal to time multiplex the Page and Acquisition Indicators was not agreed upon, the text in 25.211 was written in such a way that a merge of the PICH and the AICH should be straightforward. As an example, "Access slots" were defined also for the PICH, although they do not serve any function for the PICH itself.

With a change of chip rate to 3.84 Mcps and 15 slots per frame, the exact timing structure for the AICH is under discussion. Some of the proposals include structures that are not identical for even and odd frames. This makes it less attractive to time multiplex AICH and PICH if the10 ms Page Messages is to be kept. Furthermore, as the exact power needed for AICH and PICH is not known, it is actually not clear that a time multiplex of the AICH and PICH will lead to lower peak-power requirements. This is only true when the energy needed for the PICH is noticeably lower than the energy needed for the AICH. Therefore we propose that the PICH structure of 25.211 is kept, i.e. AICH and PICH should be separate physical channels and should not be time-multiplexed. As a result of that, we propose a somewhat modified description of the PICH, where e.g. Access slots are no longer defined for the PICH.

A further advantage with a separate physical channel for the Page Indicators is that the number of Page Indicators per frame may be significantly larger. This implies that the risk that the UE will wake-up as the result of a Page Indicator set to notify a different UE is reduced, with an increased stand-by time as a consequence.

It should be noted that the general benefits of a separate channel for Page Indicators, in terms of peak-power and code usage, is still significant, compared to the previous paging scheme.

PICH structure

With a separate PICH code with SF=256, there are 300 bits (150 symbols) per frame. It is very beneficial to have the possibility to vary the number of bits per PI, in order to have a flexible trade-off between the number of Page Indicators per frame, i.e. sleep-mode efficiency, and the power that needs to be allocated to the PICH. Therefore we suggest that only 288 bits (144 symbols) are used to carry the PI. The number of PI per frame can then be 18, 36, 72, or 144, with each PI mapped onto 2, 4, 8, and 16 consecutive bits respectively.

There is also a need to define the timing between the PICH and the associated S-CCPCH that carries the actual Page Messages. The timing should be chosen so that there is sufficient time to process the Page Indicators before a potential Page Message on the S-CCPCH is to be received. We propose 3 slots, i.e. similar to the timing between the Page Indicator and the Message part in the old Page scheme. A corresponding section should be added to Section 7 of 25.211.

We also propose that the comment in 25.211, section 5.3.3.7 "The phase reference for the PICH is the pilot symbols of the downlink PCCHPC" is removed. First, the phase reference should be the common pilot and not the PCCHPC. Furthermore, that the common pilot is the phase reference for the PICH as well as all other DL channels should be clear

from the description of the common pilot and does not need to be mentioned separately for each downlink physical channel.

We also propose that Section 4.2.15.2 in document 25.212 is removed. The description of that section is clearly not a coding procedure and the procedure is anyway described in document 25.214.

Finally, we would like to point out that the spreading/modulation of the PICH (as well as the AICH and the SCCPCH) should be described in a figure similar to Figure 11 of 25.213 (perhaps included in Figure 11). However, we do not provide text proposal for this within this document.

--- Text proposal ---

Text proposal for 25.211, Section 5.3.3.7

5.3.3.7 Page Indicator Channel

The Page Indicator Channel (PICH) is a fixed rate (SF=256) physical channel used to carry the Page Indicators (PI). The PICH is always associated with an S-CCPCH to which a PCH transport channel is mapped.

Figure 1 illustrates the frame structure of the PICH. One PICH frame of length 10 ms consists 300 bits. Of these, 288 bits are used to carry Page Indicators. The remaining 12 bits are not used.

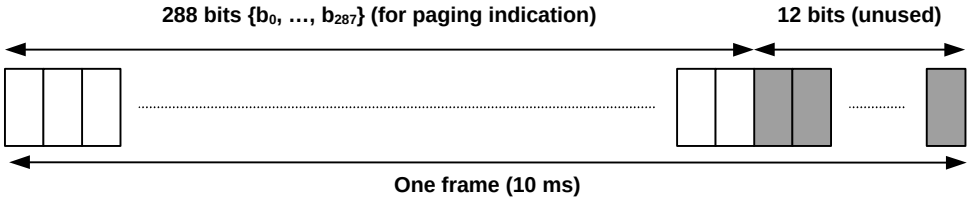


Figure 1 Frame structure of Page Indicator CHannel (PICH)

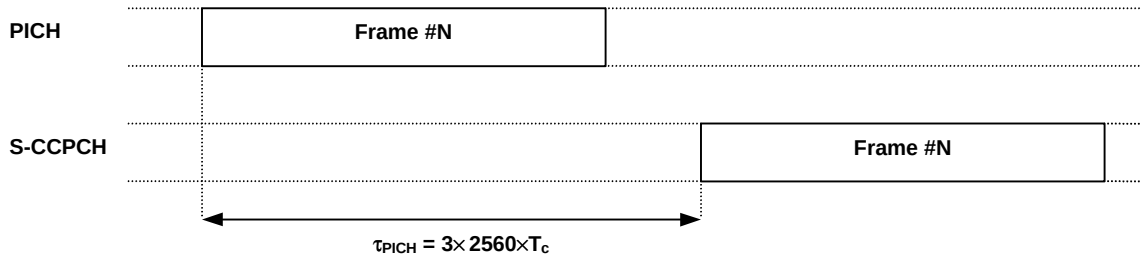
N Page Indicators $\{PI_0, \ldots, PI_{N-1}\}$ are transmitted in each PICH frame, where N=18, 36, 72, or 144. The mapping from $\{PI_0, \ldots, PI_{N-1}\}$ to the PICH bits $\{b_0, \ldots, b_{287}\}$ are according to table 1.

Number of PI per frame (N)	$PI_i = 1$	$PI_i = 0$
N=18	$\{b_{16i}, \ldots, b_{16i+15}\} = \{1,1,\ldots,1\}$	$\{b_{16i}, \ldots, b_{16i+15}\} = \{0,0,\ldots,0\}$
N=36	$\{b_{8i+}, \ldots, b_{8i+7}\} = \{1,1,\ldots,1\}$	$\{b_{8i}, \ldots, b_{8i+7}\} = \{0,0,\ldots,0\}$
N=72	$\{b_{4i}, \ldots, b_{4i+3}\} = \{1, 1,\ldots,1\}$	$\{b_{4i}, \ldots, b_{4i+3}\} = \{0, 0,\ldots,0\}$
N=144	$\{b_{2i}, \ldots, b_{2i+1}\} = \{1,1\}$	$\{b_{2i}, \ldots, b_{2i+1}\} = \{0,0\}$

Table 1 Mapping of Page Indicators (PI) to PICH bits

Text proposal for 25.211, Addition to Section 7

Figure 3 illustrates the timing between an S-CCPCH frame and the corresponding frame of an associated PICH. The frame of the associated PICH precedes the corresponding S-CCPCH frame by $\tau_{PICH} = 3 \times 2560 \times T_c$, where T_c is the time per chips.



Text proposal for 25.212, Section 4.2.15.2

Remove Section 4.2.15.2 PI part

References

[1] 3GPP TSG RAN WG#1, “Proposal for a modified PCH structure, TSGR1#5(99) 604”