TSG-RAN Working Group1 meeting #6
Espoo, Finland, 13-16, July 1999

***TSGR1#6(99)869***

**Agenda Item:** **Adhoc 14**

**Source:** **SAMSUNG Electronics Co.**

**Title:** **Further clarifications to the gain for the DPCCH gating in COS**

**Document for:** **Discussion**

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## 1. Introduction

In the last 3GPP WG1#5 Cheju meeting, SAMSUNG presented some link-level simulation results for various gating rate. Nokia asked questions about searcher performance during gated transmission of DPCCH in Control Only Substate(COS). There was also some questions and comments about the net interference reduction gain especially from Nokia and Ericsson. In this paper, we clarifiy and correct interference reduction gain with more specific calculations. We also prepared more detail explanation about searcher operation for DPCCH gating.

## 2. E-mail discussions about interference reduction gain
## 2.1 Questions

Date: Mon, 28 Jun 1999 14:00:39 +0200
From: Erik Dahlman <Erik.Dahlman@ERA-T.ERICSSON.SE>
Subject: Re: AH14, DPCCH gating E-mail discussion kick-off

I do not fully understand how you calculate the overall uplink interference reduction in R1(99)669 (or below) from the uplink DPDCH performance loss.

As far as I understand, the DPDCH loss is due to
- Reduced UL PC performancem due to lower PC rate on DL.
- Reduced UL channel estimation.

However, this loss only affects the uplink interference when the DPDCH is actually transmitted, while the gain due to gating affects the uplink interference when the DPDCH is not transmitted, i.e. when gating is used. So how can you add the gain and loss together to get a overall gain? As ar as I understand, the overall gain should depend on the DPDCH duty cycle, i.e. how often the DPDCH is actually transmitted.

Mayby this has something to do with the correction you made based on Ms. Virtanen's comment. However, I still do not really understand.

## 2.2 Uplink interference reduction gain

The understanding of above question is right because the overall interference reduction gain depends on the duty cycle of DPDCH. In this paper, we re-calculate the overall interference reduction gain(table 3 in Tdoc R1(99)669).

Assume,

**DPDCH duty cycle = 1%,**
**Power of DPCCH = P,**
**Power of DPDCH = 2P**

Required total power(DPCCH+DPDCH) when no gating is

**99 * P + 1 * (P + 2P) = 102 P**

For the 1/2 gating in 3km/h case, there is a 0.2dB loss in BER when only DPCCH is transmitted (see Fig. 2 in Tdoc 669). Therefore, the required power of DPCCH during DPCCH only transmission is

**99 * P * 0.5 * 1.05 = 51.98 P ,** where 0.5 is due to 1/2 gating

During DPDCH transmission, there is 0.71 dB loss, so the required power is

**1 * (P + 2P) * 1.17 = 3.52 P**

We can re-caculate the overall gain as followining,

**Overall Gain = 10 * log10 ( 102P / (51.98P + 3.52P)) = 2.68 [dB]**

Based on the above method, we re-caculate the table 3 in Tdoc R1(99)669

| $f_d$ [Hz] | Gating rate | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 1/2 | | | 1/4 | | | 1/8 | | |
| | DPDCH existing | DPDCH not existing | inter. reduction gain[dB] | DPDCH existing | DPDCH not existing | inter. reduction gain[dB] | DPDCH existing | DPDCH not existing | inter. reduction gain[dB] |
| 5.6 | 0.71 | 0.2 | **2.68** | 1.84 | 0.5 | **5.00** | 3.76 | 1.4 | **6.23** |
| 56 | 1.07 | 0.8 | **2.08** | 1.96 | 1.5 | **4.10** | 2.65 | 1.5 | **6.46** |
| 222 | 0.56 | 0.5 | **2.39** | 1.43 | 0.5 | **5.05** | 1.78 | 0.5 | **7.44** |

- DPDCH existing: Performance loss compared with no gating(gating rate=1/1) when DPDCH is existing
- DPDCH not existing: Performance loss compared with no gating(gating rate=1/1) when DPDCH is not existing(DPCCH only transmition)
- inter. reduction gain : overall interference reduction gain

**Table 3. Uplink interference reduction [dB]**

## 3. Is there performance degradation in the searcher operation during gating?

**Answer**) There is no performance degradation of the UE searcher performance due to continuously transmitting Common Pilot channel(CPICH) which is a new downlink physical channel used by UE to perform searching, channel tracking, and channel estimation[2]. Therefore, we focus the base station searcher operation.

By using the gated transmission in the uplink DPCCH, the searchers in the base station demodulator do not have signals during the gate-off period. However, if we consider the buffering of the gate-on period signal and searching operation over the buffered signal samples, i.e off-line searcher processing, searchers can be operated during the gate-off period. Actually, the efficiency of the searcher operation depends on the base station implementation. In most of cases, searchers can not cover all hypothesis in the window at one time, we can avoid search performance degradation with buffered operation. Therefore, this is not a significant issue for considering uplink/downlink DPCCH gated transmission.

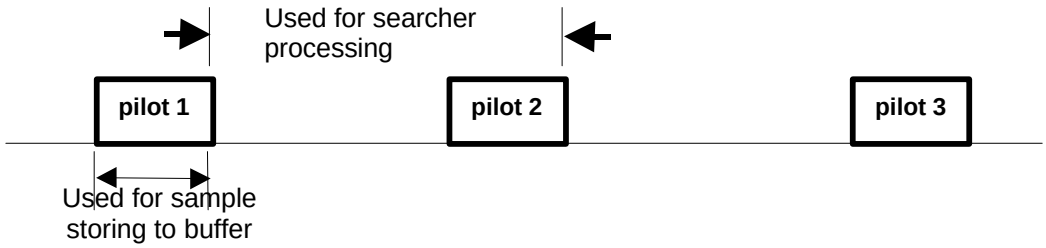


**Figure 1. Explanation for the searcher operation in the Base station receiver for the Control Only Sub-state**

## 4. Coclusion

Of course, the above gain depends on the duty cycle of DPDCH. However, Control Only Subtate(COS) is the state which has no traffic but only control information. If there is a traffic to send, they must go to user data active state. So, we think the duty cycle of DPDCH is less than 1%.

The COS is very important state because this is the last state which keep the link maintenance. We believe that gating DPCCH is necessary operation to enhance various data service more efficiently.

## Appendix. Simulation results from Tdoc R1(99)669.

1.2 Simulation results

Table 2. Uplink DPDCH Performance (required Rx. $E_b/N_0$[dB], FER=1%)

| Doppler frequency [Hz] | Gating Rate | | | |
|---|---|---|---|---|
| | 1/1 | 1/2 | 1/4 | 1/8 |
| 5.6 (3km/h) | 2.44 | 3.15 (+0.71) | 4.28 (+1.84) | 6.20 (+3.76) |
| 56 (30km/h) | 3.62 | 4.69 (+1.07) | 5.58 (+1.96) | 6.27 (+2.65) |
| 222 (120km/h) | 4.08 | 4.64 (+0.56) | 5.51 (+1.43) | 5.86 (+1.78) |

* ( ) indicates Eb/No difference compared with 1/1(no gating)

Rx. $E_b = E_{DPDCH} + E_{DPCCH}$ per one antenna

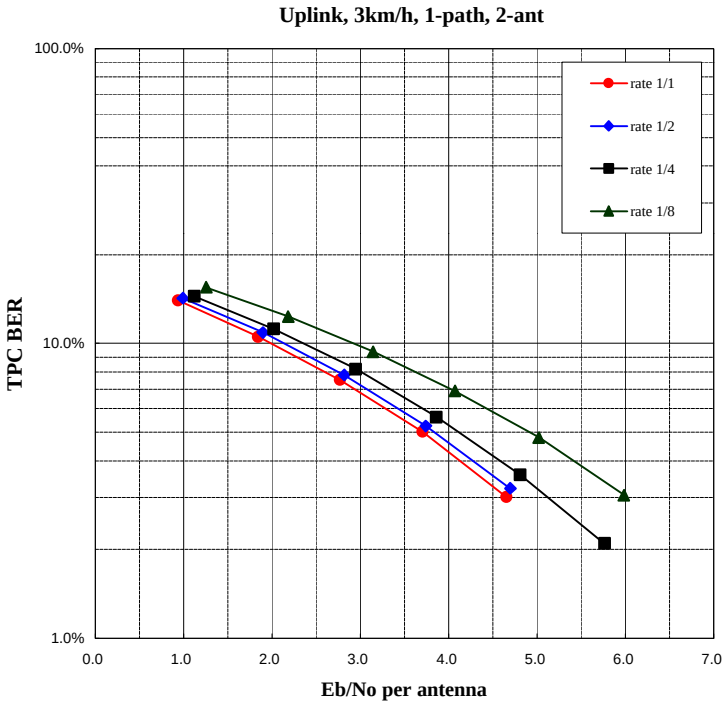


Figure 2. Uplink TPC Performance (3km/h)

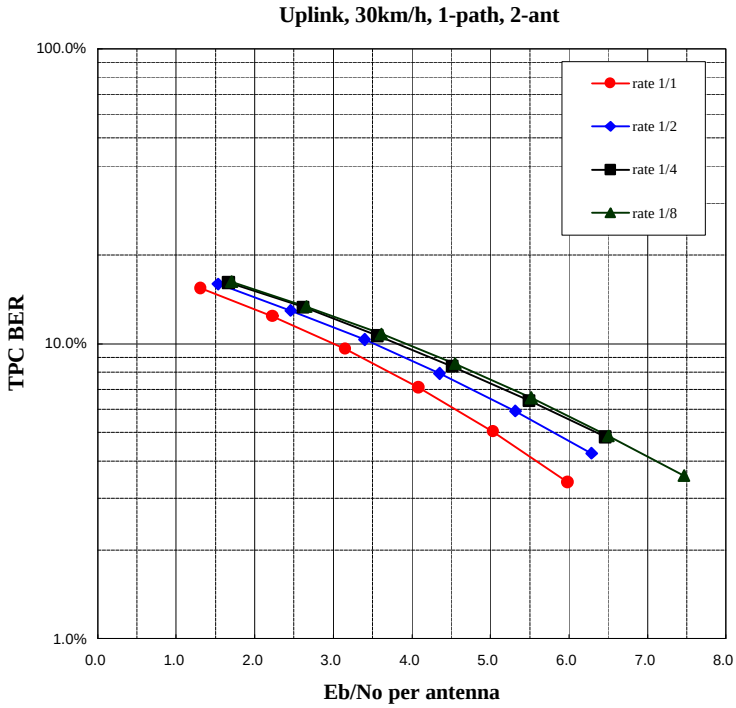


Figure 3. Uplink TPC Performance (30km/h)

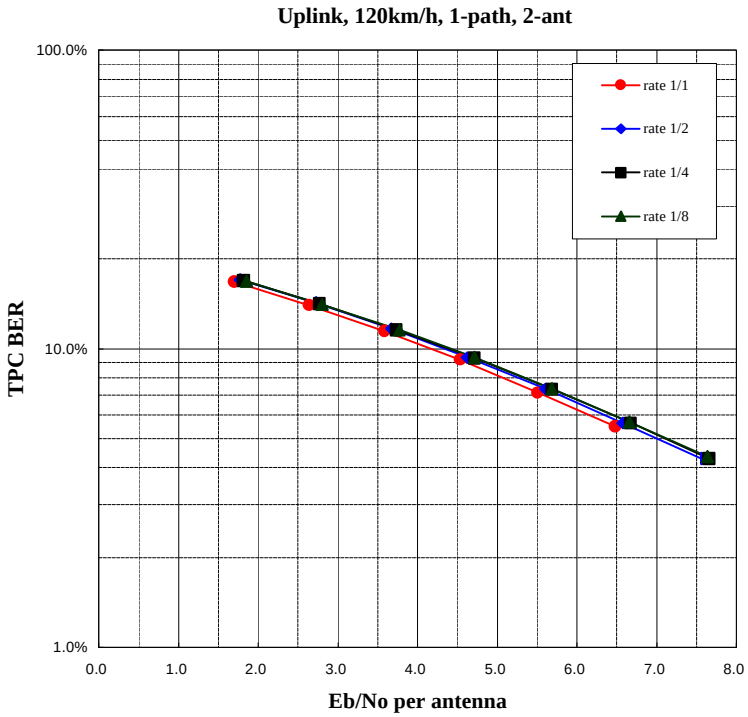


Figure 4. Uplink TPC Performance (120km/h)

## [Reference]

[1] TSGR1#4(99)669, “Performance evaluation of uplink/downlink DPCCH gating”, SAMSUNG.
[2] 3GPP TSGR1#5(99)677, “Impact of OHG harmonization recommendation – UTRA/FDD and UTRA/TDD”
[3] 3GPP TSGR1#5(99)669, “Performance evaluation of uplink/downlink DPCCH gating”
[4] 3GPP TSGR1#5(99)753, “Adhoc-14 report”

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