**[100b-e-NR-5G\_V2X\_NRSL-SYNC-01]**

**Email discussion/approval related to PSBCH contents - indication of TDD configuration**

[100b-e-NR-5G\_V2X\_NRSL-SYNC-01] Email discussion/approval related to PSBCH contents - Indication of TDD configuration

(a,k.a. issue 1-1) by 4/24, with potential TPs by 4/29 (CATT, Teng)

**Issue 1-1 Indication of TDD configuration**

**4/20-4/23**

From the email responses 4/20-4/23, the preference on the TDD indication can be summarized as following table.

* For X and Y, two alternatives are discussed. X and Y indicate pattern and periodicity separately or jointly.
* For Z, now I see many companies think that 8 bits can provide much more flexibility on the indication of UL slots, while 7 bits cannot, especially for FR2 120kHz. Whether Z=7 or 8 bits is also related to the total TDD bits in PSBCH and how X and Y are used.
* Reserve bits, few companies expressed the concerns on taking one bit from the reserve bit is not applicable, since there is only 2 reserve bits in PSBCH.

|  |  |  |  |
| --- | --- | --- | --- |
| **Alternatives** | **Overhead** | **Indication of Slot/symbol-level timing** | **Supporting companies** |
| Alt. 1 | 12 bits | 1bit (Pattern) + 4bits (Periodicity) + 7bits (UL slots) | [Huawei, HiSilicon] [ZTE] [Spreadtrum] [Ericsson] [LGE] [MediaTek] [Intel] [Fujitsu] [DOCOMO] |
| Alt. ~~2~~ 4 | 5bits (Pattern + Periodicity) + 7bits (UL slots) | [OPPO][Qualcomm] |
| Alt. 3 | 4bits (Pattern + Periodicity) + 8bits (UL slots) | [Samsung] |
| Alt. ~~4~~ 2 | 13 bits | 1bit (Pattern) + 4bits (Periodicity) + 8bits (UL slots) | [CMCC][Huawei, HiSilicon] [Spreadtrum] [Apple] [Nokia] |
| Alt. 5 | 5bits (Pattern + Periodicity) + 8bits (UL slots) | [vivo] |

I propose the following alternatives for further discussion and potential down-selection.

* For X and Y, how they can be used for indication is easy to wording in the proposal.
* For Z, a principle wording can be agreed first, and the details can be discussed during the TP stage.

**4/23-4/24**

Based on the three alternatives below, companies had detailed discussion, and the supported solutions are quite different. Besides the following three alternatives, there are still some companies prefer to have other indication combination as shown in above table.

The current situation can be summarized below, and there are 5 combinations that are supported by companies.

* For indication of TDD configuration:
* For X and Y
* Opt 1: X=1 bit, Y=4 bits
* Opt 2: X=0, Y=4 bits
* Opt 3: X=0, Y=5 bits
* For Z
* Opt 1: Z=7 bits
* Opt 2: Z=8 bits

**FL comments:**

* No matter 7 or 8 is used for Z, the granularity loss is high. I did the calculation work, and it is highlighted as follows. The granularity loss is the disadvantages in PSBCH TDD indication due to bit limit (12 bits). Based on my calculation, approximately 13327 states may not be fully indicated. Z=7 bits has a loss of 11663, and Z=8 bits has a loss of 10447. Under this dimension, the difference (11663-10447=1216) between 7 or 8 bits seems like not so large. Anyhow, there is always more than 10000 granularity loss which is inevitable.
* For jointly indication by combination of X and Y, there is forward compatibility when it is 5 bits. When X=0 and Y=4 bits, some periods cannot be fully indicated, i.e. period 4, 5 and 10 ms. By calculation, 68 granularity loss happens. This is because there is no indication on one pattern or two patterns are configured.
* If 1 reserve bit is taken for TDD indication, only 1 reserve bit left. The concern is that it is not good for future function extension. From my perspective, 1 bit or 2 bits of reservation does not have so much difference.
* My previous proposal on Z is FFS the details on how to indicate UL slots. I think jointly indication when two patterns are configured is a proper way, so I add it to the Alt 1 and 2.
* There is also another critical issue mentioned by one company: different interpretation of SL slots between InC UEs and OoC UEs. InC UEs will have the symbol-level resource indication from gNB, while OoC UEs can only get slot-level resource indication from PSBCH. As it was agreed that 7~14 symbols within one slot can be used for SL UE, PSBCH cannot indicate those slots with only partial symbols are UL. There will be a problem when InC UEs communicate with OoC UEs.
* **FL: It is quite difficult for me to determine which Alt can be taken for TDD indication in PSBCH, because each one has pros accompanied with cons that cannot be ignored. From my perspective, I would like to take Alt 1 as a working assumption.**

|  |  |
| --- | --- |
| **Alt 1: 1+4+7** | |
| **Pros** | Following the WA of 12 bits.  For one pattern: Full indication of all periods |
| **Cons** | For 2 patterns: Granularity loss (approx. 11663) |

|  |  |
| --- | --- |
| **Alt 2: 1+4+8** | |
| **Pros** | For one pattern: Full indication of all periods |
| **Cons** | Revert WA of 12 bits.  Consume 1 reserve bit.  For two patterns: Granularity loss (approx. 10447) |

|  |  |
| --- | --- |
| **Alt 3: 0+4+8** | |
| **Pros** | Following the WA of 12 bits. |
| **Cons** | For one pattern: period 4/5/10 ms cannot be fully indicated.  For one patterns: Granularity loss (approx. 68)  For two patterns: Granularity loss (approx. 10447) |

|  |  |
| --- | --- |
| **Alt 4: 0+5+7** | |
| **Pros** | Following the WA of 12 bits.  For one pattern: Full indication of all periods  Forward compatibility of 5 bits |
| **Cons** | For 2 patterns: Granularity loss (approx. 11663) |

|  |  |
| --- | --- |
| **Alt 5: 0+5+8** | |
| **Pros** | For one pattern: Full indication of all periods  Forward compatibility of 5 bits |
| **Cons** | Revert WA of 12 bits.  Consume 1 reserve bit.  For two patterns: Granularity loss (approx. 10447) |

***FL proposals:***

***Alt 1:***

* ***For indication of TDD configuration:***
* ***X=1 bit indicates the number of patterns***
* ***Value 0 indicates one pattern is used.***
* ***Value 1 indicates two patterns are used.***
* ***Y=4 bits indicate the periodicity information***
* ***When one pattern is used, Y indicates the periodicity of the pattern.***
* ***When two patterns are used, Y jointly indicates the periodicities of the two patterns.***
* ***Z=7 bits indicate the UL slots***
* ***UL slots are jointly indicated by 7 bits when two patterns are configured.***
* ***FFS other details.***

***Alt 2:***

* ***For indication of TDD configuration:***
* ***X=1 bit indicates the number of patterns***
* ***Value 0 indicates one pattern is used.***
* ***Value 1 indicates two patterns are used.***
* ***Y=4 bits indicate the periodicity information***
* ***When one pattern is used, Y indicates the periodicity of the pattern.***
* ***When two patterns are used, Y jointly indicates the periodicities of the two patterns.***
* ***Z=8 bits indicate the UL slots***
* ***UL slots are jointly indicated by 8 bits when two patterns are configured.***
* ***FFS detail.***

***Alt. 3:***

* ***For indication of TDD configuration:***
* ***X=0 bit indicates the number of patterns***
* ***Two patterns are used.***
* ***Y=4 bits indicate the periodicity information***
* ***Y indicates the periodicities of the two patterns.***
* ***Z=8 bits indicate the UL slots***
* ***First 4 bits indicates the number of UL slots in the first pattern and second 4 bits indicates the number of UL slots in the second pattern.***

For Alt 3, I add the following table for further explanation on how to use 2 patterns to indicate 1 pattern of the period. Please correct me if my summary is wrong.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Index | 1 Pattern  (msec) | | 2 Pattern  (msec) | Slot configuration period of *pattern1*  (msec) | Slot configuration period of *pattern2*  (msec) |
| 0 | 0.5 | | 1 | 0.5 | 0.5 |
| 1 | 0.625 | | 1.25 | 0.625 | 0.625 |
| 2 | 1 | | 2 | 1 | 1 |
| 3 | 2.5 |  | 2.5 | 0.5 | 2 |
| 4 | 1.25 | 2.5 | 1.25 | 1.25 |
| 5 |  | 2.5 | 2 | 0.5 |
| 6 | 4 |  | 4 | 1 | 3 |
| 7 | 2 | 4 | 2 | 2 |
| 8 |  | 4 | 3 | 1 |
| 9 | 5 | | 5 | 1 | 4 |
| 10 | 5 | 2 | 3 |
| 11 | 5 | 2.5 | 2.5 |
| 12 | 5 | 3 | 2 |
| 13 | 5 | 4 | 1 |
| 14 | 10 | | 10 | 5 | 5 |
| 15 |  | | 20 | 10 | 10 |

**Email responses in 4/23-4/24**

|  |  |
| --- | --- |
| **Company** | **Views** |
| Nokia | (Note: corrected Nokia position above table. Also just noting that we also considered option with Y=3 enabled by preconfiguration but as it is in minority it can be left out from the table).  Our preference would be Alt.2  On compressing the patterns (P, P+P2) to Y=4 bits, we proposed excluding cases where P2>P (And alignment rule that every 20/P or 20/(P+P2) patterns, first symbol of the pattern(s) is a first symbol of an even frame) to make the number of P+P2 cases to be 12.  For compressing the UL slots, like noted earlier, we think that larger granularity is acceptable (e.g. based on SCS and/or pattern). However, it would seem difficult to restrict the number of bits below 8 (4+4) while maintaining sufficient flexibility. Hence we would support increasing the size of the TDD configuration indication with one bit. If 1 reserved bit is not sufficient, we can reduce the size of tehslot index (based on the TDD pattern as the used slot has to be within the SL slots). |
| Huawei, HiSilicon | We think both Alt. 1 and Alt. 2 are agreeable. |
| LGE | Alt. 1 is supported.  Using Z=8 bits sacrifices the reserved bits from 2 bits to 1 bit, which is too small for future extension. Guaranteeing future extension is more beneficial than reducing a few cases of granularity loss. |
| Samsung | Based on I commented in email body, I rephrased my wording as below.  It seems common understanding that 11~13 bits are not clearly enough to indicate full UL slots for one or two patterns for Uu.  We have strong concern on having 1 bit of pattern indication based on our analysis. It does not bring significant benefits, and wasteful bit. This is not optional signaling design, PSBCH content that should be broadcasted everywhere and everytime. So, it should be carefully designed with a certain principle.  In this sense, alt.1 and alt. 2 are not necessary since there is no strong justification why 1 bit of pattern indication is necessary.  We support alt. 3. |
| ZTE, Sanechips | Alte 1 (Z = 7 bits). It is not sensible to reduce 1 bit out of the 2 bits reserved in PSBCH for enhancement in future release.  Our position is that it's of critical importance to ensure the same interpretation of the SL slots for InC and OoC UEs. The current working assumption under structure agenda indicates the SL slot for InC UEs are determined from ***TDD-UL-DL-ConfigCommon.*** Given the PSBCH indication would surely suffer from granularity loss irrespective of any altes taken and we are concerned on the potential slot misalignment issues caused due to the limited slot indication capability in PSBCH. We would like to propose the following under the proposal.  ***note: The UL slot(s) derived by out of coverage UE from PSBCH should be aligned with that derived by in coverage UE from TDD-UL-DL-ConfigCommon.*** |
| Qualcomm | (Note: corrected Qualcomm’s position in the table, our earlier comment was about the details of compressing/subsampling the content)  We still think that joint (X+Y) would be a good solution.  Of the alternatives on the table, we are ok with Alt 1 or Alt 3. We can be ok with Alt 2 depending on where the extra bit comes from. |
| OPPO | We agree with QC that joint (X+Y) indication of pattern/periodicity is OK. In this case X+Y=5. Based on our analysis, up to 25 code-points are enough considering all combinations of pattern and periodicity. Rest 7 code-point can be saved and more suitable for forward compatibility.  We are OK to set Z=8 to indicate UL slot with finer granularity. |
| CMCC | We are Ok with Alt 2 or Alt 3.  As noted earlier, by omitting the state that the full periodicity are all UL slot, more periodicity combinations (11 combinations totally) can be indicated within 8bits without sacrificing slot granularity, and for 10ms+10ms combination, the granularity is reduced from eight-slots to five-slots. So Z=8 bits is more preferred.  As noted by Samsung, we share similar view that 4ms single pattern can be indicated by 1ms+3ms dual pattern case.  Therefore, Alt 2 or Alt 3 are both OK for us. |
| NTT DOCOMO | We support Alt 1. Alt 3 is OK as well. We do not support Alt 4 and Alt 5.  Advantage of Alt. 4/5 is not so much while one reserved bit is sacrificed. Considering future release, two reserved bits are preferable for us. In addition, the main motivation of Alt 4/5 is case of 10+10ms/120kHz for dual patterns.  For smaller SCS, the advantage is very limited. For example, in SCS=30kHz, the issue occurs only in 10+10ms of dual patterns (see R1-2002440 - table 1). Based on RAN4 discussion, FR1 seems to be the typical use case in Rel-16. The reserved bit reduction mainly for FR2 is not preferable in the current situation. Therefore, we suggest that X+Y+Z=12.  Note: also our position is corrected as the above table. We do not support 13 bits, as our contribution mentioned. (What we supported in table below is CMCC’s direction of the discussion. Not total number.) |
| Ericsson | We support Alt.1 |
| Fujitsu | Either Alt1 or Alt2 is agreeable |
| vivo | We support Alt.2 with Z=8 bits but for X and Y, we still prefer to indicate (Pattern + Periodicity) jointly with 5 bits.  Technically there is no significant difference between separate indication (Pattern=1 bits, Periodicity=4 bits) and joint indication(Pattern + Periodicity =5 bits). However, as we explained in the first round input, the joint indication of the number of patterns and periodicity with X+Y=5 bits is beneficial from the perspective of future extension. |

**Email responses 4/20-4/23**

|  |  |
| --- | --- |
| **Company** | **Views** |
| CMCC | **Not fully agree.**   1. ***X=1 bit indicates the number of patterns: Agree*** 2. ***Y=4 bits indicate the periodicity information: Agree*** 3. ***Z=7 bits indicate the UL slots: Not agree***   We think the number of bits of Z is highly related to the indication method, i.e. joint indication (option 1) or independent indication (option 2) of UL slot in two patterns, so it is preferred to be discuss the design details first. It can be observed from the table below that for FR2, ***only the first 6 periodicity combinations (highlighted in grey) can be indicated within Z=7 bits (joint indication) or Z=8 bits (independent indication) using one-120KHz-slot granularity.*** For the rest of the periodicities, the granularity should be larger which sacrifices the indication flexibility, i.e. for 10ms+10ms periodicity, six-slot granularity is used for independent indication with Z=8 bits and eight-slot granularity is used for joint indication with Z=7 bits.  ***We are considering an additional way to reduce the impact, that is, we omit the state that the full periodicity are all UL slot***, which lead to option 1’(joint indication) and option 2’(independent indication) in the following table. For example, when 2ms+2ms is configured, if we do not indicate the case with all 16 slots as UL, the number of states to indicate is only 16, resulting that only 8bits (either joint indication or independent indication) are needed compared with the original option 1/2 where 9bits/10bits are required. In this way, ***more periodicity combinations (11 combinations highlighted in grey) can be indicated within 8bits without sacrificing slot granularity.*** Regarding the resource waste, we consider it acceptable since sacrificing only one slot when the whole periodicity is configured as UL. Therefore, ***it is preferred to use Z=8bits independent indication for finer granularity for more periodicity combination. The number of UL slots is indicated using 120KHz as reference SCS with different granularities for different periodicity combinations as follow:***  *• For 0.5+0.5ms, 0.625+0.625ms, 1+1ms, 0.5+2ms, 2+0.5ms, 1.25+1.25ms, 1+3ms, 3+1ms, 2+2ms, 1+4ms and 4+1ms periodicity combinations,* ***one-slot granularity*** *is used;*  *• For 2+3ms, 3+2ms and 2.5+2.5ms combinations,* ***two-slot granularity*** *is used;*  *• For 5ms+5ms periodicity,* ***three-slot granularity*** *is used;*  *• For 10ms+10ms periodicity,* ***five-slot granularity*** *is used.*  **Table 1 Number of bits needed for indicating number of UL slot using 120Khz as reference SCS**   |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | | Pattern 1 | Pattern 2 | Total number of 120KHz slots N\_1 | Total number of 120KHz slots N\_2 | Option 1:  Number of bits for ***joint indication*** | Option 2:  Number of bits for ***independent indication*** | Option 1‘:  Option 1 with no full UL slot indication | Option 2‘:  Option 2 with no full UL slot indication | | 0.5 | 0.5 | 4 | 4 | 5 | 6 | 4 | 4 | | 0.625 | 0.625 | 5 | 5 | 6 | 6 | 5 | 6 | | 1 | 1 | 8 | 8 | 7 | 8 | 6 | 6 | | 0.5 | 2 | 4 | 16 | 7 | 8 | 6 | 6 | | 2 | 0.5 | 16 | 4 | 7 | 8 | 6 | 6 | | 1.25 | 1.25 | 10 | 10 | 7 | 8 | 7 | 8 | | 1 | 3 | 8 | 24 | 8 | 9 | 8 | 8 | | 3 | 1 | 24 | 8 | 8 | 9 | 8 | 8 | | 2 | 2 | 16 | 16 | 9 | 10 | 8 | 8 | | 1 | 4 | 8 | 32 | 9 | 10 | 8 | 8 | | 4 | 1 | 32 | 8 | 9 | 10 | 8 | 8 | | 2 | 3 | 16 | 24 | 9 | 10 | 9 | 9 | | 3 | 2 | 24 | 16 | 9 | 10 | 9 | 9 | | 2.5 | 2.5 | 20 | 20 | 9 | 10 | 9 | 10 | | 5 | 5 | 40 | 40 | 11 | 12 | 11 | 12 | | 10 | 10 | 80 | 80 | 13 | 14 | 13 | 14 | |
| NTT DOCOMO | Firstly, how to use each part of X/Y/Z should be clarified. Otherwise, the same discussion in the last meeting would be repeated.  We agree with the direction of CMCC’s proposal, i.e. in some cases, UL slots are indicated with granularity of more than one slot. This direction should be discussed and agreed if possible. Then, the granularity level can be discussed with the size of Z.  Similarly, how to X/Y should be clarified. For example, “X = 1 bit with 0 indicates one pattern and 1 indicates two patterns. Y = 4 bits, where one value from {0.5, 0.625, 1, 1.25, 2, 2.5, 4, 5, 10} is indicated with 0000 = 0.5, 0001 = 0.625, etc. for one pattern, …” something like this. |
| Samsung | No support with following reasons.   * It is evident that Z=8 (assuming X=0, default dual pattern) can provide more candidate numbers of UL slots rather than Z=7 (assuming X=1). For Z=7, 80 ( = min(27,80) for single pattern) + 128 ( = 27 for dual pattern) = **208** candidates. For Z=8, 16 ( = 24 for single pattern) + 256 ( = 28 for dual pattern) = **272** candidates. * For Z=7, it is quite difficult to find a single solution since companies supporting (X,Y,Z)=(1,4,7) have different detailed solutions and furthermore Z=7 has an issue of how to determine the number of UL slots per pattern in case of dual pattern as it is odd number. * It is unnecessary to have X=1 as the set of period for single pattern are subset of periods for dual pattern. Instead of indicating patterns, it should be used for other purpose such as indicating UL slots. * We also agree with DCM, CMCC such that just deciding how (X,Y,Z) sizes are should be done with detailed of design since different company have different design principle although they have shown the preference of same size of (X,Y,Z). Also, we agree to have something like the concept of different granularity depending on period since it is evident that all bitmap information cannot indicate entire TDD configuration considering it has limited bitmap size. * Regarding the proposal such as X+Y+Z=13 bits, we have strong concern of reducing reserved bits for PSBCH since reserved bits should be used for future V2X services that have not been identified. That’s why 2 reserved bits should be kept as working assumption.   In this sense, we are supportive of (X,Y,Z) =(0,4,8) with dual pattern as default without reverting working assumption. There is no need to revert working assumption, and it can provide higher flexibility / much information than (1,4,7). |
| Huawei, HiSilicon | We agree CMCC and DOCOMO’s view to first more clearly define the usage of the parameters of X, Y and Z. And considering the number of bits limitation, also we need to agree UL slots are indicated with scaled granularity. Then our proposal as following:  ***Proposal 1: Among the 12 bits for indication of TDD configuration:***   * ***X=1 bit indicates the number of patterns.***   + ***Xv=0: indicates one TDD-UL-DL Pattern 1 is used***   + ***Xv=1: indicates both TDD-UL-DL Pattern 1 and Pattern 2 is used*** * ***Y=4 bits indicate the periodicity information.***   + ***If Xv equals to 0, Y is used to indicate a TDD-UL-DL Pattern 1 periodicity***   + ***If Xv equals to 1, Y is used to jointly indicate both the TDD-UL-DL Pattern 1 and Pattern 2 periodicity*** * ***Z bits indicate the UL slots with scaled granularity***   + ***the Z field can be decided once X and Y are clear*** |
| Nokia | We share the view with other companies that we need to clarify how the bits assigned to X/Y/Z are used to complete the discussion.  We also agree with CMCC and NTT DOCOMO that that we can use higher granularity in higher SCS to indicate the number of SL slots. This may result of course some restriction (mainly numSLslots<=numULslots) depending on the used configuration, but would be acceptable in our view.  We agree with Samsung that the number of reserved bits should not be reduced (from 2) to increase the size of bits used for TDD configuration. However as pointed out in our paper (R1-2001806) we could consider reduce the bits used for slot index, if we account the TDD configuration information reducing the candidate locations for SL slots. |
| vivo | **For X and Y, We prefer to jointly indicate the periodicity and number of patterns, and X+Y=5 bits**.  9 different periodicities are supported for a single pattern case, while up to 16 possibilities are allowed in two patterns case. Thereby 25 combinations of periodicity and number of patterns are supported, and **5 bits are sufficient for joint indication wherein codepoints#25-31 are left unused**.  From the perspective of the indication of the number of patterns and the periodicities, there is no significant difference between using separate indication and joint indication. However, joint indication does have some merits in the perspective of forward compatibility. For example, if some new periodicities are introduced in future releases, such a scheme may only require a few modifications to exploit the unused codepoints for an extension. By contrast, the independent indication scheme needs more bits for extension whenever some of these parameters change.  **For Z, We prefer Z=8.**  We share a similar concern as CMCC and Samsung on Z =7 bits that it can cause a considerable loss in granularity and resource indication, especially when SCS=120kHz. We would like to decide the value of Z first, and then the granularity of Z can be discussed.  Additionally, we think **some extreme cases can also be precluded** to avoid significant compression of resource indication. To be specific, the following cases can be ruled out when two patterns are configured:   * 1. Case1. One or both patterns have no UL slots: 0 slots in P1 and/or 0 slots in P2      1. If there are no UL slots in both patterns, it is impossible to operate NR SL.      2. gNB should configure a single TDD pattern with a UL portion instead of configuring two TDD patterns wherein one of them has no UL   2. Case2. One or both patterns have full UL slots: full UL for P1 and/or full UL for P2      1. This case has already been discussed in the last meeting, it is not reasonable to assume that a whole pattern is UL or the consecutive UL resources across patterns.   By excluding case1 and case2, 1-slot granularity can be used for resource indication in the following cases except for the ones highlighted in yellow.   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Two patterns: P1+P2 | | 120kHz | | Number of combinations(exclude case1 case2) | | P1(ms) | P2(ms) | P1(slot) | P2(slot) | | 0.5 | 0.5 | 4 | 4 | 9 | | 0.625 | 0.625 | 5 | 5 | 16 | | 1 | 1 | 8 | 8 | 49 | | 1.25 | 1.25 | 10 | 10 | 81 | | 2 | 0.5 | 16 | 4 | 45 | | 0.5 | 2 | 4 | 16 | 45 | | 2 | 2 | 16 | 16 | 225 | | 3 | 1 | 24 | 8 | 161 | | 1 | 3 | 8 | 24 | 161 | | 4 | 1 | 32 | 8 | 217 | | 1 | 4 | 8 | 32 | 217 | | 2.5 | 2.5 | 20 | 20 | 361 | | 3 | 2 | 24 | 16 | 345 | | 2 | 3 | 16 | 24 | 345 | | 5 | 5 | 40 | 40 | 1521 | | 10 | 10 | 80 | 80 | 6241 |   For these cases, coarse granularity is needed. For 2.5+2.5, 2+3, or 3+2, either 1-slot granularity or 2-slot granularity is acceptable. However, for 5 ms +5 ms, 10 ms +10 ms, if only one codepoint is used (and therefore 256 combinations are allowed), the indication granularity will be increased to 5 slots which is imprecise for resource indication. **Note that there are some unused codepoints of the indication of pattern number and pattern periodicities. Some of them can be reused together with Z bits for resource indication.**  For example, for P1+P2=10ms+10 ms and SCS=120KHz, the granularity of resource indication can be kept as small as 2-slots if 4 codepoints are exploited for 10ms+10ms. For example, if the indicator of periodicity and the number of patterns =M~M+3, P1+P2=10 ms+10 ms, and both patterns contain SL resources, up to 2^10 combinations can be indicated by PSBCH. We assume that the number of slots available for SL indicated by PSBCH is somehow restricted by the S-SSB number (pre-)configured as the S-SSB should be either concentrated on a set of consecutive UL slots or a set of equally spaced UL slots. Configurations can be envisioned that the consecutive slots available for SL in a pattern is no larger than 64 slots in this case. Thereby 4 codepoints+Z bits are sufficient to cover all combinations for 10+10 ms with 2-slot granularity. Similarly, for 5 ms+5ms, 2 codepoints +Z bits are sufficient to cover all combinations for 5+5 ms with 2-slot granularity if the number of available slots in each pattern is assumed to be no larger than 32 slots. |
| ZTE, Sanechips | We agree to the proposal. Though we echo that the bit width for different fields is substantial, further details including considerations on granularity for UL slot indication need to be captured in the proposal or make up a separate proposal to deliver the whole picture of TDD configuration indication. As analyzed in R1-2001578, Z = 7 bits could indicate the slot numbers within 10ms and the other periodicity values under single pattern. For double patterns, our considerations on this UL slot indication granularity works based on a reference SCS as follows.  Firstly, a reference SCS: ***refSCS*** is derived implicitly through a formula, e.g. ***refSCS*** = min(***SL SCS***, maximal supportable SCS with at most 7 bits) for any given pattern and period combination.  Secondly, the remainder bit(s), if any, are used to indicate the remainder slots measured in SL SCS.  For step 1, our thinking is that the range of {1,2,...,Ns,1} and{0,2,...,Ns,2-1}slots needs to be indicated. The following are the rationale behind:  1. At least 1 downlink/flexible slot should be reserved for SSB transmission and we suppose this case, if configured, places the downlink/flexible slot in the second pattern.  2. 0 UL slot, if configured, always presents in pattern 2. Single pattern could be configured instead otherwise.  3.At least 1 uplink slot should be reserved for sidelink.  The following example together with Fig.1 is put forward to illustrate the above methodology.  Example: Double patterns with periodicity {1ms, 4ms}and SL SCS = 120kHz  The slot combinations to be indicated is 8\*32 =256. The maximal supportable SCS with at most 7 bits is 60kHz with which the combinations to be indicated is 4\*16 = 64.  The remainder bits account for 7-log2(64) = 1 bit  Some remainder slot could be indicated with this bit.    Figure. 1 |
| Spreadtrum | We support that X=1 bit indicates the number of patterns and Y=4 bits indicate the periodicity information.  For the value of Z, we think the indication mechanism for the UL slots in two patterns should be discussed first, i.e., whether scaled granularity is supported in some cases and in which cases it is supported. |
| OPPO | We prefer **joint indication of patterns and periodicities: X+Y = 5 bits**. The following table shows the possible combination of patterns and periodicities.  To indicate the number of UL slot, we propose a default SCS is used to determine the number of UL slots based on TDD-UL-DL-Configuration, for example, 15kHz for FR1, and 60kHz for FR2. In this case, Z= 7 bits can be used for UL slot indication.     |  |  |  |  | | --- | --- | --- | --- | | Index | Slot configuration period  (msec) | Slot configuration period of *pattern1*  (msec) | Slot configuration period of *pattern2*  (msec) | | 0 | 0.5 | 0.5 | 0 | | 1 | 0.625 | 0.625 | 0 | | 2 | 1 | 1 | 0 | | 3 | 1 | 0.5 | 0.5 | | 4 | 1.25 | 1.25 | 0 | | 5 | 1.25 | 0.625 | 0.625 | | 6 | 2 | 2 | 0 | | 7 | 2 | 1 | 1 | | 8 | 2.5 | 1.25 | 1.25 | | 9 | 2.5 | 2.5 | 0 | | 10 | 2.5 | 2 | 0.5 | | 11 | 2.5 | 0.5 | 2 | | 12 | 4 | 4 | 0 | | 13 | 4 | 1 | 3 | | 14 | 4 | 2 | 2 | | 15 | 4 | 3 | 1 | | 16 | 5 | 5 | 0 | | 17 | 5 | 1 | 4 | | 18 | 5 | 2 | 3 | | 19 | 5 | 2.5 | 2.5 | | 20 | 5 | 3 | 2 | | 21 | 5 | 4 | 1 | | 22 | 10 | 10 | 0 | | 23 | 10 | 5 | 5 | | 24 | 20 | 10 | 10 | |
| Ericsson | Agree with the proposal |
| Qualcomm | We agree with the proposal overall. However, as indicated by others, clarification on details of the 3 fields is still needed.  For X and Y, we prefer a joint encoding in 5 bits. For example, the table shown by OPPO.  For Z, we agree that for larger period values, 7 bits may not be sufficient to indicate all the combinations in all cases. The details can be discussed separately. |
| LGE | FL Proposal is supported.  Additionally we need to define the details of each value as follows.  X value;   |  |  | | --- | --- | | *X value* | *Number of patterns* | | *0* | *1* | | *1* | *2* |   Y value for X=0;   |  |  | | --- | --- | | *Y value (in decimal)* | *Periodicity* | | *0* | *0.5* | | *1* | *0.625* | | *2* | *1* | | *3* | *1.25* | | *4* | *2* | | *5* | *2.5* | | *6* | *4* | | *7* | *5* | | *8* | *10* |   Y value for X=1;   |  |  |  | | --- | --- | --- | | *Y value (in decimal)* | *Periodicity of pattern 1* | *Periodicity of pattern 2* | | *0* | *0.5* | *0.5* | | *1* | *0.625* | *0.625* | | *2* | *1* | *1* | | *3* | *0.5* | *2* | | *4* | *2* | *0.5* | | *5* | *1.25* | *1.25* | | *6* | *1* | *3* | | *7* | *3* | *1* | | *8* | *2* | *2* | | *9* | *1* | *4* | | *10* | *4* | *1* | | *11* | *2* | *3* | | *12* | *3* | *2* | | *13* | *2.5* | *2.5* | | *14* | *5* | *5* | | *15* | *10* | *10* |   Z value for given X and Y;   |  |  |  | | --- | --- | --- | | *Z value (in decimal)* | *#UL slots in pattern 1* | *#UL slots in pattern 2* | | *0, …, NP2-1* | *0* | *1,…, NP2* | | *NP2, …, 2\* NP2* | *1* | *0,…, NP2* | | *2\* NP2+1, …, 3\* NP2+1* | *2* | *0,…, NP2* | | *…* | *…* | *…* | | *k\* NP2+k-1, …, (k+1)\* NP2+k-1* | *k* | *0,…, NP2* | | *…* | *…* | *…* | | *NP1\* NP2+ NP1-1, …, ( NP1+1)\* NP2+ NP1-1* | *NP1* | *0,…, NP2* |   where *NP1* and *NP2* are the maximum number of UL slots in pattern 1 and 2 respectively.  Regarding the reference SCS, the default value is the actual SL SCS unless Z cannot represent all the cases of the number of UL slots. If the possible number of UL slots exceeds the Z value range for a combination of SCS and the periodicity for two patterns, the reference SCS can be adjusted as follows. For a single pattern, the actual SL SCS is always used as the reference SCS.   |  |  |  |  | | --- | --- | --- | --- | | *SL SCS* | *Pattern 1 periodicity* | *Pattern 2 periodicity* | *Ref. SCS* | | *120 kHz* | *1* | *3* | *60 kHz* | | *3* | *1* | | *2* | *2* | | *1* | *4* | | *4* | *1* | | *2* | *3* | | *3* | *2* | | *2.5* | *2.5* | | *5* | *5* | *30 kHz* | | *10* | *10* | *15 kHz* | | *60 kHz* | *5* | *5* | *30 kHz* | | *10* | *10* | *15 kHz* | | *30 kHz* | *10* | *10* | *15 kHz* | | *All other cases* | | | *SL SCS* |   The reference SCS is (pre-)configured by a higher layer signaling rather than determined by an implicit rule. The UL slot counted in Z bits includes the slot that contains at least Y-th, (Y+1)-th, ..., (Y+X-1)-th UL symbols, where X and Y are sl-LengthSymbols and sl-StartSymbol respectively. The ‘virtual’ UL slots counted based on the reference SCS should include only the ‘actual’ UL slots based on the SL SCS. That is, if e.g. DL slots are included as part of the virtual UL slot, this virtual UL slot is discarded from UL slot indication in PSBCH. |
| Apple | We agree that X=1 to indicate the number of patterns and Y=4 to indicate periodicity.  We do not support Z=7. Instead, we think Z is 8 bits. Even with 8 bits, we are unable to exactly indicate the number of SL slots for two TDD patterns at high SCS. As mentioned by CMCC and other companies, we can allow higher granularity for the high SCS cases for two TDD patterns. Also, we prefer separate indication of two TDD patterns, and 4 bits are used to indicate the number of SL slots in each TDD pattern. |
| MediaTek | Agree with the proposal with the need of more consideration on the usage of Z bits. For the bits consuming patterns such as {2ms,2ms},{2.5ms,2.5ms},{5ms,5ms}, a reference pattern such as {2ms,2ms} with only total 6 bits (at SCS 60khz) can be used to indicate the UL slots. That is, the signaling based on 6 bits of the reference pattern {2ms,2ms} can be used to derive the UL slots of the other patterns by scaling with a granularity. For example, the signaling indicates 6 UL slots based on the reference pattern {2ms,2ms}, then the UL slots for the actual pattern {5ms,5ms} = 6 / RefPeriod \* ActualPeriod = 6/2\*5=15 UL slots. |
| Intel | We agree with proposal. Looking forward for further proposal on encoding details. |
| Fujitsu | Agree with the proposal. The details of X,Y,Z need to be further discussed as indicated by other companies. | The proposal can be agreed but the details of X,Y,Z need to be further discussed as indicated by other companies. |