# **3GPP TSG RAN Meeting #28 Quebec, Canada, 1 - 3 June 2005**

RP-050202

Title CRs (Rel-5 & Rel-6 CatA) to 25.101 on Clarification to HS-DPCCH time mask

requirements

Source 3GPP TSG RAN WG4 (Radio)

Agenda Item 7.5.5

WG Tdoc	Spec	CR	R	Cat	Rel	Curr Ver	Title	Work Item
R4-050551	25.101	424	1	F	Rel-5	5.14.0	Clarification to HS-DPCCH time mask requirements	TEI5
R4-050552	25.101	425	1	Α	Rel-6	6.7.0	Clarification to HS-DPCCH time mask requirements	TEI5

## Athens, Greece 9 - 13 May 2005

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#### How to create CRs using this form:

Comprehensive information and tips about how to create CRs can be found at <a href="http://www.3gpp.org/specs/CR.htm">http://www.3gpp.org/specs/CR.htm</a>. Below is a brief summary:

1) Fill out the above form. The symbols above marked \( \mathbb{H} \) contain pop-up help information about the field that they are closest to.

- 2) Obtain the latest version for the release of the specification to which the change is proposed. Use the MS Word "revision marks" feature (also known as "track changes") when making the changes. All 3GPP specifications can be downloaded from the 3GPP server under <a href="ftp://ftp.3gpp.org/specs/">ftp://ftp.3gpp.org/specs/</a>. For the latest version, look for the directory name with the latest date e.g. 2001-03 contains the specifications resulting from the March 2001 TSG meetings.
- 3) With "track changes" disabled, paste the entire CR form (use CTRL-A to select it) into the specification just in front of the clause containing the first piece of changed text. Delete those parts of the specification which are not relevant to the change request.

#### 6.5.5 HS-DPCCH

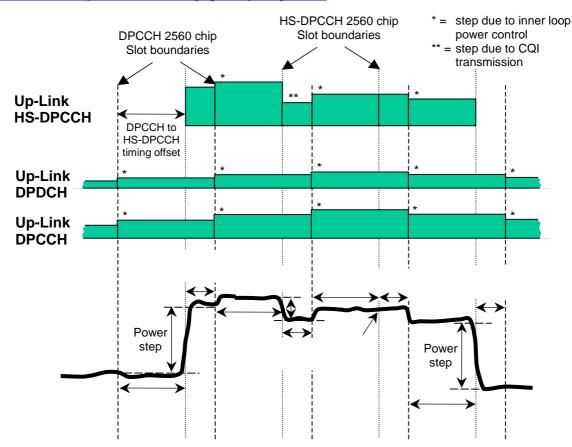
The transmission of Ack/Nack or CQI over HS-DPCCH causes the transmission power in the uplink to vary. The ratio of the amplitude between the DPCCH and the Ack/Nack and CQI respectively is signalled by higher layers.

#### 6.5.5.1 Minimum requirement

The <u>nominal</u> sum power on DPCCH+DPDCH is independent of the transmission of Ack/Nack and CQI unless the UE output power when Ack/Nack or CQI is transmitted would exceed the maximum value specified in Table 6.1A or fall below the value specified in 6.4.3.1, whereupon the UE shall apply additional scaling to the total transmit power as defined in section 5.1.2.6 of TS.25.214 [8].

The composite transmitted power (DPCCH + DPDCH+HS-DPCCH) shall be rounded to the closest integer dB value. When the HS-DPCCH slot timing is aligned with the DPCCH slot timing, the calculation of the power step and any subsequent change in transmitted power occurs once per DPCCH slot at the DPCCH slot boundaries. When the HS-DPCCH slot timing is not aligned with the DPCCH slot timing, this same process occurs twice per DPCCH slot, once at the DPCCH boundary and once at the HS-DPCCH boundary. A power step exactly half-way between two integer values shall be rounded to the closest integer of greater magnitude. The accuracy of the power step, given the step size, is specified in Table 6.9A.

The nominal power step due to transmission of Ack/Nack or CQI is defined as the difference between the nominal mean powers of any two adjacent power evaluation periods either side of an HS-DPCCH boundary. The first evaluation period starts 25µs after a DPCCH slot boundary and ends 25µs before the following HS-DPCCH slot boundary. The second evaluation period starts 25µs after the same HS-DPCCH slot boundary and ends 25µs before the following DPCCH slot boundary. This is described graphically in figure 6.6.



The power step due to HS-DPCCH transmission is the difference between the mean powers transmitted before and after an HS-DPCCH slot boundary. The mean power evaluation period excludes a 25µs period before and after any DPCCH or HS-DPCCH slot boundary.

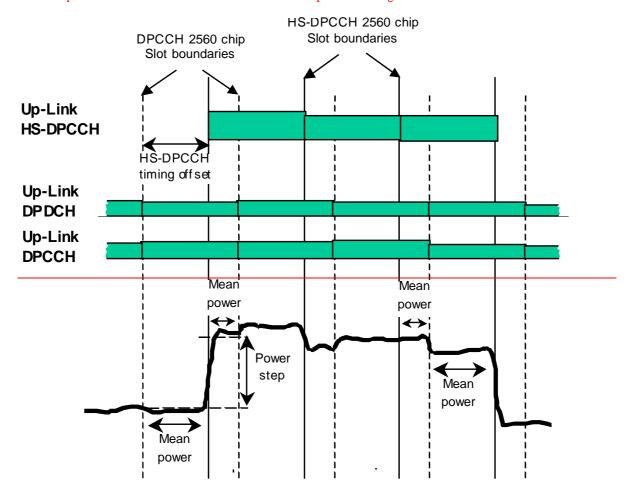
The tolerance of the power step due to transmission of the HS-DPCCH shall meet the requirements in table 6.9A.

In the simple case where the HS DPCCH slots are aligned with the DPCCH slots, each power evaluation period shall be one DPCCH timeslot in length. In the case where the HS DPCCH timeslots are not aligned with the DPCCH timeslots, the power evaluation periods are shorter and start with a DPCCH slot boundary ending with the next HS DPCCH slot boundary or start with an HS-DPCCH slot boundary and end with the next DPCCH slot boundary. In this non-aligned case, the length of any two adjacent power evaluation periods equals 2560 chips. In all cases the evaluation of mean power shall exclude a 25µs period before and after any DPCCH or HS DPCCH slot boundary.

Table 6.9A: Transmitter power step tolerance

Nominal power step size (Up or down) ΔP [dB]	Transmitter power step tolerance [dB]
0	+/- 0.5
1	+/- 0.5
2	+/- 1.0
3	+/- 1.5
4 ≤ Δ P ≤ 7	+/- 2.0

The transmit power levels versus time shall meet the mask specified in Figure 6.6.



The mean power is evaluated excluding a 25µs transient period either side of any DPCCH or HS-DPCCH slot boundary

Figure 6.6: Transmit power template during HS-DPCCH transmission

### Athens, Greece 9 - 13 May 2005

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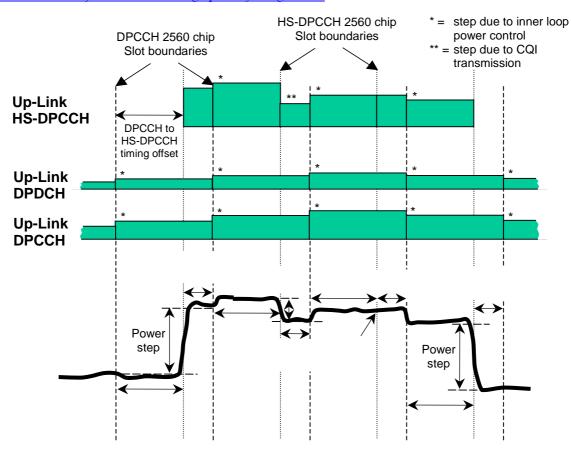
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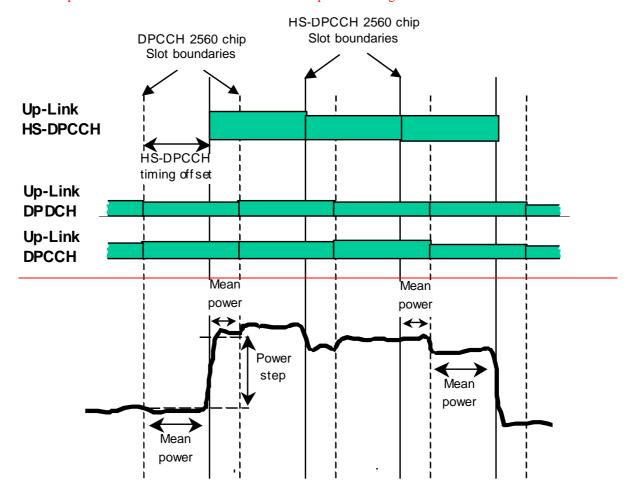
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