TSG RAN Meeting #27 **RP-050090**
Tokyo, Japan, 9 - 11 March 2005

Title **CR (Rel-6 Category F) to TS25.211 for E-HICH/E-RGCH/E-AGCH timing**
Source **TSG RAN WG1**
Agenda Item **9.6**

RAN1 Tdoc	Spec	CR	Rev	Rel	Cat	Current Version	Subject	Work item	Remarks
R1-050223	25.211	202	2	Rel-6	F	6.3.0	E-HICH/E-RGCH/E-AGCH timing	EDCH-Phys	

3GPP TSG-RAN WG1 Meeting #40
Scottsdale, AZ, USA, 14–18 February 2005

Tdoc ⌘ R1-050223

CR-Form-v7.1

CHANGE REQUEST

⌘ **25.211** **CR** **202** ⌘ **rev** **2** ⌘ Current version: **6.3.0** ⌘

*For **HELP** on using this form, see bottom of this page or look at the pop-up text over the ⌘ symbols.*

Proposed change affects: UICC apps⌘ [ ] ME [X] Radio Access Network [X] Core Network [ ]

Title:	⌘	E-HICH/E-RGCH/E-AGCH timing
Source:	⌘	RAN WG1
Work item code:	⌘	EDCH-Phys
Date:	⌘	2/18/2005
Category:	⌘	**F**
Release:	⌘	Rel-6

Use one of the following categories:
F *(correction)*
A *(corresponds to a correction in an earlier release)*
B *(addition of feature),*
C *(functional modification of feature)*
D *(editorial modification)*
Detailed explanations of the above categories can be found in 3GPP TR 21.900.

Use one of the following releases:
Ph2 (GSM Phase 2)
R96 (Release 1996)
R97 (Release 1997)
R98 (Release 1998)
R99 (Release 1999)
Rel-4 (Release 4)
Rel-5 (Release 5)
Rel-6 (Release 6)
Rel-7 (Release 7)

Reason for change:	⌘	E-HICH/E-RGCH/E-AGCH timing is unspecified
Summary of change:	⌘	• Adding missing specification text • Introducing 12 slots E-HICH and E-RGCH duration
Consequences if not approved:	⌘	Can not operate E-DCH

Clauses affected:	⌘	7

Other specs affected: ⌘	Y	N	
		X	Other core specifications
		X	Test specifications
			O&M Specifications

⌘

Other comments: ⌘

How to create CRs using this form:
Comprehensive information and tips about how to create CRs can be found at http://www.3gpp.org/specs/CR.htm.
Below is a brief summary:

1) Fill out the above form. The symbols above marked ⌘ contain pop-up help information about the field that they are closest to.
2) Obtain the latest version for the release of the specification to which the change is proposed. Use the MS Word "revision marks" feature (also known as "track changes") when making the changes. All 3GPP specifications can be downloaded from the 3GPP server under ftp://ftp.3gpp.org/specs/ For the latest version, look for the directory name with the latest date e.g. 2001-03 contains the specifications resulting from the March 2001 TSG meetings.

3) With "track changes" disabled, paste the entire CR form (use CTRL-A to select it) into the specification just in front of the clause containing the first piece of changed text. Delete those parts of the specification which are not relevant to the change request.

5.3.2.4 E-DCH Relative Grant Channel

The E-DCH Relative Grant Channel (E-RGCH) is a fixed rate (SF=128) dedicated downlink physical channel carrying the uplink E-DCH relative grants. Figure 12A illustrates the structure of the E-RGCH. A relative grant is transmitted using 3, 12 or 15 consecutive slots and in each slot a sequence of 40 ternary values is transmitted. The 3 and 12 slot duration shall be used to control UEs for which the cell is the E-DCH serving cell and which E-DCH TTI is respectively 2 and 10 ms. The 15 slot duration shall be used to control UEs for which the cell is not the E-DCH serving cell.

The sequence $b_{i,0}$, $b_{i,1}$, …, $b_{i,39}$ transmitted in slot i in Figure 12A is given by $b_{i,j} = a\ C_{ss,40,l,j}$. In a serving E-DCH radio link set, the relative grant a is set to +1, 0, or -1 and in a non-serving E-DCH radio link set, the relative grant a is set to 0 or -1. The orthogonal signature sequences $C_{ss,40,l}$ is given by Table 16A and the E-RGCH signature sequence index l is given by higher layers.

In case STTD-based open loop transmit diversity is applied for E-RGCH, STTD encoding according to subclause 5.3.1.1.1 is applied to the sequence $b_{i,j}$.

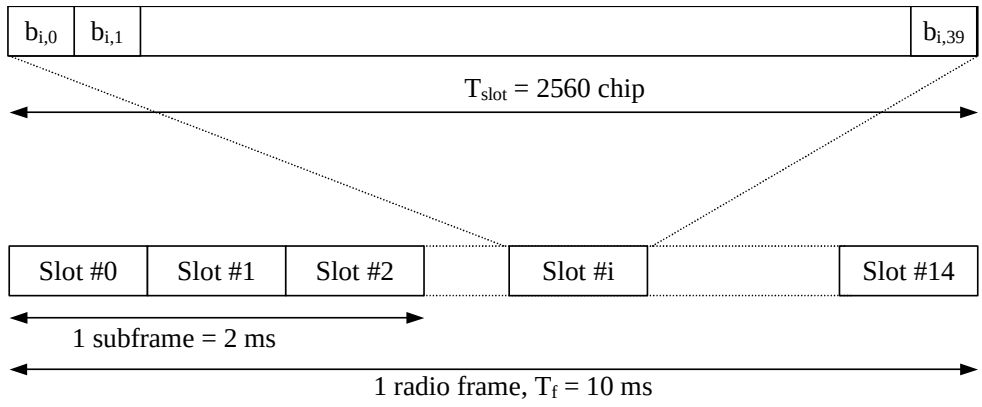

Figure 12A: E-RGCH and E-HICH structure

Table 16A: E-RGCH and E-HICH signature sequences

$C_{ss,40,0}$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$C_{ss,40,1}$	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1
$C_{ss,40,2}$	1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1
$C_{ss,40,3}$	1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1
$C_{ss,40,4}$	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1
$C_{ss,40,5}$	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1
$C_{ss,40,6}$	1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1
$C_{ss,40,7}$	1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	1	-1	-1	1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1
$C_{ss,40,8}$	1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1
$C_{ss,40,9}$	1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1
$C_{ss,40,10}$	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1
$C_{ss,40,11}$	1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1
$C_{ss,40,12}$	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1
$C_{ss,40,13}$	1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1
$C_{ss,40,14}$	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1
$C_{ss,40,15}$	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1
$C_{ss,40,16}$	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1
$C_{ss,40,17}$	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1
$C_{ss,40,18}$	1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1
$C_{ss,40,19}$	1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1
$C_{ss,40,20}$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1
$C_{ss,40,21}$	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	1	-1
$C_{ss,40,22}$	1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	-1	-1	1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	1	-1	1
$C_{ss,40,23}$	1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	-1	-1	-1	1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	1	-1	1	1
$C_{ss,40,24}$	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	-1	-1	1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	1	-1	1	1	-1
$C_{ss,40,25}$	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	1	-1	1	1	-1	-1
$C_{ss,40,26}$	1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	1	-1	1	1	-1	-1	1
$C_{ss,40,27}$	1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	1	-1	1	1	-1	-1	1	1
$C_{ss,40,28}$	1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	-1	-1	-1	-1	1	1	-1	1	1	-1	-1	1	1	1
$C_{ss,40,29}$	1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	-1	1	-1	1	-1	-1	-1	-1	1	1	-1	1	1	-1	-1	1	1	1	1	1
$C_{ss,40,30}$	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	-1	-1	-1	-1	1	1	-1	1	1	-1	-1	1	1	1	1	-1
$C_{ss,40,31}$	1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	-1	-1	1	-1	-1	-1	-1	1	1	-1	1	1	-1	-1	1	1	1	1	-1	1
$C_{ss,40,32}$	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	-1	-1	-1	-1	1	1	-1	1	1	-1	-1	1	1	1	1	-1	1	-1
$C_{ss,40,33}$	1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	-1	-1	-1	-1	1	1	-1	1	1	-1	-1	1	1	1	1	-1	1	-1	1	1
$C_{ss,40,34}$	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	-1	-1	-1	-1	1	1	-1	1	1	-1	-1	1	1	1	1	-1	1	-1	1	-1
$C_{ss,40,35}$	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	-1	-1	-1	1	1	-1	1	1	-1	-1	1	1	1	1	-1	1	-1	1	-1	-1
$C_{ss,40,36}$	1	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	-1	-1	1	1	-1	1	1	-1	-1	1	1	1	1	-1	1	-1	1	-1	-1	-1
$C_{ss,40,37}$	1	-1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	1	1	-1	1	1	-1	-1	1	1	1	1	-1	1	-1	1	-1	-1	-1	-1
$C_{ss,40,38}$	1	-1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1
$C_{ss,40,39}$	1	1	-1	-1	1	1	-1	-1	-1	-1	1	-1	1	-1	1	1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	1

The bits are transmitted in order from left to right, i.e., column 2 corresponds to index j=0 and the rightmost column corresponds to index j=39.

5.3.2.4 E-DCH Hybrid ARQ Indicator Channel

The E-DCH Hybrid ARQ Indicator Channel (E-HICH) is a fixed rate (SF=128) dedicated downlink physical channel carrying the uplink E-DCH hybrid ARQ acknowledgement indicator. Figure 12A illustrates the structure of the E-HICH. A hybrid ARQ acknowledgement indicator is transmitted using 3 or ~~15~~ 12 consecutive slots and in each slot a sequence of 40 binary values is transmitted. The 3 and 12 slot duration shall be used for UEs which E-DCH TTI is set to respectively 2 ms and 10 ms.

The sequence $b_{i,0}$, $b_{i,1}$, …, $b_{i,39}$ transmitted in slot i in Figure 12A is given by $b_{i,j} = a\ C_{ss,40,l,j}$. In a radio link set containing the serving E-DCH radio link set, the hybrid ARQ acknowledgement indicator a is set to +1 or –1, and in a radio link set not containing the serving E-DCH radio link set the hybrid ARQ indicator a is set to +1 or 0. The orthogonal signature sequences $C_{ss,40,l}$ is given by Table 16A and the E-HICH signature sequence index l is given by higher layers.

In case STTD-based open loop transmit diversity is applied for E-HICH, STTD encoding according to subclause 5.3.1.1.1 is applied to the sequence $b_{i,j}$

<<<<<<<<<<<<<<<<<<<<<<<<<<<< **Next Modified Section** >>>>>>>>>>>>>>>>>>>>>>>>>>

7 Timing relationship between physical channels

7.1 General

The P-CCPCH, on which the cell SFN is transmitted, is used as timing reference for all the physical channels, directly for downlink and indirectly for uplink.

Figure 29 below describes the frame timing of the downlink physical channels. For the AICH the access slot timing is included. Transmission timing for uplink physical channels is given by the received timing of downlink physical channels, as described in the following subclauses.

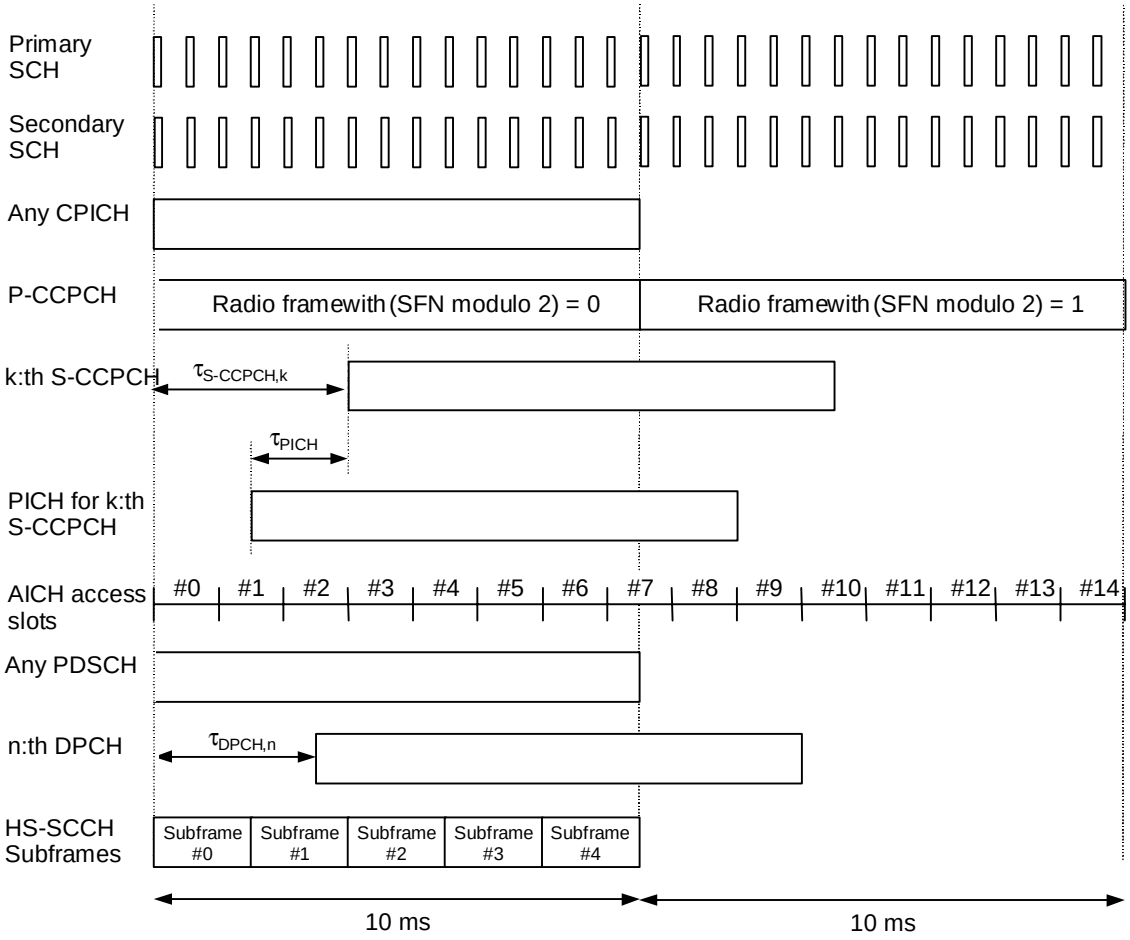

Figure 29: Radio frame timing and access slot timing of downlink physical channels

The following applies:

- SCH (primary and secondary), CPICH (primary and secondary), P-CCPCH, and PDSCH have identical frame timings.
- The S-CCPCH timing may be different for different S-CCPCHs, but the offset from the P-CCPCH frame timing is a multiple of 256 chips, i.e. $\tau_{S\text{-}CCPCH,k} = T_k \times 256$ chip, $T_k \in \{0, 1, \ldots, 149\}$.
- The PICH timing is $\tau_{PICH} = 7680$ chips prior to its corresponding S-CCPCH frame timing, i.e. the timing of the S-CCPCH carrying the PCH transport channel with the corresponding paging information, see also subclause 7.2.

- AICH access slots #0 starts the same time as P-CCPCH frames with (SFN modulo 2) = 0. The AICH/PRACH and AICH/PCPCH timing is described in subclauses 7.3 and 7.4 respectively.
- The relative timing of associated PDSCH and DPCH is described in subclause 7.5.
- The DPCH timing may be different for different DPCHs, but the offset from the P-CCPCH frame timing is a multiple of 256 chips, i.e. $\tau_{DPCH,n} = T_n \times 256$ chip, $T_n \in \{0, 1, \ldots, 149\}$. The DPCH (DPCCH/DPDCH) timing relation with uplink DPCCH/DPDCHs is described in subclause 7.6.
- The start of HS-SCCH subframe #0 is aligned with the start of the P-CCPCH frames. The relative timing between a HS-PDSCH and the corresponding HS-SCCH is described in subclause 7.8.
- The E-DPCCH and all E-DPDCHs transmitted from one UE have the same frame timing as the DPCCH.

7.2 PICH/S-CCPCH timing relation

Figure 30 illustrates the timing between a PICH frame and its associated single S-CCPCH frame, i.e. the S-CCPCH frame that carries the paging information related to the paging indicators in the PICH frame. A paging indicator set in a PICH frame means that the paging message is transmitted on the PCH in the S-CCPCH frame starting τ_{PICH} chips after the transmitted PICH frame. τ_{PICH} is defined in subclause 7.1.

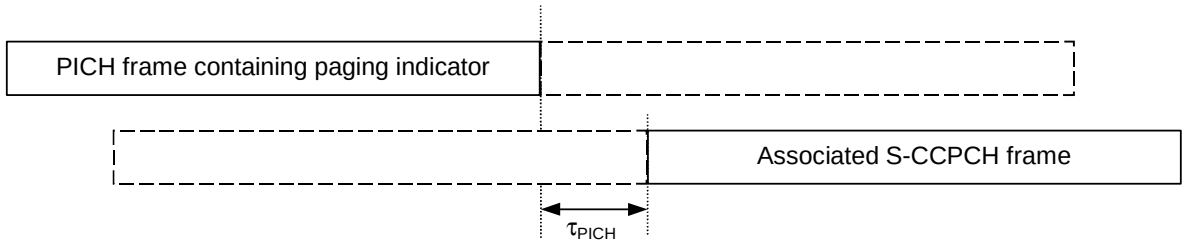

Figure 30: Timing relation between PICH frame and associated S-CCPCH frame

7.3 PRACH/AICH timing relation

The downlink AICH is divided into downlink access slots, each access slot is of length 5120 chips. The downlink access slots are time aligned with the P-CCPCH as described in subclause 7.1.

The uplink PRACH is divided into uplink access slots, each access slot is of length 5120 chips. Uplink access slot number *n* is transmitted from the UE $\tau_{p\text{-}a}$ chips prior to the reception of downlink access slot number *n*, *n* = 0, 1, …, 14.

Transmission of downlink acquisition indicators may only start at the beginning of a downlink access slot. Similarly, transmission of uplink RACH preambles and RACH message parts may only start at the beginning of an uplink access slot.

The PRACH/AICH timing relation is shown in figure 31.

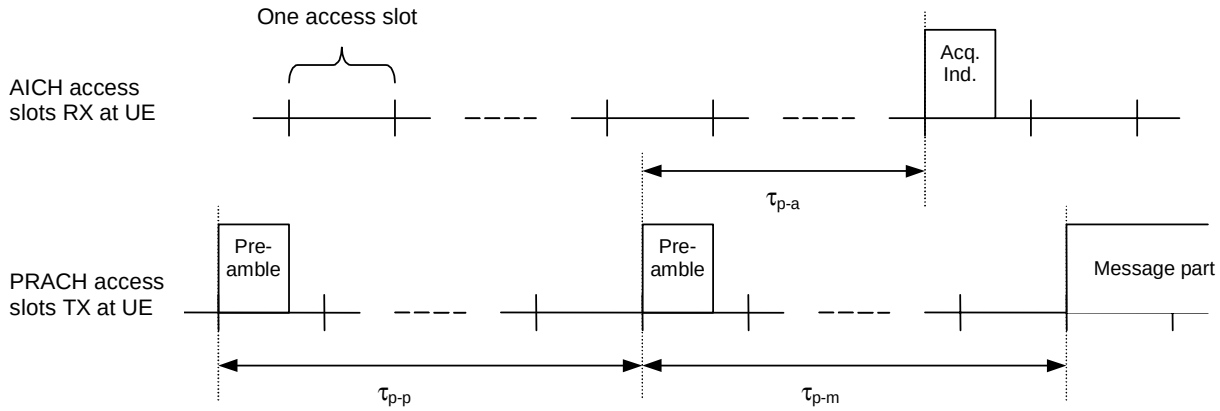

Figure 31: Timing relation between PRACH and AICH as seen at the UE

The preamble-to-preamble distance $\tau_{p\text{-}p}$ shall be larger than or equal to the minimum preamble-to-preamble distance $\tau_{p\text{-}p,min}$, i.e. $\tau_{p\text{-}p} \geq \tau_{p\text{-}p,min}$.

In addition to $\tau_{p\text{-}p,min}$, the preamble-to-AI distance $\tau_{p\text{-}a}$ and preamble-to-message distance $\tau_{p\text{-}m}$ are defined as follows:

- when AICH_Transmission_Timing is set to 0, then

  $\tau_{p\text{-}p,min}$ = 15360 chips (3 access slots)

  $\tau_{p\text{-}a}$ = 7680 chips

  $\tau_{p\text{-}m}$ = 15360 chips (3 access slots)

- when AICH_Transmission_Timing is set to 1, then

  $\tau_{p\text{-}p,min}$ = 20480 chips (4 access slots)

  $\tau_{p\text{-}a}$ = 12800 chips

  $\tau_{p\text{-}m}$ = 20480 chips (4 access slots)

The parameter AICH_Transmission_Timing is signalled by higher layers.

7.4 PCPCH/AICH timing relation

The uplink PCPCH is divided into uplink access slots, each access slot is of length 5120 chips. Uplink access slot number n is transmitted from the UE $\tau_{p\text{-}a1}$ chips prior to the reception of downlink access slot number n, n =0, 1, …,14.

The timing relationship between preambles, AICH, and the message is the same as PRACH/AICH. Note that the collision resolution preambles follow the access preambles in PCPCH/AICH. However, the timing relationships between CD-Preamble and CD/CA-ICH is identical to RACH Preamble and AICH. The timing relationship between CD/CA-ICH and the Power Control Preamble in CPCH is identical to AICH to message in RACH. The T_{cpch} timing parameter is identical to the PRACH/AICH transmission timing parameter. When T_{cpch} is set to zero or one, the following PCPCH/AICH timing values apply.

Note that a1 corresponds to AP-AICH and a2 corresponds to CD/CA-ICH.

$\tau_{p\text{-}p}$ = Time to next available access slot, between Access Preambles.

Minimum time = 15360 chips + 5120 chips X Tcpch

Maximum time = 5120 chips X 12 = 61440 chips

Actual time is time to next slot (which meets minimum time criterion) in allocated access slot subchannel group.

$\tau_{p\text{-}a1}$ = Time between Access Preamble and AP-AICH has two alternative values: 7680 chips or 12800 chips, depending on T_{cpch}

$\tau_{a1\text{-}cdp}$ = Time between receipt of AP-AICH and transmission of the CD Preamble $\tau_{a1\text{-}cdp}$ has a minimum value of $\tau_{a1\text{-}cdp,\ min}$ =7680 chips.

$\tau_{p\text{-}cdp}$ = Time between the last AP and CD Preamble. $\tau_{p\text{-}cdp}$ has a minimum value of $\tau_{p\text{-}cdp\text{-}min}$ which is either 3 or 4 access slots, depending on T_{cpch}

$\tau_{cdp\text{-}a2}$ = Time between the CD Preamble and the CD/CA-ICH has two alternative values: 7680 chips or 12800 chips, depending on T_{cpch}

$\tau_{cdp\text{-}pcp}$ = Time between CD Preamble and the start of the Power Control Preamble is either 3 or 4 access slots, depending on $T_{cpch.}$

The time between the start of the reception of DL-DPCCH slot at UE and the Power Control Preamble is T_0 chips, where T_0 is as in subclause 7.6.3.

The message transmission shall start 0 or 8 slots after the start of the power control preamble depending on the length of the power control preamble.

Figure 32 illustrates the PCPCH/AICH timing relationship whenT_{cpch} is set to 0 and all access slot subchannels are available for PCPCH.

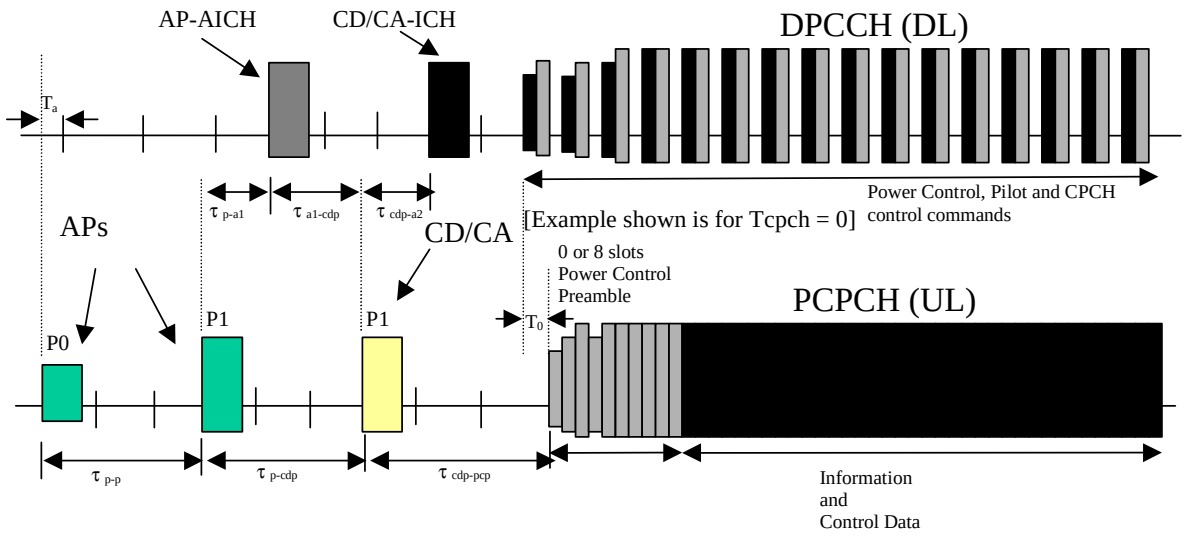

Figure 32: Timing of PCPCH and AICH transmission as seen by the UE, with T_{cpch}= 0

7.5 DPCH/PDSCH timing

The relative timing between a DPCH frame and the associated PDSCH frame is shown in figure 33.

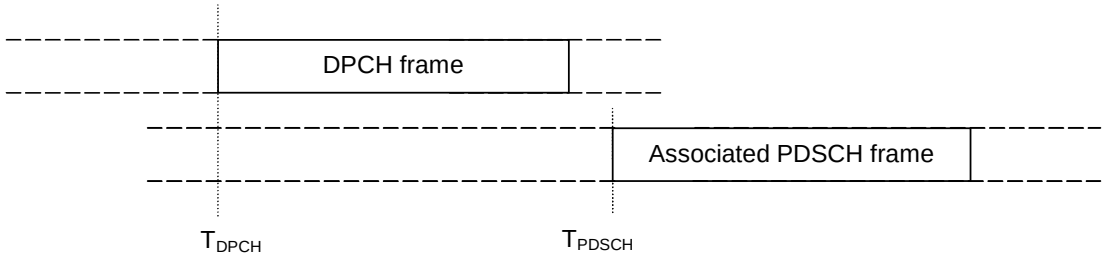

Figure 33: Timing relation between DPCH frame and associated PDSCH frame

The start of a DPCH frame is denoted T_{DPCH} and the start of the associated PDSCH frame is denoted T_{PDSCH}. Any DPCH frame is associated to one PDSCH frame through the relation 46080 chips ≤ T_{PDSCH} - T_{DPCH} < 84480 chips, i.e., the associated PDSCH frame starts between three slots after the end of the DPCH frame and 18 slots after the end of the DPCH frame, as described in subclause 7.1.

7.6 DPCCH/DPDCH timing relations

7.6.1 Uplink

In uplink the DPCCH and all the DPDCHs transmitted from one UE have the same frame timing.

7.6.2 Downlink

In downlink, the DPCCH and all the DPDCHs carrying CCTrCHs of dedicated type to one UE have the same frame timing.

Note: support of multiple CCTrChs of dedicated type is not part of the current release.

7.6.3 Uplink/downlink timing at UE

At the UE, the uplink DPCCH/DPDCH frame transmission takes place approximately T_0 chips after the reception of the first detected path (in time) of the corresponding downlink DPCCH/DPDCH frame. T_0 is a constant defined to be 1024 chips. The first detected path (in time) is defined implicitly by the relevant tests in [14]. More information about the uplink/downlink timing relation and meaning of T_0 can be found in [5].

7.7 Uplink DPCCH/HS-DPCCH/HS-PDSCH timing at the UE

Figure 34 shows the timing offset between the uplink DPCH, the HS-PDSCH and the HS-DPCCH at the UE. An HS-DPCCH sub-frame starts $m \times 256$ chips after the start of an uplink DPCH frame that corresponds to the DL DPCH frame from the HS-DSCH serving cell containing the beginning of the related HS-PDSCH subframe with *m* calculated as

$m = (T_{TX\_diff} /256) + 101$

where T_{TX_diff} is the difference in chips (T_{TX_diff} =0, 256, ..., 38144), between

- the transmit timing of the start of the related HS-PDSCH subframe (see sub-clauses 7.8 and 7.1)

and

- the transmit timing of the start of the downlink DPCH frame from the HS-DSCH serving cell that contains the beginning of the HS-PDSCH subframe (see sub-clause 7.1).

At any one time, *m* therefore takes one of a set of five possible values according to the transmission timing of HS-DSCH sub-frame timings relative to the DPCH frame boundary. The UE and Node B shall only update the set of values of *m* in connection to UTRAN reconfiguration of downlink timing.

More information about uplink timing adjustments can be found in [5].

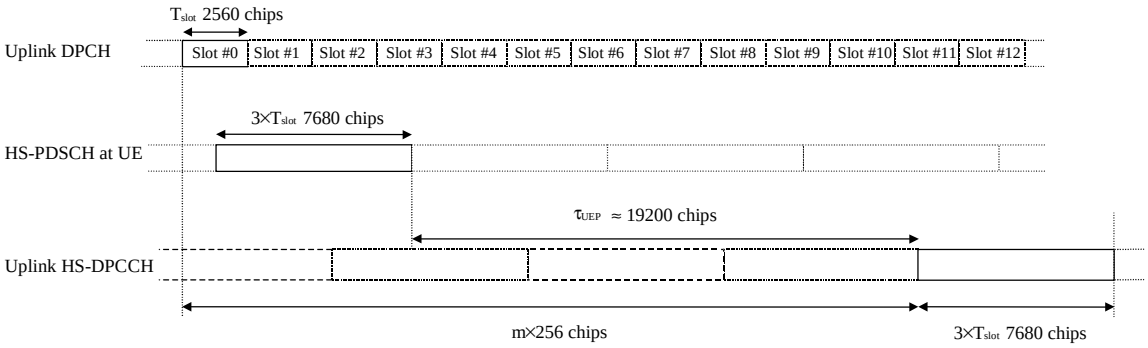

Figure 34: Timing structure at the UE for HS-DPCCH control signalling

7.8 HS-SCCH/HS-PDSCH timing

Figure 35 shows the relative timing between the HS-SCCH and the associated HS-PDSCH for one HS-DSCH sub-frame. The HS-PDSCH starts $\tau_{HS\text{-}PDSCH} = 2 \times T_{slot} = 5120$ chips after the start of the HS-SCCH.

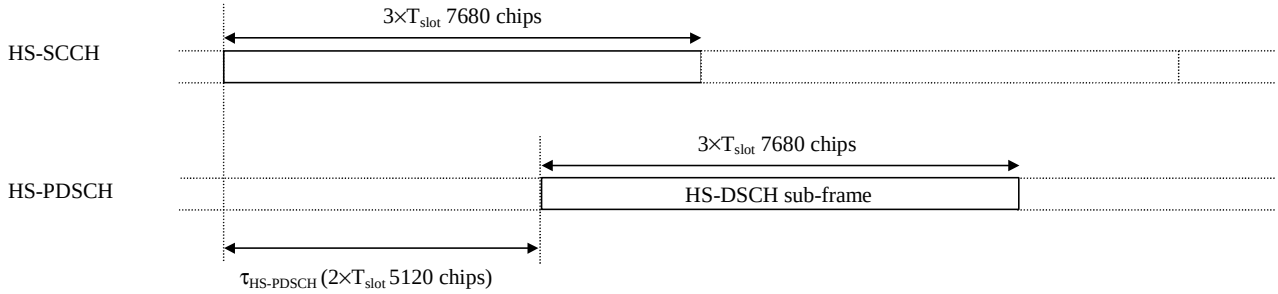

Figure 35: Timing relation between the HS-SCCH and the associated HS-PDSCH.

7.9 MICH/S-CCPCH timing relation

Figure 36 illustrates the timing between the MICH frame boundaries and the frame boundaries of the associated S-CCPCH, i.e. the S-CCPCH that carries the MBMS control information related to the notification indicators in the MICH frame. The MICH transmission timing shall be such that the end of radio frame boundary occurs τ_{MICH} chips before the associated S-CCPCH start of radio frame boundary. τ_{MICH} is equal to 7680 chips.

The MICH frames during which the Node B shall set specific notification indicators and the S-CCPCH frames during which the Node B shall transmit the corresponding MBMS control data is defined by higher layers.

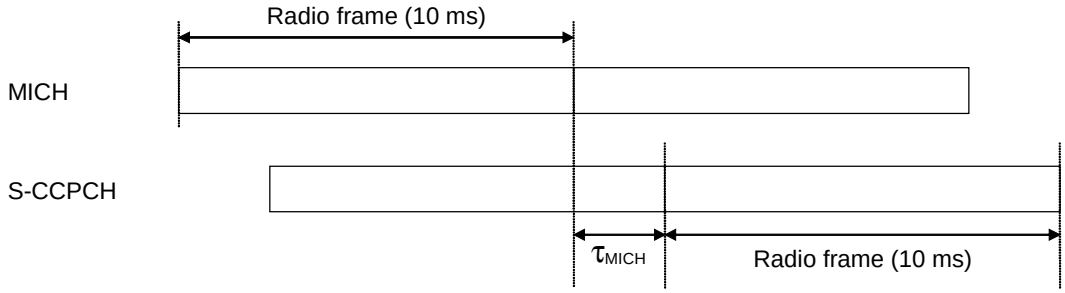

Figure 36: Timing relation between MICH frame and associated S-CCPCH frame

7.10 DL E-HICH/P-CCPCH/DPCH timing relation

The timing of the DL E-HICH relative to the P-CCPCH is illustrated in figure 37.

When the E-DCH TTI is 10 ms the E-HICH frame offset relative to P-CCPCH shall be $\tau_{E\text{-}HICH,n}$ chips with

$$\tau_{E-HICH,n} = 5120 + 7680 \times \left\lfloor \frac{(\tau_{DPCH,n}/256) - 70}{30} \right\rfloor$$

When the E-DCH TTI is 2 ms the E-HICH frame offset relative to P-CCPCH shall be $\tau_{E\text{-}HICH,n}$ chips with

$$\tau_{E-HICH,n} = 5120 + 7680 \times \left\lfloor \frac{(\tau_{DPCH,n}/256) + 50}{30} \right\rfloor$$

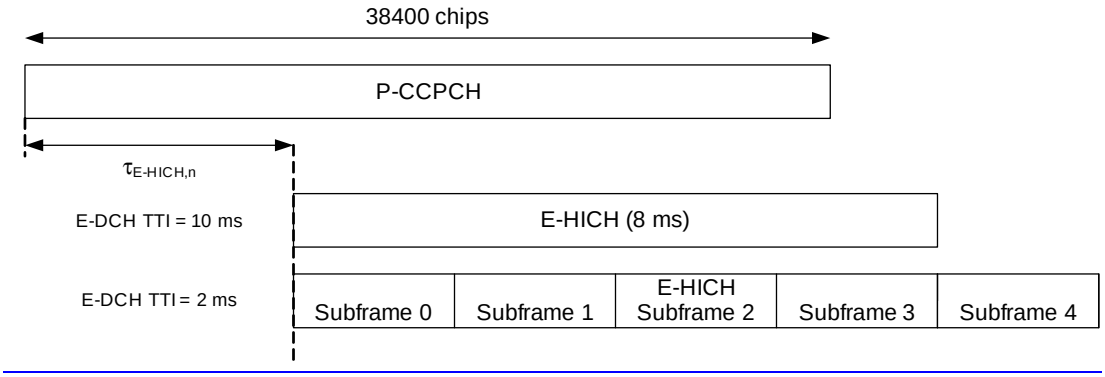

Figure 37: E-HICH timing

7.11 DL E-RGCH/P-CCPCH/DPCH timing relation

The timing of the DL E-RGCH relative to the P-CCPCH is illustrated in figure 38.

When transmitted to a UE for which the cell is the E-DCH serving cell the E-RGCH frame offset shall be as follows:

- if the E-DCH TTI is 10 ms, the E-RGCH frame offset relative to P-CCPCH shall be $\tau_{E\text{-}RGCH,n}$ chips with

$$\tau_{E-RGCH,n} = 5120 + 7680 \times \left\lfloor \frac{(\tau_{DPCH,n}/256) - 70}{30} \right\rfloor$$

- if the E-DCH TTI is 2 ms the E-RGCH frame offset relative to P-CCPCH shall be $\tau_{E\text{-}RGCH,n}$ chips with

$$\tau_{E-RGCH,n} = 5120 + 7680 \times \left\lfloor \frac{(\tau_{DPCH,n}/256) + 50}{30} \right\rfloor$$

When transmitted to a UE for which the cell is not the E-DCH serving cell, the E-RGCH frame offset relative to P-CCPCH shall be $\tau_{E\text{-}RGCH} = 5120$ chips.

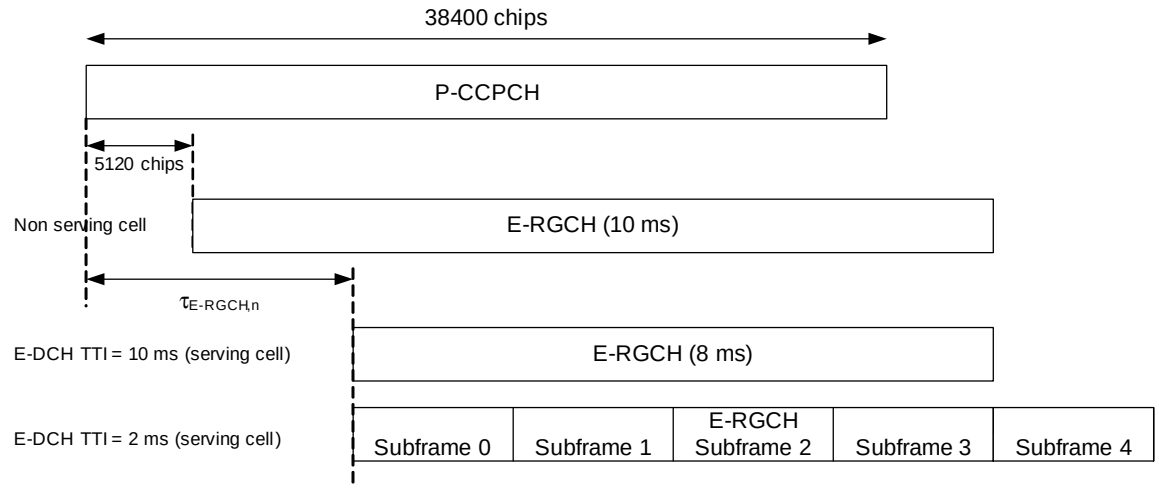

Figure 38: E-RGCH timing

7.12 E-AGCH/P-CCPCH timing relation

The E-AGCH frame offset relative to P-CCPCH shall be $\tau_{E\text{-}AGCH}$ = 5120 chips as illustrated in figure 39.

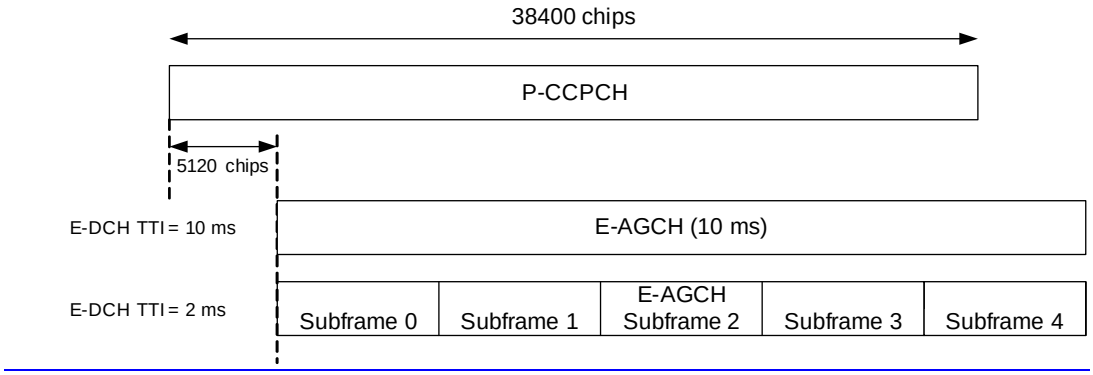

Figure 39: E-AGCH timing