TSG-RAN meeting #18 RP-020710
New Orleans, USA
December 3 – 6 2002

Status Report for SI to TSG

Study Item Name: Feasibility Study for the analysis of higher chip rates for UTRA TDD evolution

SOURCE: Rapporteur (Martin Beale, IPWireless) **TSG:** RAN **WG:** 1

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Ref. to SI sheet: RAN_Study_Items.doc

Progress Report since the last TSG (for all involved WGs):

RAN1#28bis: The skeleton draft TR25.895 “Analysis of Higher Chip Rates for UTRA TDD” was introduced and discussed. It was agreed that the TR will contain a reference configuration based on a chip rate of 7.68Mcps, there will be an analysis of link and system level performance and complexity. The feasibility of higher chip rates is to be considered in the TR.

RAN1#29: Contributions to the draft TR on the reference configuration to be studied were presented and agreed. The contributions aimed to introduce minimal changes from HCR-TDD. The reference configuration is complete in terms of multiplexing and channel coding and spreading and modulation. Midamble sequences need to be defined in order to complete the description of physical channels and mapping of transport channels to physical channels. Link performance analyses for reference channels can commence once these last remaining aspects of the reference configuration have been agreed. The reference configuration is however sufficiently complete in order to simulate some aspects of higher chip rate UTRA TDD (such as synchronisation aspects)

List of Completed elements (for complex work items):

- Elements of the reference configuration have been completed.

List of open issues:

- Finalisation of reference configuration.
- Simulation assumptions.
- Link, system and complexity analyses.
- Feasibility analysis.

Estimates of the level of completion (when possible):

10%

SI completion date review resulting from the discussion at the working group:

June 2003

References to WG's internal documentation and/or TRs: