TSG-RAN Meeting No. 18 ***TSGRP-020707***
Dec. 3-6, 2002, New Orleans, U.S.A

Status Report for SI to TSG

Study Item Name: Improvement of Inter-frequency and inter-system measurement for 1.28Mcps TDD

SOURCE: Rapporteur **TSG: RAN** **WG: WG1**

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Ref. to SI sheet: RAN_Study_Items.doc

Progress Report since the last TSG (for all involved WGs):

RAN1:

RAN1 28bis:

[2] [3] presented the performance evaluation and simulation for both asymmetric time slot allocation pattern and combination of different time slot allocation pattern in all the possible four scenarios. Several comments were proposed to further revise the related text proposals.

RAN1 29:

References [4][5] presented the revised contents of the text proposals based on [2][3]. Revised contributions for text proposal were agreed in this meeting. Reference [6] analysed the impact on beam-forming and DCA for both asymmetric pattern and pattern combination scheme, and it was also agreed. Finally, three parts of text proposal from [4][5][6] were agreed to be included into TR 25.888. Due to the lack of time, updated TR [7] was posted and approved via RAN1 email reflector. It was also agreed to present the approved TR 25.888 with version 1.1.0 in the RAN plenary meeting #18 for the information.

RAN2: There is no progress since the last TSG RAN meeting.

RAN3: There is no progress since the last TSG RAN meeting.

RAN4: There is no need of further progress.

List of Completed elements (for complex work items):

RAN1:

Agreement on the study areas of the SI

Completion of the performance evaluation and simulation for the asymmetric time slot allocation pattern to all the possible scenarios

Completion of the performance evaluation and simulation for the combination of different time slot allocation pattern

Completion of the analysis of the impact on beam-forming for the asymmetric pattern and pattern combination scheme.

RAN2: Clarification of the SI.

RAN3: Completion of internal skeleton TR for signalling support.

RAN4: Agreement on the impact to the WG4 related specifications

List of open issues:

- For the asymmetric time slot allocation pattern to all the possible scenarios, necessary upper layer signaling and impact on DCA, power control and uplink synchronization function.
- For the combination of different time slot allocation pattern, necessary upper layer signaling and impact on DCA, power control and uplink synchronization function.
- Improved signalling support for the specific measurement scheme.

Estimates of the level of completion (when possible):

45 %

SI completion date review:

TSG RAN #19 (March 2003)

References to WG's internal documentation and/or TRs:

[1] 3GPP TSG RP 02-0508 “TR25.888 of inter-RAT measurement improvement for LCR TDD”, Samsung Electronics, Sep. 2002.

[2] 3GPP TSG R1-02-1200, “Comparison of asymmetric pattern and conventional scheme used for different measurement purposes (Revision of R1-02-1060)”, Samsung Electronics, Oct. 2002.

[3] 3GPP TSG R1-02-1201, “Comparison of pattern combination and conventional scheme used for different measurement purposes (Revision of R1-02-1125)”, Samsung Electronics, Oct. 2002.

[4] 3GPP TSG R1-02-1424, “Comparison of asymmetric pattern and conventional scheme used for different measurement purposes- Rev.3 (Revision of R1-02-1274)”, Samsung Electronics, Nov. 2002.

[5] 3GPP TSG R1-02-1425, “Comparison of pattern combination and conventional scheme used for different measurement purposes- Rev.3 (Revision of R1-02-1275)”, Samsung Electronics, Nov. 2002.

[6] 3GPP TSG R1-02-1426, “Analysis of asymmetric pattern and pattern combination scheme impact on beam-forming and DCA Rev 1(R1-02-1416)”, Samsung Electronics, Nov. 2002.

[7] 3GPP TSG R1-02-1442, “Update TR 25.888”, Samsung Electronics, Nov. 2002.