TSG-RAN Meeting #6
Nice, France, 13 – 15 December 1999

TSGRP#6(99)677

Title: **Agreed CRs of category "C" (Modification) and "F" (correction) to TS 25.211**

Source: **TSG-RAN WG1**

Agenda item: **5.1.3**

Spec	CR	Rev	Phase	Subject	Cat	Version-Current	Version-New	Doc
25.211	001	1	R99	Removal of superframe notation	F	3.0.0	3.1.0	R1-99h47
25.211	002	-	R99	Use of CPICH in case of open loop Tx diversity	C	3.0.0	3.1.0	R1-99g90
25.211	003	2	R99	CPCH power control preamble length	C	3.0.0	3.1.0	R1-99i09
25.211	005	1	R99	Editorial corrections	F	3.0.0	3.1.0	R1-99h48
25.211	016	-	R99	TAB structure and timing relation for USTS	C	3.0.0	3.1.0	R1-99l29
25.211	017	-	R99	Timing for initialisation procedures	C	3.0.0	3.1.0	R1-99k52
25.211	022	-	R99	Modification of the STTD encoding scheme on DL DPCH	C	3.0.0	3.1.0	R1-99j05

3GPP TSG RAN WG1 Meeting #9
Dresden, Germany, Nov 30 - Dec 3, 1999

Document R1-99h47
e.g. for 3GPP use the format TP-99xxx
or for SMG, use the format P-99-xxx

CHANGE REQUEST

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25.211	CR	001r1	Current Version:	3.0.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to:	TSG-RAN #6	for approval	X	strategic		(for SMG use only)
list expected approval meeting # here ↑		for information		non-strategic		

Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from:* ftp://ftp.3gpp.org/Information/CR-Form-v2.doc

Proposed change affects: *(at least one should be marked with an X)*	(U)SIM		ME	X	UTRAN / Radio	X	Core Network	

Source: ~~Ericsson~~RAN WG1 **Date:** 1999-11-19

Subject: Removal of superframe notation

Work item: TS25.211

Category: *(only one category shall be marked with an X)*

F	Correction	X	**Release:**	Phase 2	
A	Corresponds to a correction in an earlier release			Release 96	
B	Addition of feature			Release 97	
C	Functional modification of feature			Release 98	
D	Editorial modification			Release 99	
				Release 00	

Reason for change: From WG1 perspective there is no more need for the superframe concept in the Layer 1 specifications. Also WG2 has expressed no need for this. It is proposed to remove any reference to the superframe from Layer 1 FDD specifications.
Note that it is still possible to uniquely identify any frame within a 40.96s window by means of a 12bit SFN (=System Frame Number) encoded on the P-CCPCH channel.

Clauses affected: 5., 5.2.1, 5.3.2, 5.3.3.1, 5.3.3.2, 5.3.3.3 and 5.3.3.5 of TS25.211

Other specs affected:

Other 3G core specifications		→ List of CRs:
Other GSM core specifications		→ List of CRs:
MS test specifications		→ List of CRs:
BSS test specifications		→ List of CRs:
O&M specifications		→ List of CRs:

Other comments:


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<--------- double-click here for help and instructions on how to create a CR.

5 Physical channels

Physical channels typically consist of a ~~three~~ layered structure of ~~superframes,~~ radio frames~~,~~ and time slots, although this is not true for all physical channels. Depending on the symbol rate of the physical channel, the configuration of radio frames or time slots varies.

~~Superframe: A Superframe has a duration of 720ms and consists of 72 radio frames. The superframe boundaries are defined by the System Frame Number (SFN):~~

~~The head radio frame of superframe : SFN mod 72=0.~~

~~The tail radio frame of superframe: SFN mod 72=71.~~

Radio frame: A Radio frame is a processing unit which consists of 15 time slots.

Time slot: A Time slot is a unit which consists of fields containing bits. The number of bits per time slot depends on the physical channel.

5.1 The physical resource

The basic physical resource is the code/frequency plane. In addition, on the uplink, different information streams may be transmitted on the I and Q branch. Consequently, a physical channel corresponds to a specific carrier frequency, code, and, on the uplink, relative phase (0 or $\pi/2$).

5.2 Uplink physical channels

5.2.1 Dedicated uplink physical channels

There are two types of uplink dedicated physical channels, the uplink Dedicated Physical Data Channel (uplink DPDCH) and the uplink Dedicated Physical Control Channel (uplink DPCCH).

The DPDCH and the DPCCH are I/Q code multiplexed within each radio frame (see [4]).

The uplink DPDCH is used to carry dedicated data generated at Layer 2 and above, i.e. the dedicated transport channel (DCH). There may be zero, one, or several uplink DPDCHs on each Layer 1 connection.

The uplink DPCCH is used to carry control information generated at Layer 1. The Layer 1 control information consists of known pilot bits to support channel estimation for coherent detection, transmit power-control (TPC) commands, feedback information (FBI), and an optional transport-format combination indicator (TFCI). The transport-format combination indicator informs the receiver about the instantaneous parameters of the different transport channels multiplexed on the uplink DPDCH, and corresponds to the data transmitted in the same frame. It is the UTRAN that determines if a TFCI should be transmitted, hence making it is mandatory for all UEs to support the use of TFCI in the uplink. There is one and only one uplink DPCCH on each Layer 1 connection.

Figure 1 shows the frame structure of the uplink dedicated physical channels. Each frame of length 10 ms is split into 15 slots, each of length T_{slot} = 2560 chips, corresponding to one power-control period~~. A super frame corresponds to 72 consecutive frames, i.e. the super frame length is 720 ms.~~

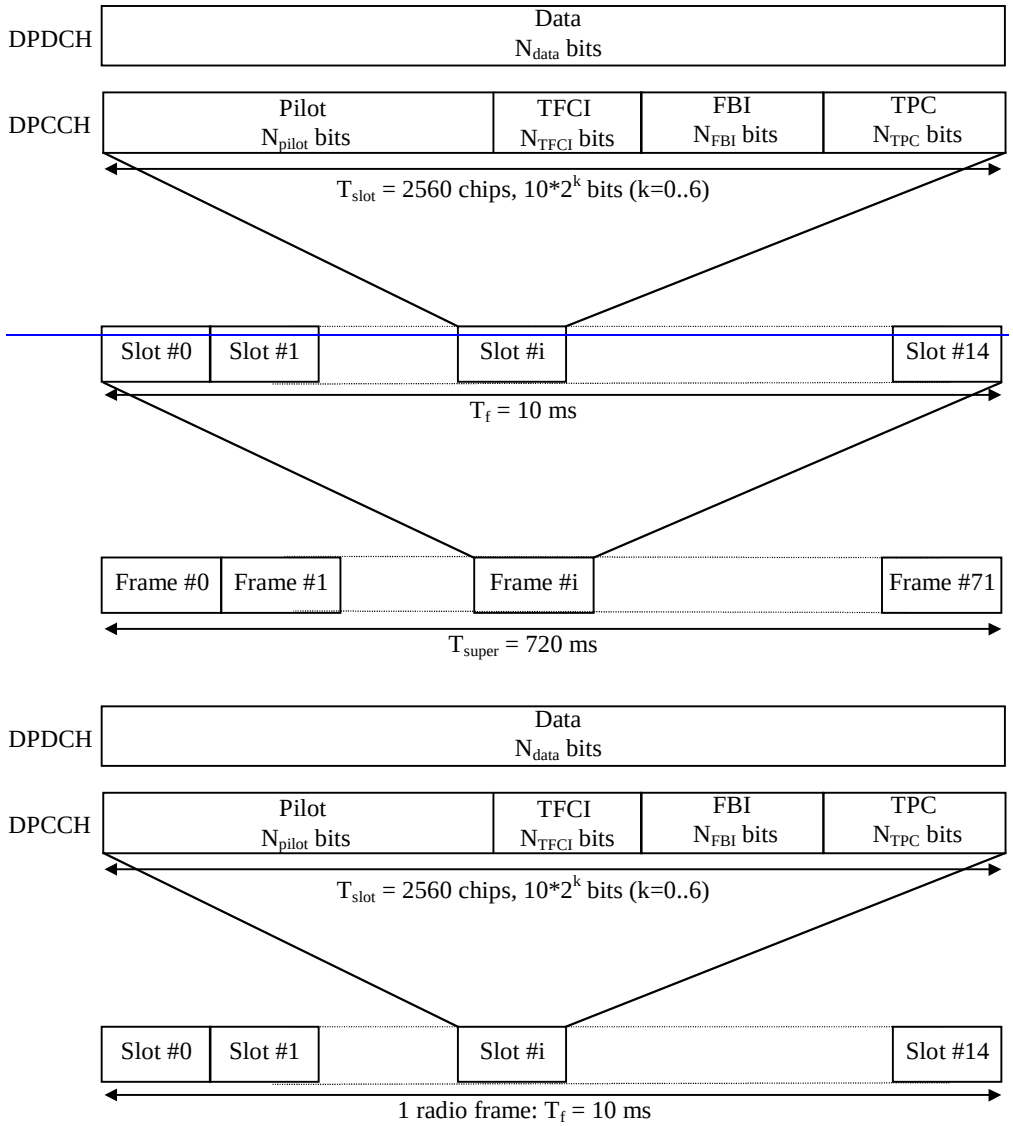

Figure 1: Frame structure for uplink DPDCH/DPCCH

The parameter k in figure 1 determines the number of bits per uplink DPDCH/DPCCH slot. It is related to the spreading factor SF of the physical channel as SF = $256/2^k$. The DPDCH spreading factor may thus range from 256 down to 4. Note that an uplink DPDCH and uplink DPCCH on the same Layer 1 connection generally are of different rates, i.e. have different spreading factors and different values of k.

The exact number of bits of the different uplink DPCCH fields (N_{pilot}, N_{TFCI}, N_{FBI}, and N_{TPC}) is determined in table 2. The field order and total number of bits/slot are fixed, though the number of bits per field may vary during a connection.

The values for the number of bits per field are given in table 1 and table 2. The channel bit and symbol rates given in table 1 are the rates immediately before spreading. The pilot patterns are given in table 3 and table 4, the TPC bit pattern is given in table 5.

The N_{FBI} bits are used to support techniques requiring feedback between the UE and the UTRAN Access Point (=cell transceiver), including closed loop mode transmit diversity and site selection diversity (SSDT). The exact details of the FBI field are shown in figure 2 and described below.

5.3.2 Dedicated downlink physical channels

There is only one type of downlink dedicated physical channel, the Downlink Dedicated Physical Channel (downlink DPCH).

Within one downlink DPCH, dedicated data generated at Layer 2 and above, i.e. the dedicated transport channel (DCH), is transmitted in time-multiplex with control information generated at Layer 1 (known pilot bits, TPC commands, and an optional TFCI). The downlink DPCH can thus be seen as a time multiplex of a downlink DPDCH and a downlink DPCCH, compare section 5.2.1. It is the UTRAN that determines if a TFCI should be transmitted, hence making it is mandatory for all UEs to support the use of TFCI in the downlink.

Figure 10 shows the frame structure of the downlink DPCH. Each frame of length 10 ms is split into 15 slots, each of length T_{slot} = 2560 chips, corresponding to one power-control period. ~~A super frame corresponds to 72 consecutive frames, i.e. the super frame length is 720 ms.~~

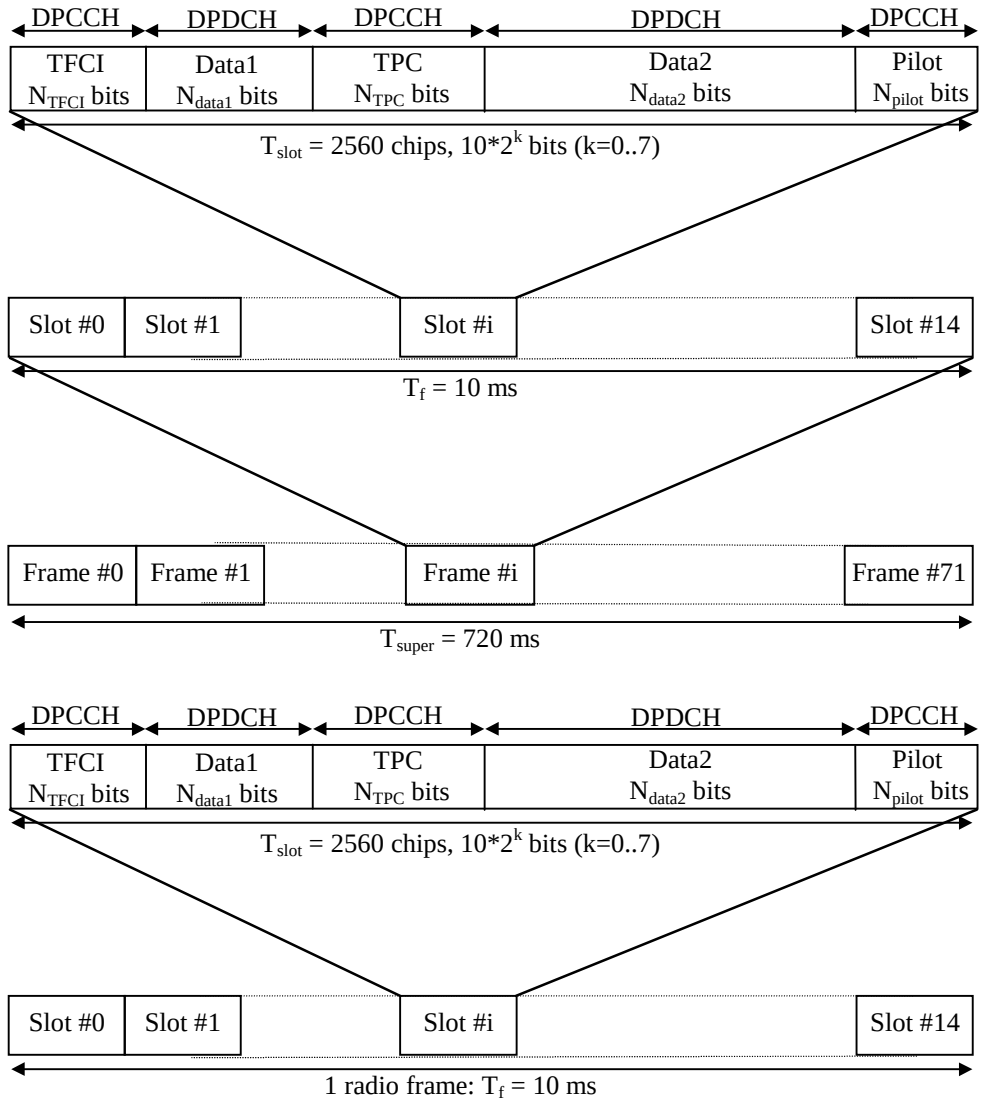

Figure 10: Frame structure for downlink DPCH

The parameter k in figure 10 determines the total number of bits per downlink DPCH slot. It is related to the spreading factor SF of the physical channel as $SF = 512/2^k$. The spreading factor may thus range from 512 down to 4.

The exact number of bits of the different downlink DPCH fields (N_{pilot}, N_{TPC}, N_{TFCI}, N_{data1} and N_{data2}) is determined in table 11.The overhead due to the DPCCH transmission has to be negotiated at the connection set-up and can be re-negotiated during the communication, in order to match particular propagation conditions.

5.3.3 Common downlink physical channels

5.3.3.1 Common Pilot Channel (CPICH)

The CPICH is a fixed rate (30 kbps, SF=256) downlink physical channel that carries a pre-defined bit/symbol sequence. Figure 13 shows the frame structure of the CPICH.

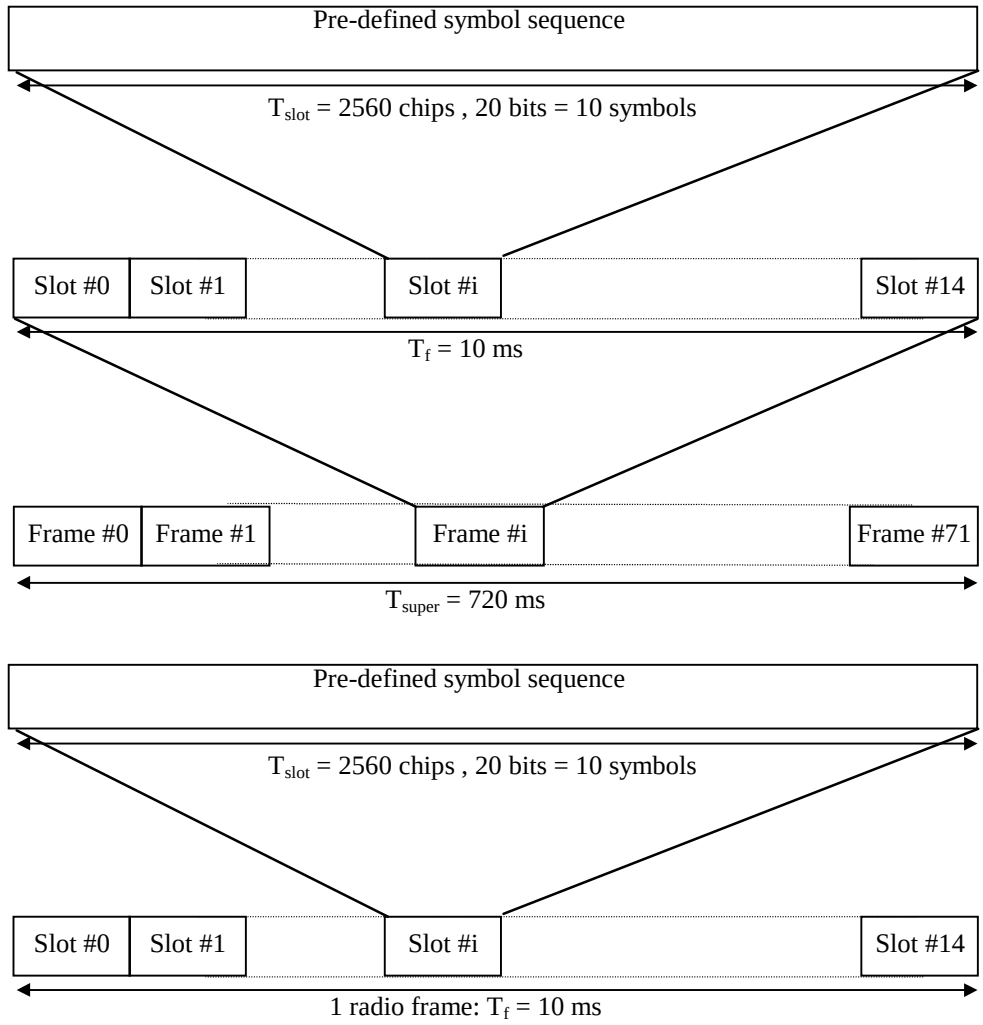

Figure 13: Frame structure for Common Pilot Channel

In case of Transmit Diversity (open or closed loop), the CPICH should be transmitted from both antennas using the same channelization and scrambling code. In this case, the pre-defined symbol sequence of the CPICH is different for Antenna 1 and Antenna 2, see figure 14. In case of no Transmit Diversity, the symbol sequence of Antenna 1 in figure 14 is used.

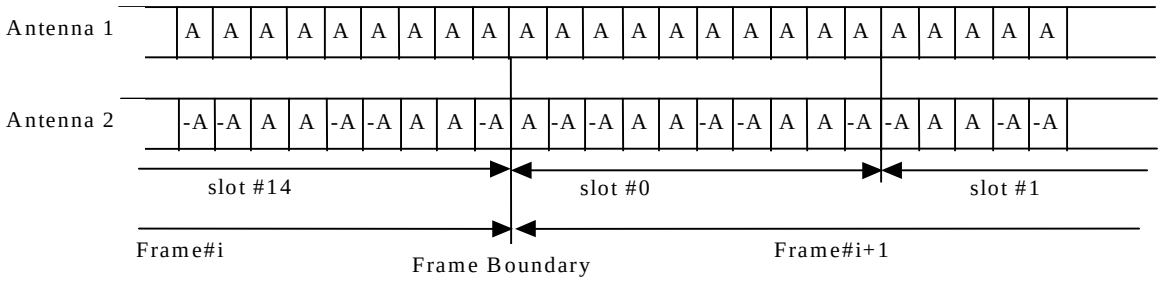

Figure 14: Modulation pattern for Common Pilot Channel (with A = 1+j)

5.3.3.2 Primary Common Control Physical Channel (P-CCPCH)

The Primary CCPCH is a fixed rate (30 kbps, SF=256) downlink physical channels used to carry the BCH.

Figure 15 shows the frame structure of the Primary CCPCH. The frame structure differs from the downlink DPCH in that no TPC commands, no TFCI and no pilot bits are transmitted The Primary CCPCH is not transmitted during the first 256 chips of each slot. Instead, Primary SCH and Secondary SCH are transmitted during this period (see section 5.3.3.4).

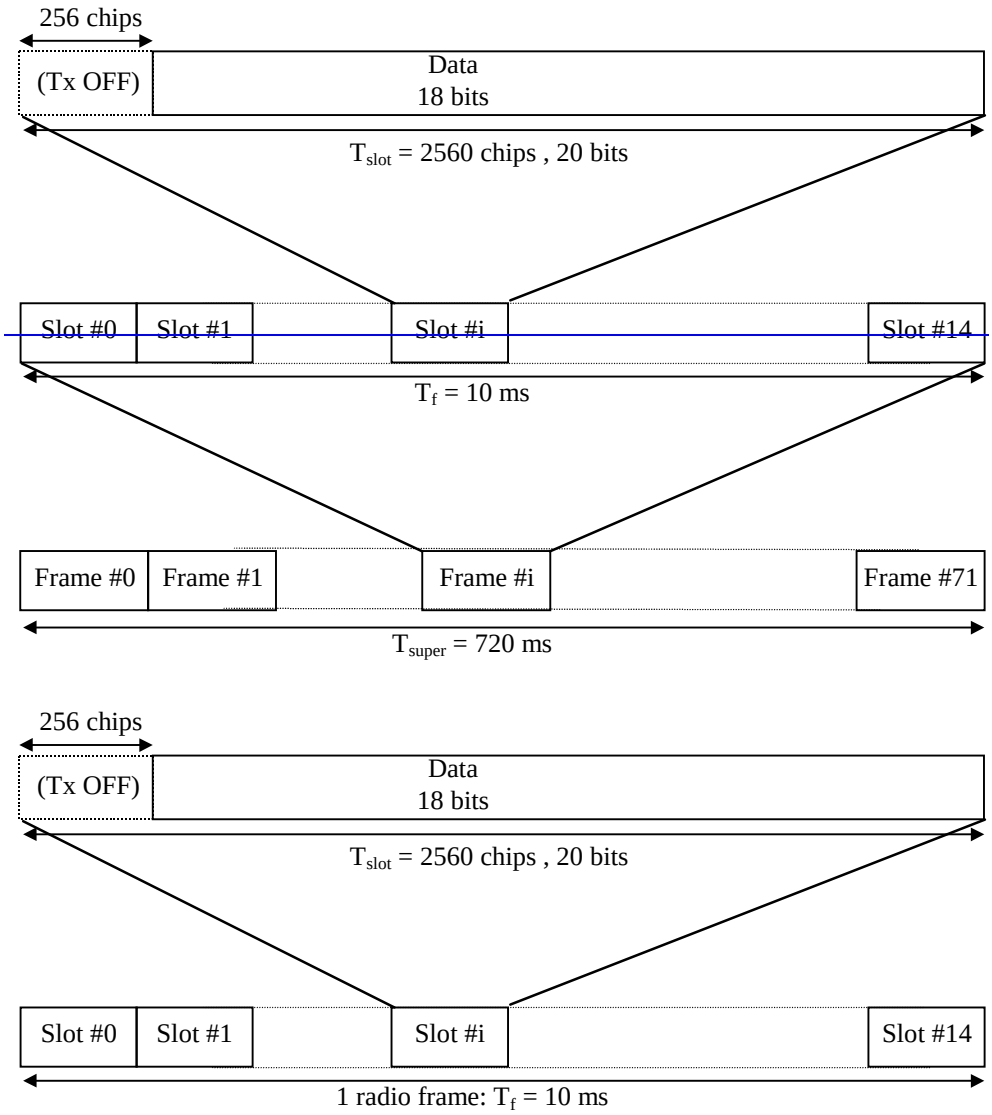

Figure 15: Frame structure for Primary Common Control Physical Channel

5.3.3.3 Secondary Common Control Physical Channel (S-CCPCH)

The Secondary CCPCH is used to carry the FACH and PCH. There are two types of Secondary CCPCH: those that include TFCI and those that do not include TFCI. It is the UTRAN that determines if a TFCI should be transmitted, hence making it mandatory for all UEs to support the use of TFCI. The set of possible rates is the same as for the downlink DPCH, see section 5.3.2. The frame structure of the Secondary CCPCH is shown in figure 17.

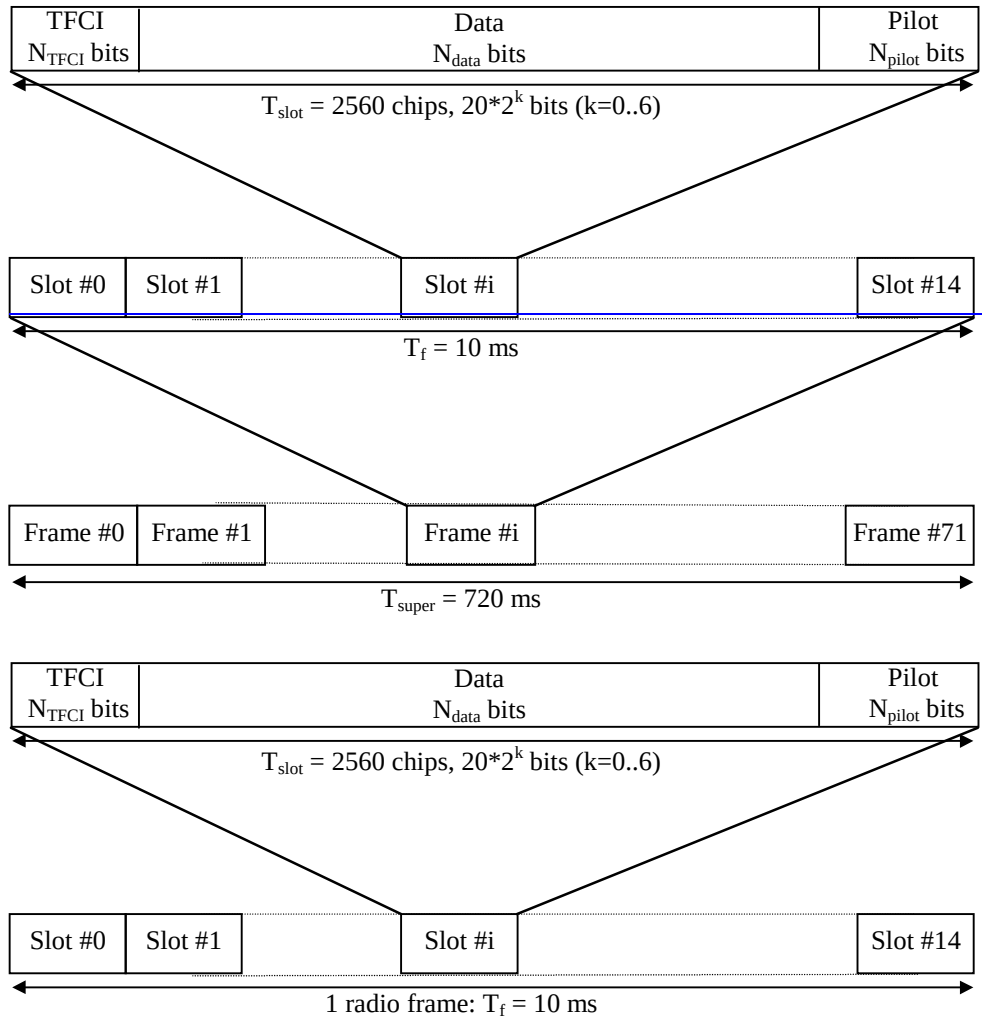

Figure 17: Frame structure for Secondary Common Control Physical Channel

The parameter k in figure 17 determines the total number of bits per downlink Secondary CCPCH slot. It is related to the spreading factor SF of the physical channel as $SF = 256/2^k$. The spreading factor range is from 256 down to 4.

The values for the number of bits per field are given in table 16 and table 17. The channel bit and symbol rates given in table 16 are the rates immediately before spreading. The pilot patterns are given in table 18.

The FACH and PCH can be mapped to the same or to separate Secondary CCPCHs. If FACH and PCH are mapped to the same Secondary CCPCH, they can be mapped to the same frame. The main difference between a CCPCH and a downlink dedicated physical channel is that a CCPCH is not inner-loop power controlled. The main difference between the Primary and Secondary CCPCH is that the Primary CCPCH has a fixed predefined rate while the Secondary CCPCH can support variable rate with the help of the TFCI field included. Furthermore, a Primary CCPCH is continuously transmitted over the entire cell while a Secondary CCPCH is only transmitted when there is data available and may be transmitted in a narrow lobe in the same way as a dedicated physical channel (only valid for a Secondary CCPCH carrying the FACH).

5.3.3.5 Physical Downlink Shared Channel (PDSCH)

The Physical Downlink Shared Channel (PDSCH), used to carry the Downlink Shared Channel (DSCH), is shared by users based on code multiplexing. As the DSCH is always associated with a DCH, the PDSCH is always associated with a downlink DPCH.

The frame and slot structure of the PDSCH are shown on figure 20.

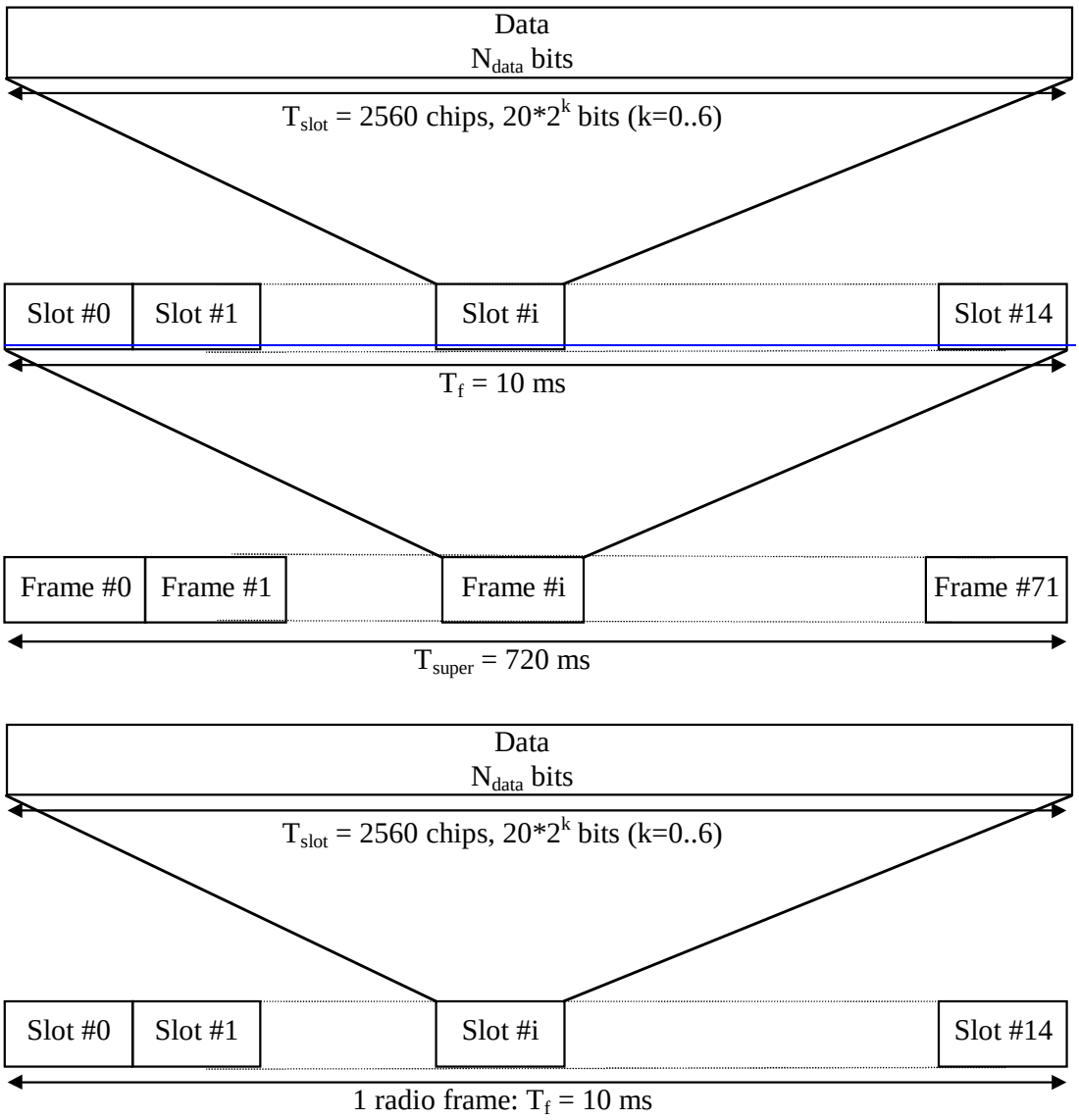

Figure 20: Frame structure for the PDSCH

To indicate for UE that there is data to decode on the DSCH, two signalling methods are possible, either using the TFCI field, or higher layer signalling.

The PDSCH transmission with associated DPCH is a special case of multicode transmission. The PDSCH and DPCH do not have necessary the same spreading factors and for PDSCH the spreading factor may vary from frame to frame. The relevant Layer 1 control information is transmitted on the DPCCH part of the associated DPCH, the PDSCH does not contain physical layer information. The channel bit and symbol rates for PDSCH are given in table 20.

For PDSCH the allowed spreading factors may vary from 256 to 4.

If the spreading factor and other physical layer parameters can vary on a frame-by-frame basis, the TFCI shall be used to inform the UE what are the instantaneous parameters of PDSCH including the channelisation code from the PDSCH OVSF code tree.

3GPP TSG-R WG1 meeting #8
New York, USA, 12-15 Oct. 1999

Document* *R1-99g90

CHANGE REQUEST

25.211	**CR**	**002**	Current Version:	3.0.0

For submission to: TSG-R #6 — for approval [X] / for information [ ] — strategic [ ] / non-strategic [ ]

Proposed change affects: (U)SIM [ ] ME [ ] UTRAN / Radio [X] Core Network [ ]

Source: ~~Nokia~~RAN WG1 **Date:** 15/10/1999

Subject: Use of CPICH in case of open loop Tx diversity

Work item: TS 25.211

Category:

F	Correction	[ ]
A	Corresponds to a correction in an earlier release	[ ]
B	Addition of feature	[ ]
C	Functional modification of feature	[X]
D	Editorial modification	[ ]

Release:

Phase 2	[ ]
Release 96	[ ]
Release 97	[ ]
Release 98	[ ]
Release 99	[X]
Release 00	[ ]

Reason for change: Use of CPICH is simplified and performance improved especially in case of small number of dedicated pilot symbols

Clauses affected: 5.3.3.1

Other specs affected:

Other 3G core specifications	[ ]	→ List of CRs:
Other GSM core specifications	[ ]	→ List of CRs:
MS test specifications	[ ]	→ List of CRs:
BSS test specifications	[ ]	→ List of CRs:
O&M specifications	[ ]	→ List of CRs:

Other comments:

1.1.1.1 Common Pilot Channel (CPICH)

The CPICH is a fixed rate (30 kbps, SF=256) downlink physical channel that carries a pre-defined bit/symbol sequence. Figure 1~~Figure 1~~ shows the frame structure of the CPICH.

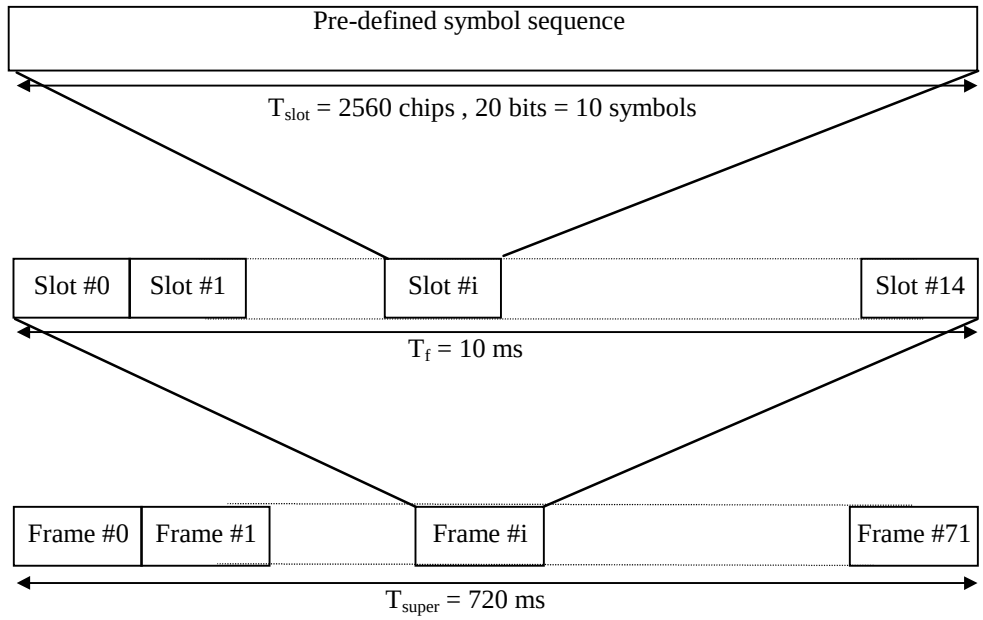

Figure 1: Frame structure for Common Pilot Channel.

In case of Transmit Diversity (open or closed loop), the CPICH ~~should~~ shall be transmitted from both antennas using the same channelization and scrambling code. In this case, the pre-defined symbol sequence of the CPICH is different for Antenna 1 and Antenna 2, see Figure 2~~Figure 2~~. In case of no Transmit Diversity, the symbol sequence of Antenna 1 in Figure 2~~Figure 2~~ is used.

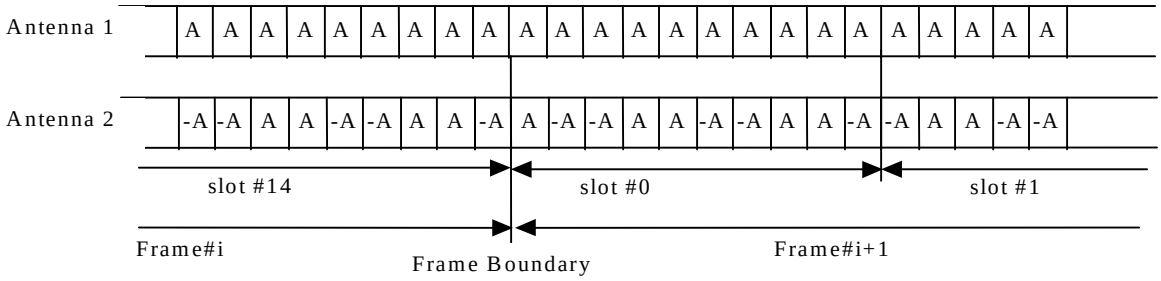

Figure ~~2~~2: Modulation pattern for Common Pilot Channel (with A = 1+j).

There are two types of Common pilot channels, the Primary and Secondary CPICH. They differ in their use and the limitations placed on their physical features.

Agenda item:	**WG1 Plenary**
Source:	**Philips, Nokia**
Title:	**Revised Text Proposal and Change Request for CPCH power control preamble length**
Document for:	**Decision**

Introduction

In the Adhoc 14 meeting at WG1#8, it was agreed that the length of the CPCH power control preamble should be a higher layer parameter which can take one of 2 values, 0 slots or 8 slots.

This paper is a re-submission of the corresponding text proposal and change requests contained in R1-99h02 and agreed in adhoc 14 at WG1#8.

The previously agreed CRs 25211-003 and 25214-006 have now been updated to use the new version of the CR form.

In addition, CR25211-003 has been modified to update another reference to the power control preamble length which had been missed in the first version of the CR.

3GPP TSG RAN WG1 Meeting #9
Dresden, Germany, Nov 30 – Dec 3, 1999

Document R1-99i09
e.g. for 3GPP use the format TP-99xxx
or for SMG, use the format P-99-xxx

CHANGE REQUEST

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3G25.211	CR	003rev2	Current Version:	3.0.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to:	TSG-RAN #6	for approval	X	strategic		(for SMG use only)
list expected approval meeting # here ↑		for information		non-strategic		

Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc*

Proposed change affects: *(at least one should be marked with an X)* (U)SIM [ ] ME [X] UTRAN / Radio [X] Core Network [ ]

Source: Philips, Nokia **Date:** 1999-11-18

Subject: CPCH power control preamble length

Work item:

Category: *(only one category shall be marked with an X)*

F	Correction	
A	Corresponds to a correction in an earlier release	
B	Addition of feature	
C	Functional modification of feature	X
D	Editorial modification	

Release:

Phase 2	
Release 96	
Release 97	
Release 98	
Release 99	X
Release 00	

Reason for change: Resolution of “ffs” item.

Clauses affected: 5.2.2.2.1 “CPCH transmission”,
5.2.2.2.4 “CPCH power control preamble part”,
7.4 “PCPCH/AICH timing relation”

Other specs affected:

Other 3G core specifications	X	→ List of CRs:	25214-006rev2
Other GSM core specifications		→ List of CRs:	
MS test specifications		→ List of CRs:	
BSS test specifications		→ List of CRs:	
O&M specifications		→ List of CRs:	

Other comments:


help.doc

<---------- double-click here for help and instructions on how to create a CR.

5.2.2.2.1 CPCH transmission

The CPCH transmission is based on DSMA-CD approach with fast acquisition indication. The UE can start transmission at a number of well-defined time-offsets, relative to the frame boundary of the received BCH of the current cell. The access slot timing and structure is identical to RACH in section 5.2.2.1.1. The structure of the CPCH random access transmission is shown in figure 6. The CPCH random access transmission consists of one or several Access Preambles [A-P] of length 4096 chips, one Collision Detection Preamble (CD-P) of length 4096 chips, a DPCCH Power Control Preamble (PC-P) which is either 0 slots or 8 slots in length, and a message of variable length Nx10 ms.

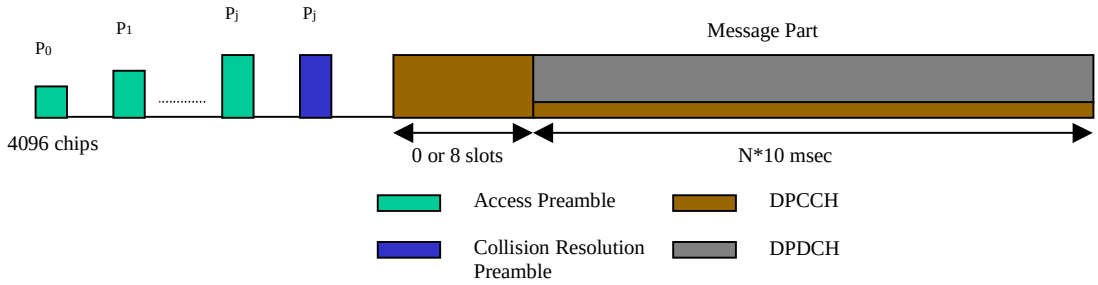

Figure 6: Structure of the CPCH random access transmission

5.2.2.2.2 CPCH access preamble part

Similar to 5.2.2.1.2 (RACH preamble part). The RACH preamble signature sequences are used. The number of sequences used could be less than the ones used in the RACH preamble. The scrambling code could either be chosen to be a different code segment of the Gold code used to form the scrambling code of the RACH preambles (see [4] for more details) or could be the same scrambling code in case the signature set is shared.

5.2.2.2.3 CPCH collision detection preamble part

Similar to 5.2.2.1.2 (RACH preamble part). The RACH preamble signature sequences are used. The scrambling code is chosen to be a different code segment of the Gold code used to form the scrambling code for the RACH and CPCH preambles (see [4] for more details).

5.2.2.2.4 CPCH power control preamble part

The power control preamble segment is a DPCCH Power Control Preamble (PC-P). The following table 9 is identical to Rows 2 and 4 of table 2 in section 5.2.1. Table 9 defines the DPCCH fields which only include Pilot, FBI and TPC bits. The Power Control Preamble length is a parameter which shall take the values 0 or 8 slots, as set by the higher layers.

Table 9: DPCCH fields for CPCH power control preamble segment.

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{pilot}	N_{TFCI}	N_{FBI}	N_{TPC}
0	15	15	256	150	10	8	0	0	2
1	15	15	256	150	10	7	0	1	2

7.4 PCPCH/AICH timing relation

Transmission of random access bursts on the PCPCH is aligned with access slot times. The timing of the access slots is derived from the received Primary CCPCH timing The transmit timing of access slot n starts n×20/15 ms after the frame boundary of the received Primary CCPCH, where n = 0, 1, …,14. In addition, transmission of access preambles in PCPCH is limited to the allocated access slot subchannel group which is assigned by higher layer signalling to each CPCH set. Twelve access slot subchannels are defined and PCPCH may be allocated all subchannel slots or any subset of the twelve subchannel slots. The access slot subchannel identification is identical to that for the RACH and is described in table 6 of section 6.1 of [5].

Everything in the previous section [PRACH/AICH] applies to this section as well. The timing relationship between preambles, AICH, and the message is the same as PRACH/AICH. Note that the collision resolution preambles follow the access preambles in PCPCH/AICH. However, the timing relationships between CD-Preamble and CD-AICH is identical to RACH Preamble and AICH. The timing relationship between CD-AICH and the Power Control Preamble in CPCH is identical to AICH to message in RACH. The T_{cpch} timing parameter is identical to the PRACH/AICH transmission timing parameter. When T_{cpch} is set to zero or one, the following PCPCH/AICH timing values apply:

Note that a1 corresponds to AP-AICH and a2 corresponds to CD-AICH.

$\tau_{p\text{-}p}$ = Time to next available access slot, between Access Preambles.

Minimum time = 15360 chips + 5120 chips X Tcpch

Maximum time = 5120 chips X 12 = 61440 chips

Actual time is time to next slot (which meets minimum time criterion) in allocated access slot subchannel group.

$\tau_{p\text{-}a1}$ = Time between Access Preamble and AP-AICH has two alternative values: 7680 chips or 12800 chips, depending on T_{cpch}

$\tau_{a1\text{-}cdp}$ = Time between receipt of AP-AICH and transmission of the CD Preamble has one value: 7680 chips.

$\tau_{p\text{-}cdp}$ = Time between the last AP and CD Preamble. is either 3 or 4 access slots, depending on T_{cpch}

$\tau_{cdp\text{-}a2}$ = Time between the CD Preamble and the CD-AICH has two alternative values: 7680 chips or 12800 chips, depending on T_{cpch}

$\tau_{cdp\text{-}pcp}$ = Time between CD Preamble and the start of the Power Control Preamble is either 3 or 4 access slots, depending on $T_{cpch.}$

Figure 27 illustrates the PCPCH/AICH timing relationship whenT_{cpch} is set to 0 and all access slot subchannels are available for PCPCH.

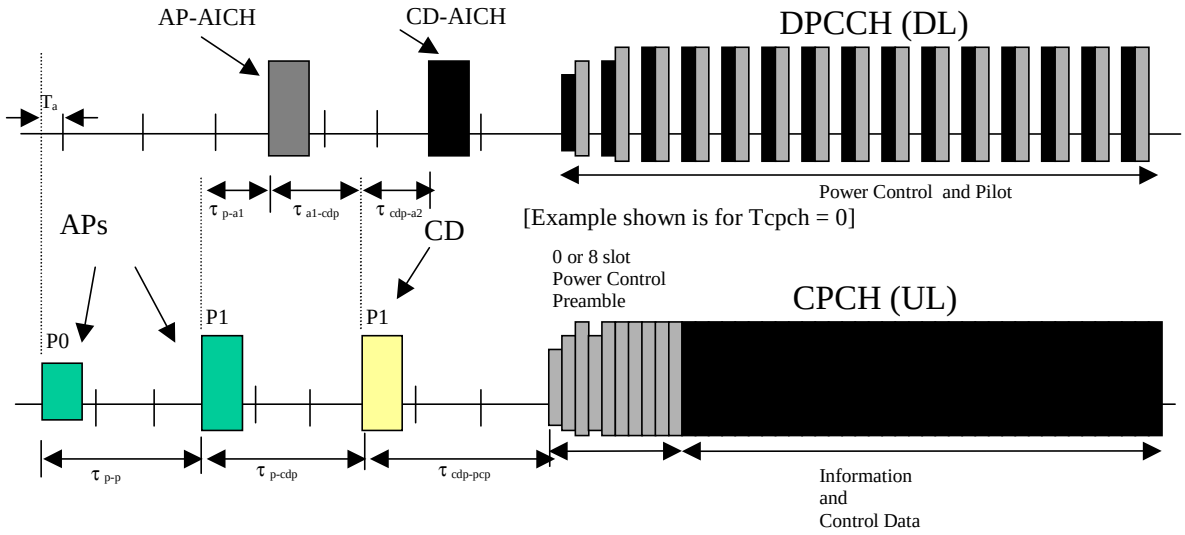

Figure 27: Timing of PCPCH and AICH transmission as seen by the UE, with T_{cpch}= 0

7.5 DPCH/PDSCH timing

The relative timing between a DPCH frame and the associated PDSCH frame is shown in figure 28.

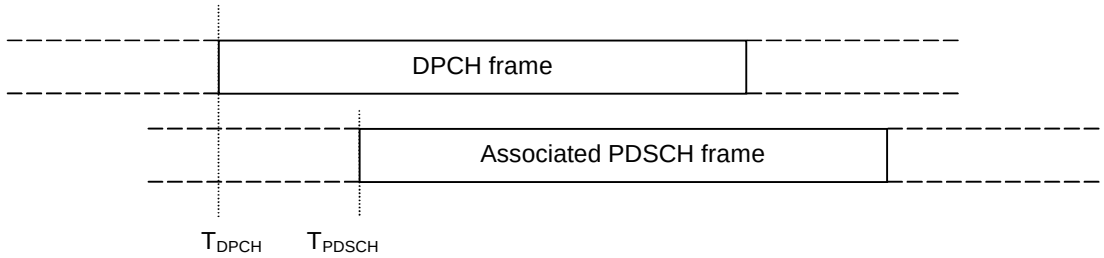

Figure 28: Timing relation between DPCH frame and associated PDSCH frame

The start of a DPCH frame is denoted T_{DPCH} and the start of the associated PDSCH frame is denoted T_{PDSCH}. Any DPCH frame is associated to one PDSCH frame through the relation -35840 chips < T_{DPCH} - T_{PDSCH} ≤ 2560 chips, i.e. the associated PDSCH frame starts anywhere between 1 slot before or up to 14 slots behind the DPCH.

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Document R1-99i09
e.g. for 3GPP use the format TP-99xxx
or for SMG, use the format P-99-xxx

CHANGE REQUEST

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3G25.214	CR	006rev2	Current Version:	3.0.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to:	TSG-RAN #6	for approval	X	strategic		(for SMG use only)
list expected approval meeting # here ↑		for information		non-strategic		

Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc*

Proposed change affects: *(at least one should be marked with an X)* (U)SIM [ ] ME [X] UTRAN / Radio [X] Core Network [ ]

Source: Philips, Nokia **Date:** 1999-11-18

Subject: CPCH power control preamble length

Work item:

Category: *(only one category shall be marked with an X)*

F	Correction	
A	Corresponds to a correction in an earlier release	
B	Addition of feature	
C	Functional modification of feature	X
D	Editorial modification	

Release:

Phase 2	
Release 96	
Release 97	
Release 98	
Release 99	X
Release 00	

Reason for change: Resolution of “ffs” item from TS25.211.

Clauses affected: 6.2 “CPCH Access Procedures”

Other specs affected:

Other 3G core specifications	X	→ List of CRs:	25211-003rev2
Other GSM core specifications		→ List of CRs:	
MS test specifications		→ List of CRs:	
BSS test specifications		→ List of CRs:	
O&M specifications		→ List of CRs:	

Other comments:


help.doc

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6.2 CPCH Access Procedures

For each CPCH physical channel in a CPCH set allocated to a cell the following physical layer parameters are included in the System Information message:

- UL Access Preamble (AP) scrambling code.
- UL Access Preamble signature set
- The Access preamble slot sub-channels group
- AP- AICH preamble channelization code.
- UL Collision Detection(CD) preamble scrambling code.
- CD Preamble signature set
- CD preamble slot sub-channels group
- CD-AICH preamble channelization code.
- CPCH UL scrambling code.
- CPCH UL channelization code. (variable, data rate dependant)
- DPCCH DL channelization code.([512] chip)

NOTE: There may be some overlap between the AP signature set and CD signature set if they correspond to the same scrambling code.

The following are access, collision detection/resolution and CPCH data transmission parameters:

Power ramp-up, Access and Timing parameters (Physical layer parameters)

1) N_AP_retrans_max = Maximum Number of allowed consecutive access attempts (retransmitted preambles) if there is no AICH response. This is a CPCH parameter and is equivalent to Preamble_Retrans_Max in RACH.

2) $P_{RACH} = P_{CPCH}$ = Initial open loop power level for the first CPCH access preamble sent by the UE.

   [RACH/CPCH parameter]

3) ΔP_0 = Power step size for each successive CPCH access preamble.

   [RACH/CPCH parameter]

4) ΔP_1 = Power step size for each successive RACH/CPCH access preamble in case of negative AICH. A timer is set upon receipt of a negative AICH. This timer is used to determine the period after receipt of a negative AICH when ΔP_1 is used in place of ΔP_0.

   [RACH/CPCH parameter]

5) T_{cpch} = CPCH transmission timing parameter: This parameter is identical to PRACH/AICH transmission timing parameter.

   [RACH/CPCH parameter]

6. $L_{pc\text{-}preamble}$ = Length of power control preamble (0 or 8 slots)

   [CPCH parameter]

NOTE: It is FFS if ΔP_0 for the CPCH access may be different from ΔP_0 for the RACH access as defined in section 6.1.

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Document R1-99h48
e.g. for 3GPP use the format TP-99xxx
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CHANGE REQUEST

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25.211	CR	005	Current Version:	3.0.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to:	TSG-RAN #6	for approval	X	strategic		(for SMG use only)
list expected approval meeting # here ↑		for information		non-strategic		

Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from:* ftp://ftp.3gpp.org/Information/CR-Form-v2.doc

Proposed change affects: *(at least one should be marked with an X)* (U)SIM [ ] ME [X] UTRAN / Radio [X] Core Network [ ]

Source: Ericsson **Date:** 1999-11-27

Subject: Editorial corrections

Work item: TS25.211

Category: *(only one category shall be marked with an X)*

F	Correction	X	**Release:**	Phase 2	
A	Corresponds to a correction in an earlier release			Release 96	
B	Addition of feature			Release 97	
C	Functional modification of feature			Release 98	
D	Editorial modification			Release 99	X
				Release 00	

Reason for change: Several editorial corrections are collected in this CR.

Clauses affected: 3.3, 5.2.1, 5.3.2, 5.3.3.1.2, 5.3.3.2, 5.3.3.3, 5.3.3.7, 6, 7.6.3 of TS25.211

Other specs affected:

Other 3G core specifications	[ ]	→ List of CRs:
Other GSM core specifications	[ ]	→ List of CRs:
MS test specifications	[ ]	→ List of CRs:
BSS test specifications	[ ]	→ List of CRs:
O&M specifications	[ ]	→ List of CRs:

Other comments:

help.doc

<--------- double-click here for help and instructions on how to create a CR.

3.3 Abbreviations

For the purposes of the present document, the following abbreviations apply:

AI	Acquisition Indicatior
AICH	Acquisition Indication Channel
AP	Access Preamble
BCH	Broadcast Channel
CCPCH	Common Control Physical Channel
CCTrCH	Coded Composite Transport Channel
CD	Collision Detection
CPCH	Common Packet Channel
CPICH	Common Pilot Channel
DCH	Dedicated Channel
DPCCH	Dedicated Physical Control Channel
DPCH	Dedicated Physical Channel
DPDCH	Dedicated Physical Data Channel
DSCH	Downlink Shared Channel
DTX	Discontinuous Transmission
FACH	Forward Access Channel
FBI	Feedback Information
MUI	Mobile User Identifier
PCH	Paging Channel
P-CCPCH	Primary Common Control Physical Channel
PCPCH	Physical Common Packet Channel
PDSCH	Physical Downlink Shared Channel
PI	Page Indicatior
PICH	Page Indication Channel
PRACH	Physical Random Access Channel
PSC	Primary Synchronisation Code
RACH	Random Access Channel
RNC	Radio Network Controller
S-CCPCH	Secondary Common Control Physical Channel
SCH	Synchronisation Channel
SF	Spreading Factor
SFN	System Frame Number
SSC	Secondary Synchronisation Code
STTD	Space Time Transmit Diversity
TFCI	Transport Format Combination Indicator
TSTD	Time Switched Transmit Diversity
TPC	Transmit Power Control
UE	User Equipment
UTRAN	UMTS Terrestrial Radio Access Network

5.2.1 Dedicated uplink physical channels

There are two types of uplink dedicated physical channels, the uplink Dedicated Physical Data Channel (uplink DPDCH) and the uplink Dedicated Physical Control Channel (uplink DPCCH).

The DPDCH and the DPCCH are I/Q code multiplexed within each radio frame (see [4]).

The uplink DPDCH is used to carry dedicated data generated at Layer 2 and above, i.e. the dedicated transport channel (DCH). There may be zero, one, or several uplink DPDCHs on each Layer 1 connection.

The uplink DPCCH is used to carry control information generated at Layer 1. The Layer 1 control information consists of known pilot bits to support channel estimation for coherent detection, transmit power-control (TPC) commands, feedback information (FBI), and an optional transport-format combination indicator (TFCI). The transport-format combination indicator informs the receiver about the instantaneous parameters of the different transport channels multiplexed on the uplink DPDCH, and corresponds to the data transmitted in the same frame. It is the UTRAN that determines if a TFCI should be transmitted, hence making it ~~is~~ mandatory for all UEs to support the use of TFCI in the uplink. There is one and only one uplink DPCCH on each Layer 1 connection.

Figure 1 shows the frame structure of the uplink dedicated physical channels. Each frame of length 10 ms is split into 15 slots, each of length T_{slot} = 2560 chips, corresponding to one power-control period. A super frame corresponds to 72 consecutive frames, i.e. the super-frame length is 720 ms.

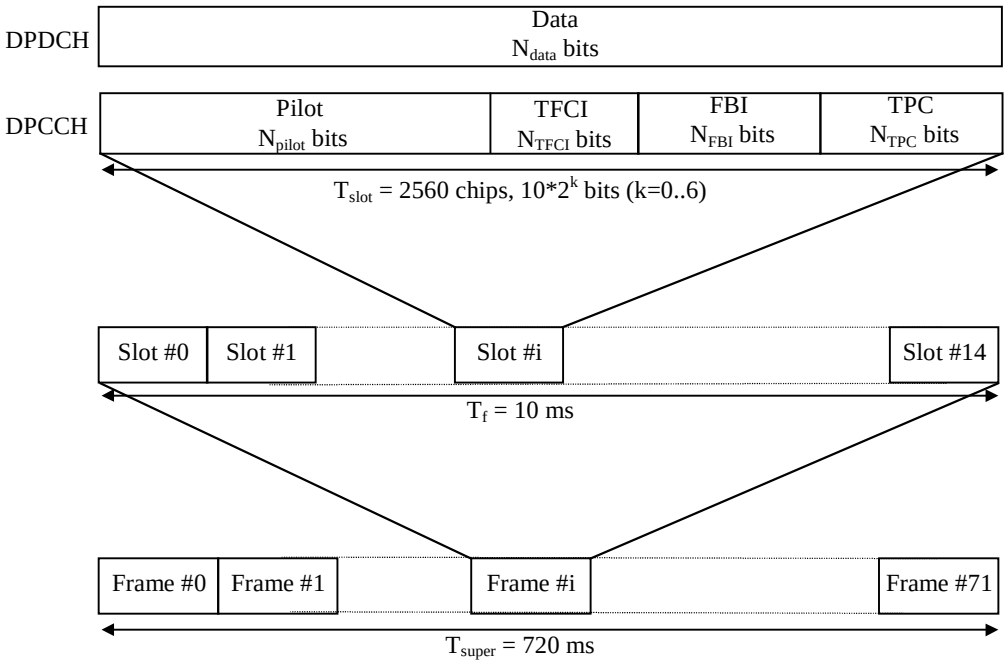


Figure 1: Frame structure for uplink DPDCH/DPCCH

The parameter k in figure 1 determines the number of bits per uplink DPDCH/DPCCH slot. It is related to the spreading factor SF of the physical channel as $SF = 256/2^k$. The DPDCH spreading factor may thus range from 256 down to 4. Note that an uplink DPDCH and uplink DPCCH on the same Layer 1 connection generally are of different rates, i.e. have different spreading factors and different values of k.

The exact number of bits of the different uplink DPCCH fields (N_{pilot}, N_{TFCI}, N_{FBI}, and N_{TPC}) is determined in table 2. The field order and total number of bits/slot are fixed, though the number of bits per field may vary during a connection.

The values for the number of bits per field are given in table 1 and table 2. The channel bit and symbol rates given in table 1 are the rates immediately before spreading. The pilot patterns are given in table 3 and table 4, the TPC bit pattern is given in table 5.

The N_{FBI} bits are used to support techniques requiring feedback between the UE and the UTRAN Access Point (=cell transceiver), including closed loop mode transmit diversity and site selection diversity (SSDT). The exact details of the FBI field are shown in figure 2 and described below.

5.3.2 Dedicated downlink physical channels

There is only one type of downlink dedicated physical channel, the Downlink Dedicated Physical Channel (downlink DPCH).

Within one downlink DPCH, dedicated data generated at Layer 2 and above, i.e. the dedicated transport channel (DCH), is transmitted in time-multiplex with control information generated at Layer 1 (known pilot bits, TPC commands, and an optional TFCI). The downlink DPCH can thus be seen as a time multiplex of a downlink DPDCH and a downlink DPCCH, compare section 5.2.1. It is the UTRAN that determines if a TFCI should be transmitted, hence making it is mandatory for all UEs to support the use of TFCI in the downlink.

Figure 10 shows the frame structure of the downlink DPCH. Each frame of length 10 ms is split into 15 slots, each of length T_{slot} = 2560 chips, corresponding to one power-control period. A super frame corresponds to 72 consecutive frames, i.e. the super-frame length is 720 ms.

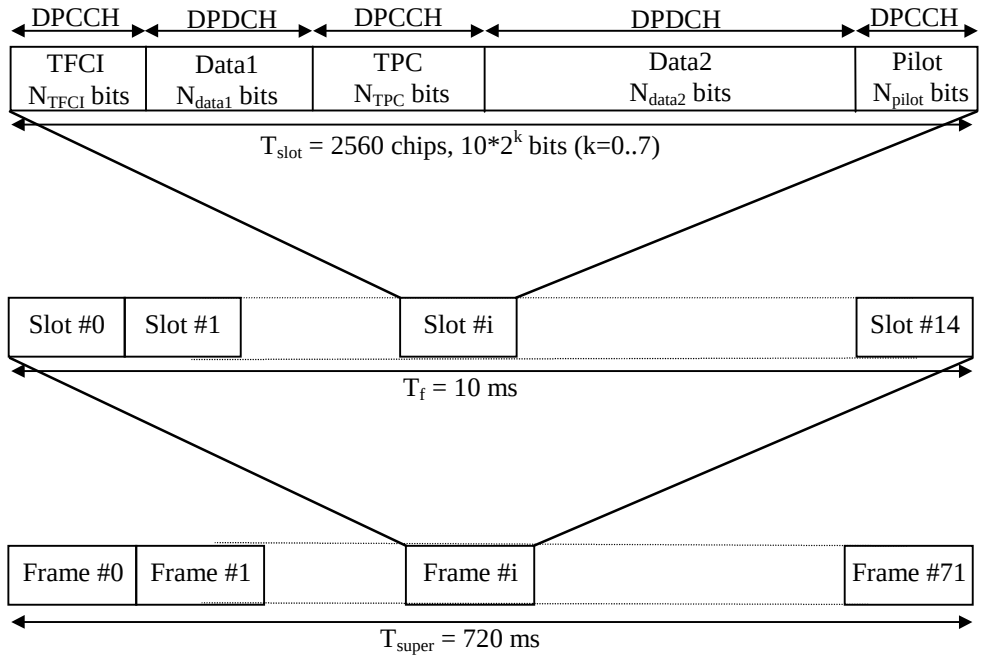


Figure 10: Frame structure for downlink DPCH

The parameter k in figure 10 determines the total number of bits per downlink DPCH slot. It is related to the spreading factor SF of the physical channel as SF = $512/2^k$. The spreading factor may thus range from 512 down to 4.

The exact number of bits of the different downlink DPCH fields (N_{pilot}, N_{TPC}, N_{TFCI}, N_{data1} and N_{data2}) is determined in table 11.The overhead due to the DPCCH transmission has to be negotiated at the connection set-up and can be re-negotiated during the communication, in order to match particular propagation conditions.

There are basically two types of downlink Dedicated Physical Channels; those that include TFCI (e.g. for several simultaneous services) and those that do not include TFCI(e.g. for fixed-rate services). These types are reflected by the duplicated rows of table 11. The channel bit and symbol rates given in table 11 are the rates immediately before spreading.

Table 11: DPDCH and DPCCH fields

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/Frame			Bits/ Slot	DPDCH Bits/Slot		DPCCH Bits/Slot		
				DPDCH	DPCCH	TOT		N_{Data1}	N_{Data2}	N_{TFCI}	N_{TPC}	N_{Pilot}
0	15	7.5	512	60	90	150	10	2	2	0	2	4
1	15	7.5	512	30	120	150	10	0	2	2	2	4
2	30	15	256	240	60	300	20	2	14	0	2	2
3	30	15	256	210	90	300	20	0	14	2	2	2
4	30	15	256	210	90	300	20	2	12	0	2	4
5	30	15	256	180	120	300	20	0	12	2	2	4
6	30	15	256	150	150	300	20	2	8	0	2	8
7	30	15	256	120	180	300	20	0	8	2	2	8
8	60	30	128	510	90	600	40	6	28	0	2	4
9	60	30	128	480	120	600	40	4	28	2	2	4
10	60	30	128	450	150	600	40	6	24	0	2	8
11	60	30	128	420	180	600	40	4	24	2	2	8
12	120	60	64	900	300	1200	80	4	56	8*	4	8
13	240	120	32	2100	300	2400	160	20	120	8*	4	8
14	480	240	16	4320	480	4800	320	48	240	8*	8	16
15	960	480	8	9120	480	9600	640	112	496	8*	8	16
16	1920	960	4	18720	480	19200	1280	240	1008	8*	8	16

* If TFCI bits are not used, then DTX shall be used in TFCI field.

The pilot symbol pattern is described in table 12. The shadowed part can be used as frame synchronization words. (The symbol pattern of the pilot symbols other than the frame synchronization word shall be "11".) In table 12, the transmission order is from left to right. (Each two-bit pair represents an I/Q pair of QPSK modulation.)

Table 12: Pilot Symbol Pattern

	N_{pilot} = 2	N_{pilot} = 4		N_{pilot} = 8				N_{pilot} = 16							
Symbol #	0	0	1	0	1	2	3	0	1	2	3	4	5	6	7
Slot #0	11	11	11	11	11	11	10	11	11	11	10	11	11	11	10
1	00	11	00	11	00	11	10	11	00	11	10	11	11	11	00
2	01	11	01	11	01	11	01	11	01	11	01	11	10	11	00
3	00	11	00	11	00	11	00	11	00	11	00	11	01	11	10
4	10	11	10	11	10	11	01	11	10	11	01	11	11	11	11
5	11	11	11	11	11	11	10	11	11	11	10	11	01	11	01
6	11	11	11	11	11	11	00	11	11	11	00	11	10	11	11
7	10	11	10	11	10	11	00	11	10	11	00	11	10	11	00
8	01	11	01	11	01	11	10	11	01	11	10	11	00	11	11
9	11	11	11	11	11	11	11	11	11	11	11	11	00	11	11
10	01	11	01	11	01	11	01	11	01	11	01	11	11	11	10
11	10	11	10	11	10	11	11	11	10	11	11	11	00	11	10
12	10	11	10	11	10	11	00	11	10	11	00	11	01	11	01
13	00	11	00	11	00	11	11	11	00	11	11	11	00	11	00
14	00	11	00	11	00	11	11	11	00	11	11	11	10	11	01

The relationship between the TPC symbol and the transmitter power control command is presented in table 13.

Table 13: TPC Bit Pattern

TPC Bit Pattern			Transmitter power control command
N_{TPC} = 2	N_{TPC} = 4	N_{TPC} = 8	
11	1111	11111111	1
00	0000	00000000	0

For slot formats using TFCI, the TFCI value in each radio frame corresponds to a certain combination of bit rates of the DCHs currently in use. This correspondence is (re-)negotiated at each DCH addition/removal. The mapping of the TFCI bits onto slots is described in [3].

5.3.3.1.2 Secondary Common Pilot Channel

A Secondary Common Pilot Channel the following characteristics:

- Can use an arbitrary channelization code of SF=256, see [4]
- Scrambled by either the primary or a secondary scrambling code, see [4]
- Zero, one, or several per cell
- May be transmitted over only a part of the cell
- A Secondary CPICH may be the reference for the Secondary CCPC~~C~~CH and the downlink DPCH. If this is the case, the UE is informed about this by higher-layer signalling.

5.3.3.2 Primary Common Control Physical Channel (P-CCPCH)

The Primary CCPCH is a fixed rate (30 kbps, SF=256) downlink physical channels used to carry the BCH.

Figure 15 shows the frame structure of the Primary CCPCH. The frame structure differs from the downlink DPCH in that no TPC commands, no TFCI and no pilot bits are transmitted. The Primary CCPCH is not transmitted during the first 256 chips of each slot. Instead, Primary SCH and Secondary SCH are transmitted during this period (see section 5.3.3.4).

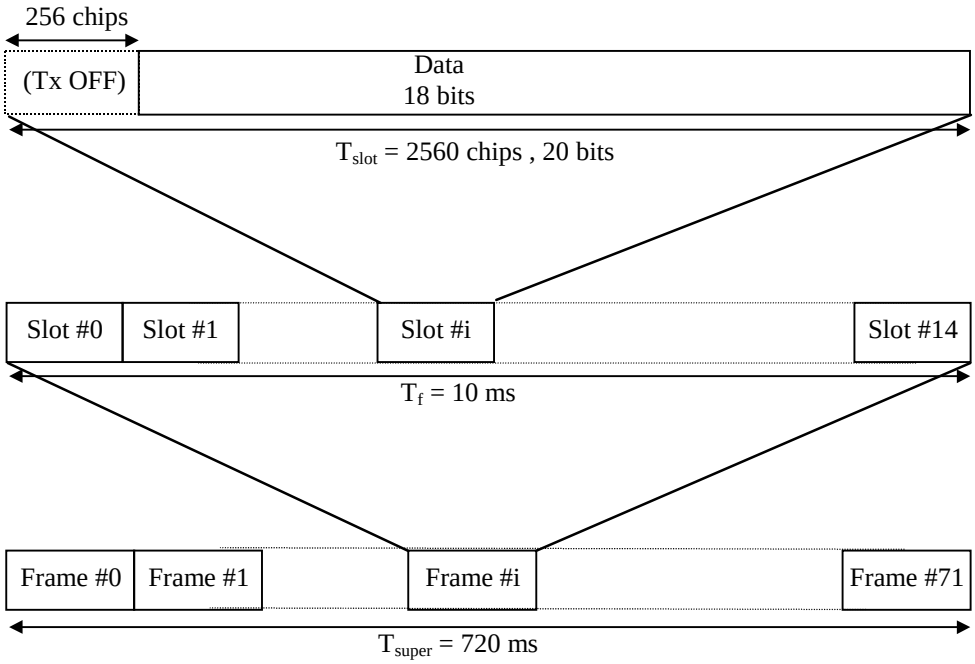


Figure 15: Frame structure for Primary Common Control Physical Channel

5.3.3.3 Secondary Common Control Physical Channel (S-CCPCH)

The Secondary CCPCH is used to carry the FACH and PCH. There are two types of Secondary CCPCH: those that include TFCI and those that do not include TFCI. It is the UTRAN that determines if a TFCI should be transmitted, hence making it mandatory for all UEs to support the use of TFCI. The set of possible rates is the same as for the downlink DPCH, see section 5.3.2. The frame structure of the Secondary CCPCH is shown in figure 17.

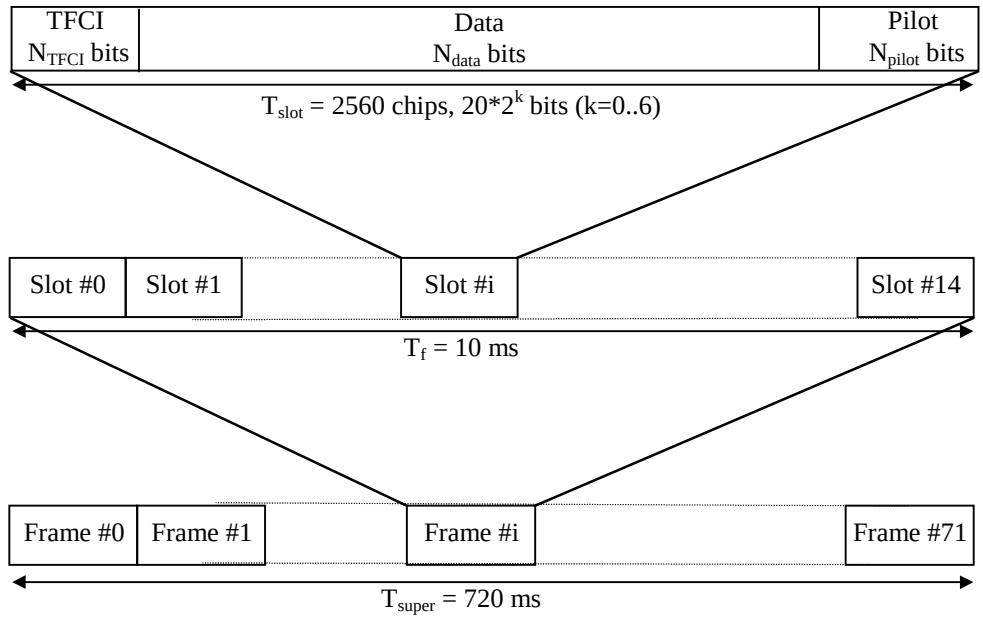


Figure 17: Frame structure for Secondary Common Control Physical Channel

The parameter k in figure 17 determines the total number of bits per downlink Secondary CCPCH slot. It is related to the spreading factor SF of the physical channel as SF = $256/2^k$. The spreading factor range is from 256 down to 4.

The values for the number of bits per field are given in table 16 ~~and table 17~~. The channel bit and symbol rates given in table 16 are the rates immediately before spreading. The pilot patterns are given in table 18.

The FACH and PCH can be mapped to the same or to separate Secondary CCPCHs. If FACH and PCH are mapped to the same Secondary CCPCH, they can be mapped to the same frame. The main difference between a CCPCH and a downlink dedicated physical channel is that a CCPCH is not inner-loop power controlled. The main difference between the Primary and Secondary CCPCH is that the Primary CCPCH has a fixed predefined rate while the Secondary CCPCH can support variable rate with the help of the TFCI field included. Furthermore, a Primary CCPCH is continuously transmitted over the entire cell while a Secondary CCPCH is only transmitted when there is data available and may be transmitted in a narrow lobe in the same way as a dedicated physical channel (only valid for a Secondary CCPCH carrying the FACH).

Table 16: Secondary CCPCH fields ~~with pilot bits~~

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{data}	N_{pilot}	N_{TFCI}
0	30	15	256	300	20	20	0	0
~~0~~1	30	15	256	300	20	12	8	0
3	30	15	256	300	20	18	0	2
~~4~~1	30	15	256	300	20	10	8	2
5	60	30	128	600	40	40	0	0
6~~2~~	60	30	128	600	40	32	8	0
7	60	30	128	600	40	38	0	2
8~~3~~	60	30	128	600	40	30	8	2
9	120	60	64	1200	80	72	0	8*
10~~4~~	120	60	64	1200	80	64	8	8*
11	240	120	32	2400	160	152	0	8*
12~~5~~	240	120	32	2400	160	144	8	8*
13	480	240	16	4800	320	312	0	8*
14~~6~~	480	240	16	4800	320	296	16	8*
15	960	480	8	9600	640	632	0	8*
16~~7~~	960	480	8	9600	640	616	16	8*
17	1920	960	4	19200	1280	1272	0	8*
18~~8~~	1920	960	4	19200	1280	1256	16	8*

* If TFCI bits are not used, then DTX shall be used in TFCI field.

~~Table 17: Secondary CCPCH fields without pilot bits~~

~~Slot Format #i~~	~~Channel Bit Rate (kbps)~~	~~Channel Symbol Rate (ksps)~~	~~SF~~	~~Bits/ Frame~~	~~Bits/ Slot~~	~~N_{data}~~	~~N_{pilot}~~	~~N_{TFCI}~~
~~0~~	~~30~~	~~15~~	~~256~~	~~300~~	~~20~~	~~20~~	~~0~~	~~0~~
~~1~~	~~30~~	~~15~~	~~256~~	~~300~~	~~20~~	~~18~~	~~0~~	~~2~~
~~2~~	~~60~~	~~30~~	~~128~~	~~600~~	~~40~~	~~40~~	~~0~~	~~0~~
~~3~~	~~60~~	~~30~~	~~128~~	~~600~~	~~40~~	~~38~~	~~0~~	~~2~~
~~4~~	~~120~~	~~60~~	~~64~~	~~1200~~	~~80~~	~~72~~	~~0~~	~~8*~~
~~5~~	~~240~~	~~120~~	~~32~~	~~2400~~	~~160~~	~~152~~	~~0~~	~~8*~~
~~6~~	~~480~~	~~240~~	~~16~~	~~4800~~	~~320~~	~~312~~	~~0~~	~~8*~~
~~7~~	~~960~~	~~480~~	~~8~~	~~9600~~	~~640~~	~~632~~	~~0~~	~~8*~~
~~8~~	~~1920~~	~~960~~	~~4~~	~~19200~~	~~1280~~	~~1272~~	~~0~~	~~8*~~

~~* If TFCI bits are not used, then DTX shall be used in TFCI field.~~

The pilot symbol pattern is described in table 18. The shadowed part can be used as frame synchronization words. (The symbol pattern of pilot symbols other than the frame synchronization word shall be “11”). In table 18, the transmission order is from left to right. (Each two-bit pair represents an I/Q pair of QPSK modulation.)

5.3.3.7 Page Indication Channel (PICH)

The Page Indicator Channel (PICH) is a fixed rate (SF=256) physical channel used to carry the Page Indicators (PI). The PICH is always associated with an S-CCPCH to which a PCH transport channel is mapped.

Figure 22 illustrates the frame structure of the PICH. One PICH frame of length 10 ms consists of 300 bits. Of these, 288 bits are used to carry Page Indicators. The remaining 12 bits are not used.

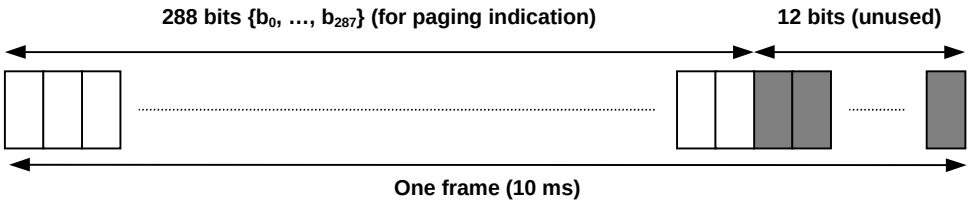


Figure 22: Structure of Page Indicator Channel (PICH)

N Page Indicators $\{PI_0, \ldots, PI_{N-1}\}$ are transmitted in each PICH frame, where N=18, 36, 72, or 144. The mapping from $\{PI_0, \ldots, PI_{N-1}\}$ to the PICH bits $\{b_0, \ldots, b_{287}\}$ are according to table 21.

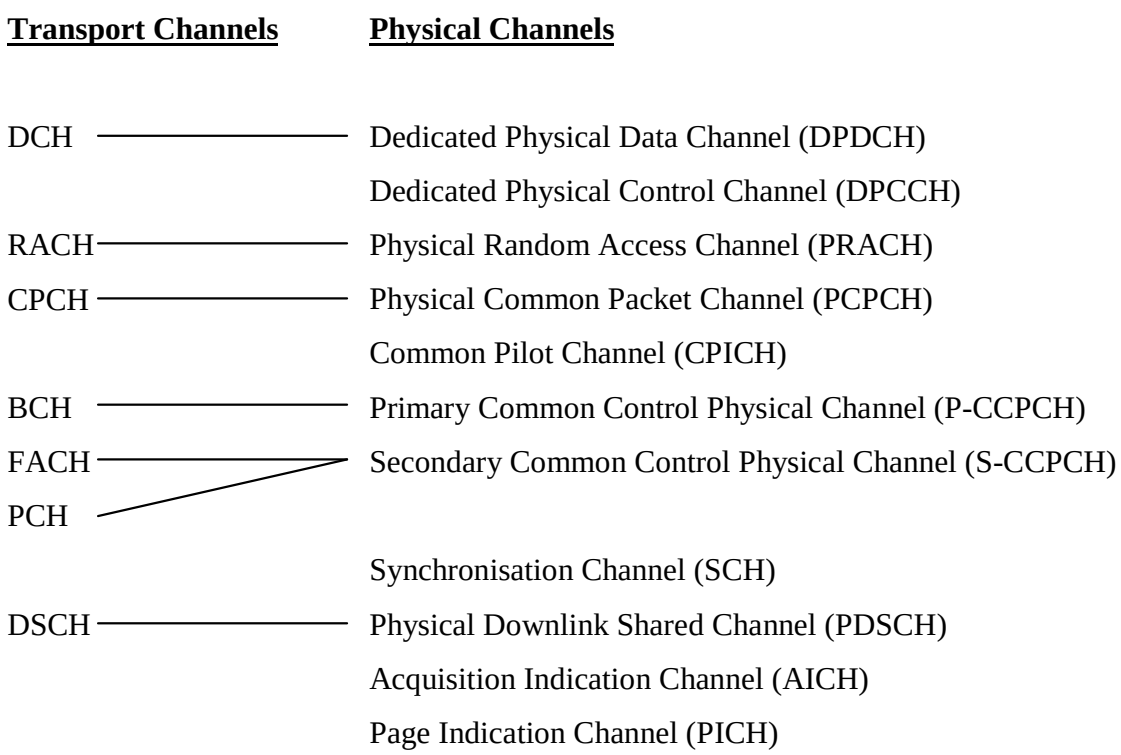
Table 21: Mapping of Page Indicators (PI) to PICH bits

Number of PI per frame (N)	$PI_i = 1$	$PI_i = 0$
N=18	$\{b_{16i}, \ldots, b_{16i+15}\} = \{1,1,\ldots,1\}$	$\{b_{16i}, \ldots, b_{16i+15}\} = \{0,0,\ldots,0\}$
N=36	$\{b_{8i}, \ldots, b_{8i+7}\} = \{1,1,\ldots,1\}$	$\{b_{8i}, \ldots, b_{8i+7}\} = \{0,0,\ldots,0\}$
N=72	$\{b_{4i}, \ldots, b_{4i+3}\} = \{1, 1,\ldots,1\}$	$\{b_{4i}, \ldots, b_{4i+3}\} = \{0, 0,\ldots,0\}$
N=144	$\{b_{2i}, b_{2i+1}\} = \{1,1\}$	$\{b_{2i}, b_{2i+1}\} = \{0,0\}$

If a Paging Indicator in a certain frame is set to "1" it is an indication that UEs associated with this Page Indicator should read the corresponding frame of the associated S-CCPCH.

6 Mapping of transport channels onto physical channels

Figure 23 summarises the mapping of transport channels onto physical channels.



~~Transport Channels~~	~~Physical Channels~~
~~BCH~~	~~Primary Common Control Physical Channel (P-CCPCH)~~
~~FACH~~ ~~PCH~~	~~Secondary Common Control Physical Channel (S-CCPCH)~~
~~RACH~~	~~Physical Random Access Channel (PRACH)~~
~~CPCH~~	~~Physical Common Packet Channel (PCPCH)~~
~~DCH~~	~~Dedicated Physical Data Channel (DPDCH)~~
	~~Dedicated Physical Control Channel (DPCCH)~~
	~~Synchronisation Channel (SCH)~~
~~DSCH~~	~~Physical Downlink Shared Channel (PDSCH)~~
	~~Page Indication Channel (PICH)~~
	~~Acquisition Indication Channel (AICH)~~

Figure 23: Transport-channel to physical-channel mapping

The DCHs are coded and multiplexed as described in [3] , and the resulting data stream is mapped sequentially (first-in-first-mapped) directly to the physical channel(s). The mapping of BCH and FACH/PCH is equally straightforward, where the data stream after coding and interleaving is mapped sequentially to the Primary and Secondary CCPCH respectively. Also for the RACH, the coded and interleaved bits are sequentially mapped to the physical channel, in this case the message part of the random access burst on the PRACH.

7.6.3 Uplink/downlink timing at UE

At the UE, the uplink DPCCH/DPDCH frame transmission takes place approximately T_0 chips after the reception of the first significant path of the corresponding downlink DPCCH/DPDCH frame. T_0 is a constant defined to be 1024 chips. More information about the uplink/downlink timing relation and meaning of T_0 can be found in [5]~~, section 4.5~~.

TSG-RAN Working Group 1 meeting #9 ***TSGR1#9(99)L29***
Dresden, Germany, Nov. 30 – Dec. 3, 1999

Agenda Item:
Source: **SK Telecom**
Title: **CR for TAB structure and timing relation for USTS in 25.211**
Document for: **Decision**

---

1. Introduction

The procedure for Uplink Synchronous Transmission Scheme (USTS) was accepted in text (in section 9 of TS25.214) at the last Kyongju meeting [1]. However it is required to elaborate the specification related to USTS. Therefore 'Time Alignment Bit (TAB)' structure for USTS should be included in section 5.3.2 of TS25.211 which is the section for downlink dedicated physical channel. Timing issue for USTS should be also included in section 7.6.3 of TS25.211 which is the section related to uplink/downlink DPCH timing at UE. This document have CR for change in TS25.211 for USTS.

2. References

[1] SK Telecom, "Uplink Synchronous Transmission Scheme," TSGR1#7 (99)e68

3GPP TSG RAN WG1 Meeting #9
Dresden, Germany, Nov 30 – Dec 3, 1999

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25.211	**CR**	016	Current Version:	3.0.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

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Proposed change affects: *(at least one should be marked with an X)* (U)SIM [ ] ME [X] UTRAN / Radio [X] Core Network [ ]

Source: SK Telecom **Date:** 1999-12-03

Subject: TAB structure and timing relation for USTS

Work item:

Category: *(only one category shall be marked with an X)*

F	Correction	
A	Corresponds to a correction in an earlier release	
B	Addition of feature	
C	Functional modification of feature	X
D	Editorial modification	

Release:

Phase 2	
Release 96	
Release 97	
Release 98	
Release 99	X
Release 00	

Reason for change: The additional descriptions are required to support the timing information for Initial synchronization and tracking of USTS.

Clauses affected: 5.3.2, 7.6.3

Other specs affected:

Other 3G core specifications	[ ]	→ List of CRs:
Other GSM core specifications	[ ]	→ List of CRs:
MS test specifications	[ ]	→ List of CRs:
BSS test specifications	[ ]	→ List of CRs:
O&M specifications	[ ]	→ List of CRs:

Other comments:

5.3.2 Dedicated downlink physical channels

There is only one type of downlink dedicated physical channel, the Downlink Dedicated Physical Channel (downlink DPCH).

Within one downlink DPCH, dedicated data generated at Layer 2 and above, i.e. the dedicated transport channel (DCH), is transmitted in time-multiplex with control information generated at Layer 1 (known pilot bits, TPC commands, and an optional TFCI). The downlink DPCH can thus be seen as a time multiplex of a downlink DPDCH and a downlink DPCCH, compare Section 5.2.1. It is the UTRAN that determines if a TFCI should be transmitted, hence making it is mandatory for all UEs to support the use of TFCI in the downlink. In case of USTS, the TPC bits in slot #14 in frames with CFN mod 2 = 0 are replaced by Time Alignment Bits (TABs) as described in section 9.3 of TS 25.214.

Figure 10 shows the frame structure of the downlink DPCH. Each frame of length 10 ms is split into 15 slots, each of length T_{slot} = 2560 chips, corresponding to one power-control period. A super frame corresponds to 72 consecutive frames, i.e. the super-frame length is 720 ms.

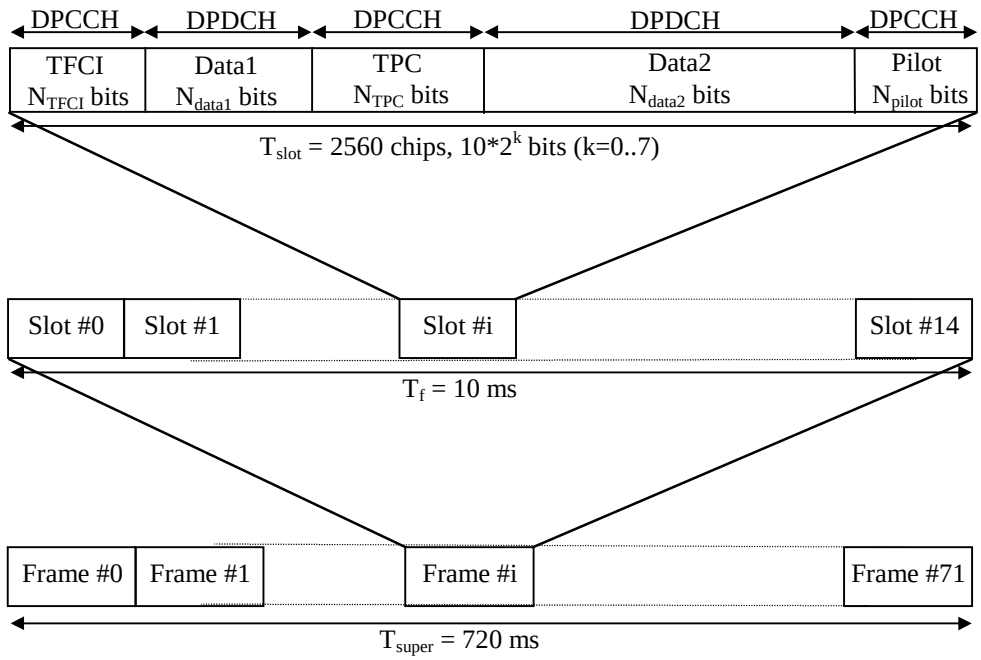

Figure 10: Frame structure for downlink DPCH

7.6.3 Uplink/downlink timing at UE

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TSG-RAN Working Group 1 meeting #9 ***TSGR1#9(99)L29***
Dresden, Germany, Nov. 30 – Dec. 3, 1999

Agenda Item:
Source: **SK Telecom**
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Document for: **Decision**

---

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Dresden, Germany, Nov 30 – Dec 3, 1999

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Proposed change affects: *(at least one should be marked with an X)* (U)SIM [ ] ME [X] UTRAN / Radio [X] Core Network [ ]

Source: SK Telecom **Date:** 1999-12-03

Subject: TAB structure and timing relation for USTS

Work item:

Category: *(only one category shall be marked with an X)*

F	Correction	
A	Corresponds to a correction in an earlier release	
B	Addition of feature	
C	Functional modification of feature	X
D	Editorial modification	

Release:

Phase 2	
Release 96	
Release 97	
Release 98	
Release 99	X
Release 00	

Reason for change: The additional descriptions are required to support the timing information for Initial synchronization and tracking of USTS.

Clauses affected: 5.3.2, 7.6.3

Other specs affected:

Other 3G core specifications	[ ]	→ List of CRs:
Other GSM core specifications	[ ]	→ List of CRs:
MS test specifications	[ ]	→ List of CRs:
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O&M specifications	[ ]	→ List of CRs:

Other comments:

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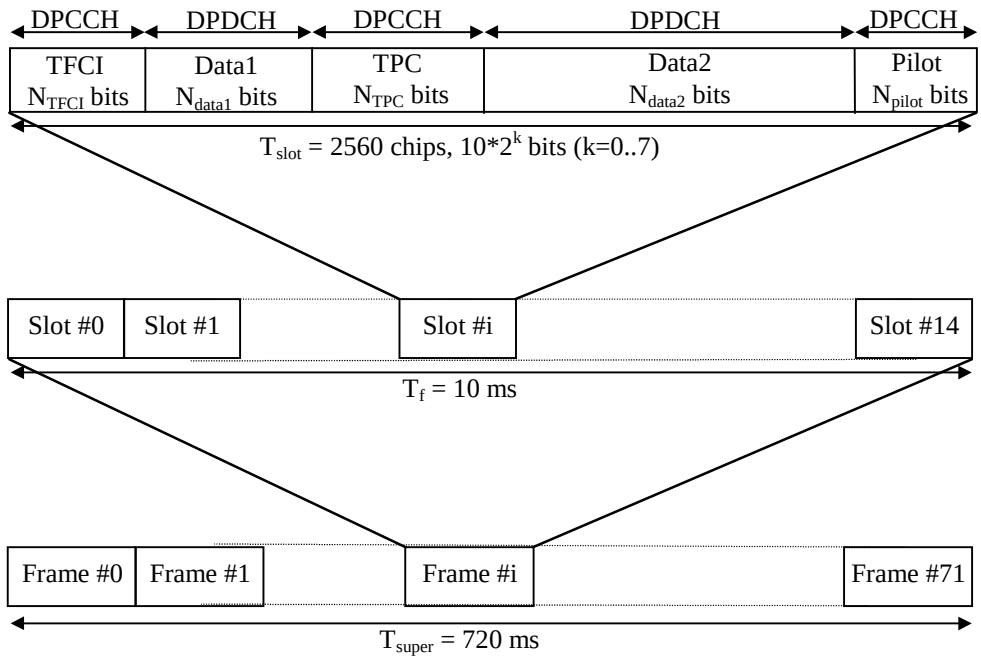

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At the UE, the uplink DPCCH/DPDCH frame transmission takes place approximately T_0 chips after the reception of the first significant path of the corresponding downlink DPCCH/DPDCH frame. T_0 is a constant defined to be 1024 chips. More information about the uplink/downlink timing relation and meaning of T_0 can be found in [5], section 4.5.

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3GPP TSG RAN WG1 ***TSGR1#9(99)k52***
November 30 – December 3, 1999, Dresden, Germany

Agenda item: **Ad hoc 14**

Source: **Philips**

Title: **Text Proposal for Timing for Initialisation Procedures**

Document for: **Decision**

Introduction

This paper is a revision of R1-99i17 following email and offline discussions.

The aim of the text proposal is to clarify the timing requirements for initialisation of DCHs and DSCHs, replacing the text currently found in section 7.1 of TS 25.214 with a new section 7.7 in TS 25.211.

3GPP TSG RAN WG1 Meeting #9
Dresden, Germany, 30 Nov – 3 Dec 1999

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GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

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Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc*

Proposed change affects: *(at least one should be marked with an X)*	(U)SIM		ME	X	UTRAN / Radio	X	Core Network	

Source:	Philips	**Date:**	1999-12-01

Subject: Timing for initialisation procedures

Work item:

Category: *(only one category shall be marked with an X)*

F	Correction	
A	Corresponds to a correction in an earlier release	
B	Addition of feature	
C	Functional modification of feature	X
D	Editorial modification	

Release:

Phase 2	
Release 96	
Release 97	
Release 98	
Release 99	X
Release 00	

Reason for change:
The current text in section 7 of TS25.214 describing rapid initialisation of DCHs is unclear and inconsistent with other parts of the specifications.
CR214-015rev1 has moved the power control information out of section 7 of TS25.214. The remaining information is timing information, which should be in TS25.211.
This CR creates a new section in TS25.211 for a clarified version of the timing information from section 7 of TS25.214.
There is also an editorial change to a cross-reference in section 7.6.3.

Clauses affected:
7 Timing relationship between physical channels (new section 7.7)
7.6.3 Uplink / downlink timing at UE

Other specs affected:

Other 3G core specifications	X	→ List of CRs:	CR25214-018rev1
Other GSM core specifications		→ List of CRs:	
MS test specifications		→ List of CRs:	
BSS test specifications		→ List of CRs:	
O&M specifications		→ List of CRs:	

Other comments:


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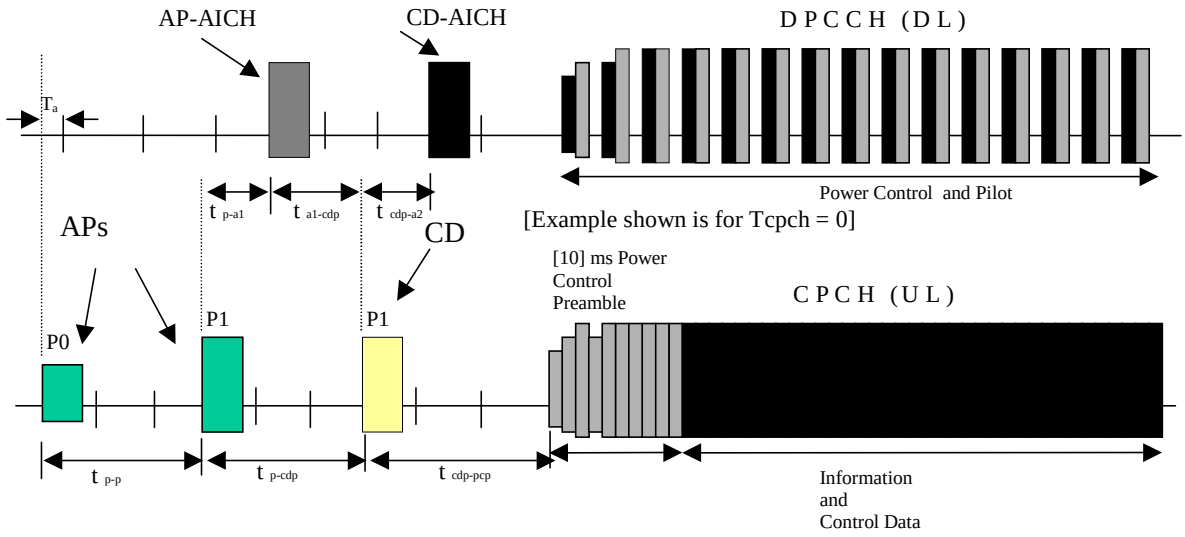

Figure 27: Timing of PCPCH and AICH transmission as seen by the UE, with T_{cpch}= 0

7.5 DPCH/PDSCH timing

The relative timing between a DPCH frame and the associated PDSCH frame is shown in figure 28.

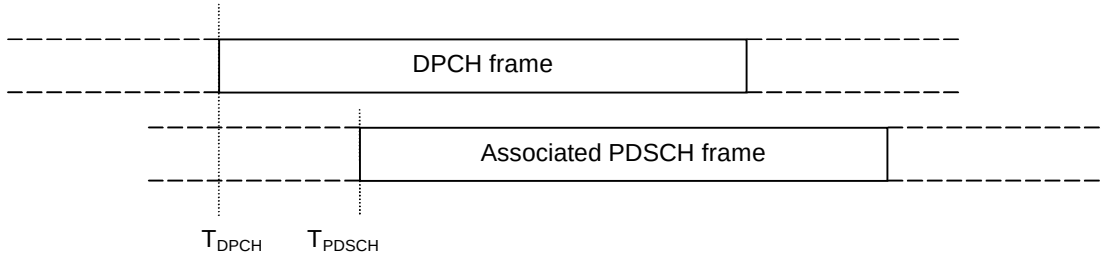

Figure 28: Timing relation between DPCH frame and associated PDSCH frame

The start of a DPCH frame is denoted T_{DPCH} and the start of the associated PDSCH frame is denoted T_{PDSCH}. Any DPCH frame is associated to one PDSCH frame through the relation -35840 chips < T_{DPCH} - T_{PDSCH} ≤ 2560 chips, i.e. the associated PDSCH frame starts anywhere between 1 slot before or up to 14 slots behind the DPCH.

7.6 DPCCH/DPDCH timing relations

7.6.1 Uplink

In uplink the DPCCH and all the DPDCHs transmitted from one UE have the same frame timing.

7.6.2 Downlink

In downlink, the DPCCH and all the DPDCHs carrying CCTrCHs of dedicated type to one UE have the same frame timing.

7.6.3 Uplink/downlink timing at UE

At the UE, the uplink DPCCH/DPDCH frame transmission takes place approximately T_0 chips after the reception of the first significant path of the corresponding downlink DPCCH/DPDCH frame. T_0 is a constant defined to be 1024 chips. More information about the uplink/downlink timing relation and meaning of T_0 can be found in [5], section 4.~~5~~3.

7.7 Timing relations for initialisation of channels

Figure 29 shows the timing relationships between the physical channels involved in the initialisation of a DCH.

The maximum time permitted for the UE to decode the relevant FACH frame before the first frame of the DPCCH is received shall be $T_{B\text{-}min}$ = 38400 chips (i.e.15 slots).

The downlink DPCCH shall commence at a time T_B after the end of the relevant FACH frame, where $T_B \geq T_{B\text{-}min}$ according to the following equation:

$$T_B = (T_n - T_k) \times 256 - N_{pcp} \times 2560 + N_{offset\_1} \times 38400 \text{ chips}$$, where:

N_{pcp} is a higher layer parameter set by the network, and represents the length (in slots) of the power control preamble (see [5], section 5.1.2.4).

N_{offset_1} is a parameter derived from the activation time set by higher layers. In order that $T_B \geq T_{B\text{-}min}$, N_{offset_1} shall be an integer number of frames such that:

$$N_{offset\_1} \geq \begin{cases} 1 \text{ when } T_n - T_k \geq \frac{T_{B-\min}}{256} + 10N_{pcp} - 150 \\ 2 \text{ when } \frac{T_{B-\min}}{256} + 10N_{pcp} - 300 \leq T_n - T_k < \frac{T_{B-\min}}{256} + 10N_{pcp} - 150 \\ 3 \text{ when } T_n - T_k < \frac{T_{B-\min}}{256} + 10N_{pcp} - 300 \end{cases}$$

T_n and T_k are parameters defining the timing of the frame boundaries on the DL DPCCH and S-CCPCH respectively (see section 7.1). These parameters are provided by higher layers.

The uplink DPCCH shall commence at a time T_C after the end of the relevant FACH frame, where

$T_C = T_B + T_0 + N_{offset\_2} \times 38400$ chips, where T_0 is as in section 7.6.3 and N_{offset_2} is a UE-specific higher-layer parameter which shall be an integer number of frames greater than or equal to zero.

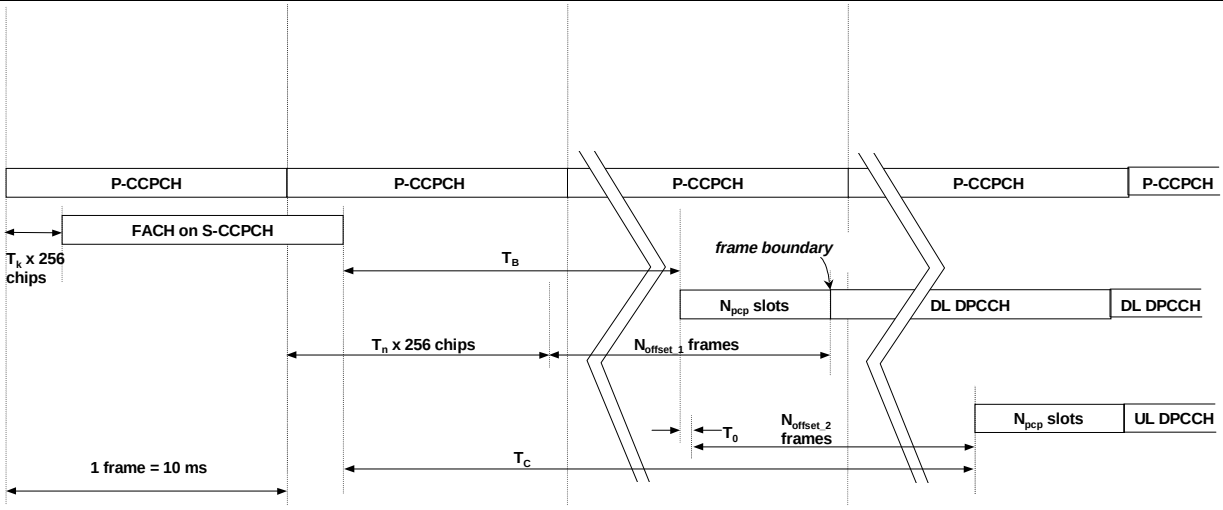

Figure 29: Timing for initialisation of DCH

The data channels shall not commence before the end of the power control preamble.

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Dresden, Germany, 30 Nov – 3 Dec 1999

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Proposed change affects: (U)SIM [ ] ME [X] UTRAN / Radio [X] Core Network [ ]
(at least one should be marked with an X)

Source: Philips **Date:** 1999-12-01

Subject: Timing for initialisation procedures

Work item:

Category: *(only one category shall be marked with an X)*

F	Correction		**Release:**	Phase 2	
A	Corresponds to a correction in an earlier release			Release 96	
B	Addition of feature			Release 97	
C	Functional modification of feature	X		Release 98	
D	Editorial modification			Release 99	X
				Release 00	

Reason for change:
The current text in section 7 of TS25.214 describing rapid initialisation of DCHs is unclear and inconsistent with other parts of the specifications.
CR214-015rev1 has moved the power control information out of section 7 of TS25.214.
CR211-017 has created a new section in TS25.211 for a clarified version of the remaining information from section 7.1 of TS25.214.
This CR therefore deletes section 7.1 of TS25.214.

Clauses affected: 7.1 Rapid initialisation of DCH for packet data transfer

Other specs affected:

Other 3G core specifications	X	→ List of CRs:	CR25211-017
Other GSM core specifications		→ List of CRs:	
MS test specifications		→ List of CRs:	
BSS test specifications		→ List of CRs:	
O&M specifications		→ List of CRs:	

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7 Procedures in Packet Data Transfer

7.1 Rapid Initialization of DCH for Packet Data Transfer

A rapid initialization procedure for establishing a DCH is defined to support bursting packet data transfer. The rapid initialization may be invoked for downlink packet data transfer on the DSCH or uplink packet data transfer on the DCH. The procedure may also be invoked to resume a recently discontinued DCH connection.

7.1.1 Rapid Initialization of DCH for Packet Data Transfer using DSCH

The synchronization of the DSCH/DCH pair may be expedited so that data transmission using DSCH can commence in slightly over 10 ms following the FACH burst assigning the TFCI using DCH. Figure 3shows the timing diagram of RACH/FACH to DCH/DCH+DSCH state transition. The parameter T_A specifies the RACH/FACH response time. The parameters T_B, T_C and T_D are referenced relative to the FACH frame. T_B specifies the time period when the downlink DPCCH is started. The parameter T_C specifies the period at which the UE will start the uplink DPCCH. Finally, T_D specifies the period that the DCH will be stable and the first frame of data may arrive. The parameters T_B, T_C, and T_D have the following relationship:

$$T_B < T_C << T_D$$

$$T_D = T_B + N_{slots}*0.666$$

where N_{slots} is a positive integer.

In order to initialise fast uplink link power control loop, searcher and channel estimator at the Node B, the UE will adhere to the following:

- The transmission of uplink link DPCCH will start at N_{slots} slots (1 to 15 slots) prior to the scheduled downlink packet data transmission using DSCH.
- The DPCCH will be transmitted with an additional negative power offset P_{offset} from the computed open loop estimate.
- The initial power control step size for transmitting the DPCCH will be set at P_{step} (typically: 2dB).
- The UE will revert back to the normal power control (PC) step size upon the receipt of the first down power control command during the uplink DPCCH transmission phase,
- The step size always goes back to its nominal setting in the beginning of DSCH transmission

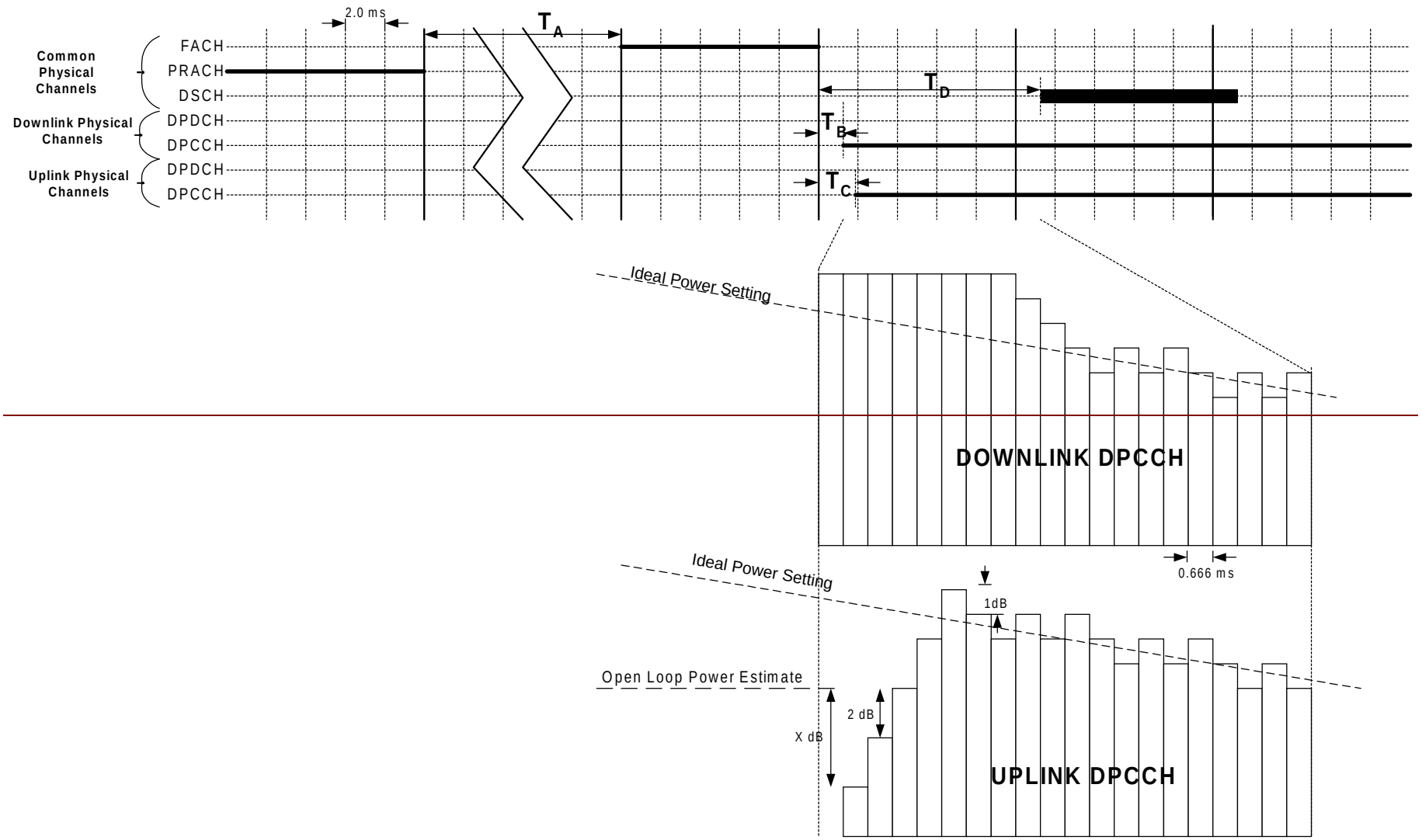
The parameters T_B, T_C, T_D, N_{slots}, P_{offset} and P_{step} may be negotiated with each individual UE or broadcast by the system so that the transition from RACH/FACH to DCH/DCH+DSCH sub-state is optimised.

7.1.2 Rapid Initialization of DCH for Uplink Packet Data Transfer

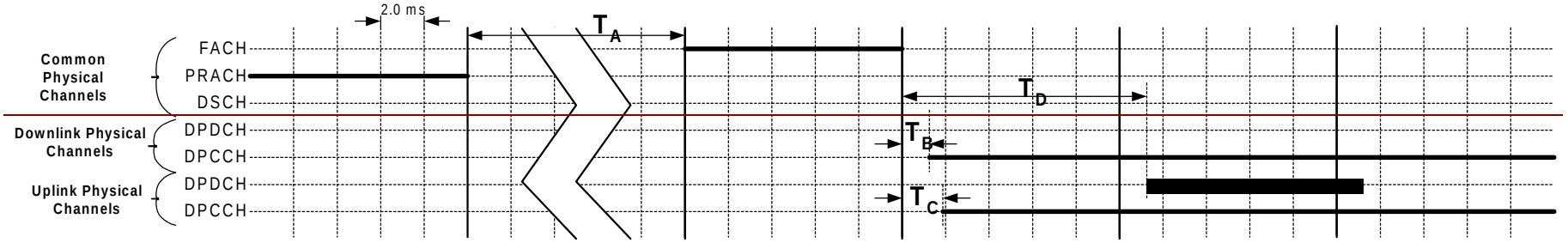
The synchronization of the DCH may also be expedited for the transfer of uplink packet data.. Figure 4 shows the same parameters T_B, T_C, and T_D applied to an uplink packet data transfer. The UE, upon detecting data in its queue, transmits a RACH with measurement report. After the UTRAN assigns the DCH via the FACH message, the downlink DPCCH is started after a time period T_B. The UE then begins transmission of the uplink DPCCH for reasons as outlined in section 7.3.4 at time period T_C. T_C is measured relative to the FACH transmit timing. Finally, the UE begins transmitting the data on the DPDCH after the period. The procedure for starting the uplink DPCCH transmission will be similar to Section 7.3.4.1

7.1.3 Resumption of DCH for Downlink or Uplink Packet Data Transfer

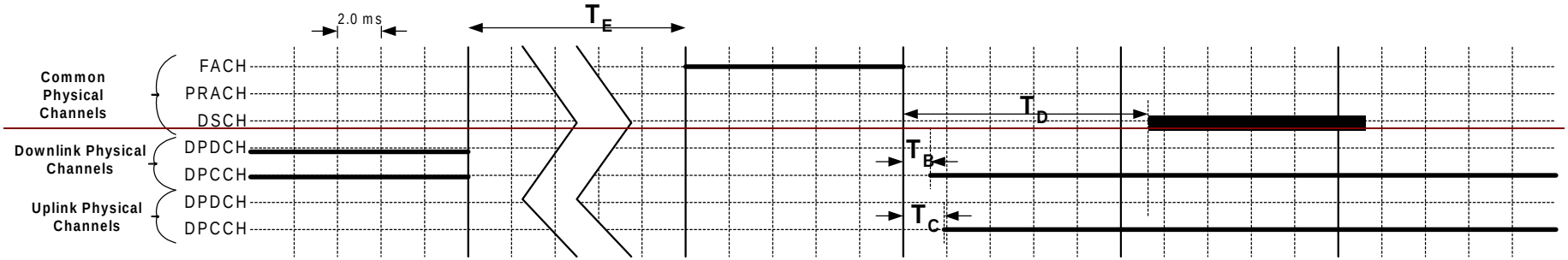
The synchronization of the DCH technique may be used to resume a DCH/DCH+DSCH connection that has been dropped for a short period.. This is applicable for packet data transfer using DSCH or uplink DPDCH or bi-directional data transfer using DSCH/Uplink DPDCH. Figure 5 shows the case where the DCH has been discontinued based on an inactivity timer T_E. The UTRAN, upon detecting data in the queue, may resume the DCH operation provided the period T_E has not elapsed. Typically T_E is set to 1000msec.



~~Figure 3: Rapid Initialization of DCH for packet data transfer over the DSCH~~



~~Figure 4: Rapid initialization of the DCH for transfer of uplink packet data~~



~~Figure 5: Resumption of the DCH for transmission of downlink packet data~~

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Document R1-99j05
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or for SMG, use the format P-99-xxx

CHANGE REQUEST

Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.

25.211	CR	022	Current Version:	3.0.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to:	TSG RAN #6	for approval	X	strategic		(for SMG use only)
list expected approval meeting # here ↑		for information		non-strategic		

Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc*

Proposed change affects: *(at least one should be marked with an X)* (U)SIM [ ] ME [X] UTRAN / Radio [X] Core Network [ ]

Source: NEC **Date:** 1999-11-30

Subject: Modification of the STTD encoding scheme on DL DPCH with SF 512

Work item:

Category: *(only one category shall be marked with an X)*

F	Correction	
A	Corresponds to a correction in an earlier release	
B	Addition of feature	
C	Functional modification of feature	X
D	Editorial modification	

Release:

Phase 2	
Release 96	
Release 97	
Release 98	
Release 99	X
Release 00	

Reason for change: To avoid STTD-encoding the TPC bits with bits from other fields.

Clauses affected: 5.3.2.1

Other specs affected:

Other 3G core specifications	X	→ List of CRs:	25.211-CR008
Other GSM core specifications		→ List of CRs:	
MS test specifications		→ List of CRs:	
BSS test specifications		→ List of CRs:	
O&M specifications		→ List of CRs:	

Other comments:

5.3.2.1 STTD for DPCH

The block diagrams shown in figure 7 and figure 8 are used to STTD encode the DPDCH, TPC and TFCI symbols. The pilot symbol pattern for the DPCH channel transmitted on the diversity antenna is given in table 14. In the SF=~~512~~256 DPCH, if there is only one dedicated pilot symbol, it is STTD encoded together with the last symbol (data or DTX) of the second data field (data2) of the slot. For the SF=512 DPCH ~~the last odd data symbol in every radio frame is~~, the first two bits in each slot, i.e. TPC bits, are not STTD encoded and the same ~~symbol is~~bits are transmitted with equal power from the two antennas. The following four bits are STTD encoded.

Table 14: Pilot pattern of the DPCH channel for the diversity antenna using STTD

	N_{pilot} = 2	N_{pilot} = 4		N_{pilot} = 8				N_{pilot} = 16							
Symbol #	0	0	1	0	1	2	3	0	1	2	3	4	5	6	7
Slot #0	01	01	10	11	00	00	10	11	00	00	10	11	00	00	10
1	10	10	10	11	00	00	01	11	00	00	01	11	10	00	10
2	11	11	10	11	11	00	00	11	11	00	00	11	10	00	11
3	10	10	10	11	10	00	01	11	10	00	01	11	00	00	00
4	00	00	10	11	11	00	11	11	11	00	11	11	01	00	10
5	01	01	10	11	00	00	10	11	00	00	10	11	11	00	00
6	01	01	10	11	10	00	10	11	10	00	10	11	01	00	11
7	00	00	10	11	10	00	11	11	10	00	11	11	10	00	11
8	11	11	10	11	00	00	00	11	00	00	00	11	01	00	01
9	01	01	10	11	01	00	10	11	01	00	10	11	01	00	01
10	11	11	10	11	11	00	00	11	11	00	00	11	00	00	10
11	00	00	10	11	01	00	11	11	01	00	11	11	00	00	01
12	00	00	10	11	10	00	11	11	10	00	11	11	11	00	00
13	10	10	10	11	01	00	01	11	01	00	01	11	10	00	01
14	10	10	10	11	01	00	01	11	01	00	01	11	11	00	11