TSG-RAN Working Group 4 (Radio) meeting #94-eR4-2002870

Electronic Meeting, February 24th – March 06th 2020

**Source:** Ericsson

**Title:** TP to TR 38.820: Phase noise trends and example parameterized phase noise model in subclause 5.5.3 and Annex B

**Agenda item:** 10.3.6

**Document for:** Approval

# Introduction

In previous RAN4 meetings, the technical background for phase noise characteristics for a complete frequency generation sub-system taking to account and example parameterized phase noise models for different example frequencies were discussed [1, 2].

In this contribution, it is proposed to add the background information around phase noise trends considering PLL and VCO contributions in a new Annex B and example parameterized model for phase noise characteristics in TR 38.820. This text proposal is an improved version of the text proposals presented in [1, 2].

This is a revised version of R4-2001018.

# Discussion

In previous RAN4 meeting, in-depth analysis over phase noise characteristics for 7-24 GHz example frequencies was presented [1,2]. The analysis was based on data published covering PLLs as well as crystal oscillators and the presented characteristics consider the influence from both. The phase noise characteristics of the complete frequency generation system including PLL, crystal oscillator, and loop filter is essential for the base station performance.

In [2], based on the phase noise characteristics and trends presented in [1], examples for parameterized phase noise model for 10 GHz, 15 GHz and 20 GHz example frequencies was presented.

The intention with this paper is to propose text to capture the background analysis and example parameterized phase noise models for 7-24 GHz example frequencies in the technical report.

Summary of change:

1. In subclause 5.5.3.1, technical background information on how to model phase noise for example frequencies is created.
2. In Annex B, technical background information relevant for the frequency generation sub-system is created.

Additional changes in revision:

1. Compress the text and focus on the collection of published phase noise characteristics for PLL, XO and noise floor.
2. Removed subclause 5.5.3.1.
3. Added a reference to Annex B in subclause 5.5.3.

# Conclusion

It is proposed that the attached text proposal is included in TR 38.820 [3]. The intension with the text proposal is to give an example on phase noise characteristics for a compete frequency generation sub-system and show an example on how to model phase noise characteristics for different example frequencies.

# References

[1] R4-1906185, “Further elaboration on 7-24 GHz phase noise for different example frequencies”, Ericsson

[2] R4-1911831, “Parameterized phase noise model for example frequencies in 7-24 GHz”, Ericsson

[3] R4-1916102, “Draft TR 38.820, v0.4.0”, Huawei

TEXT PROPOSAL:

### 5.5.3 Phase noise

Sufficiently low phase noise at the measurement interface is required to avoid excessive EVM. Based on the available data [35 - 40], a descriptive phase noise profile is shown in figure 5.5.3-1. It shows performance of the current PLLs (i.e. as of 2019) for base stations operating in 7 – 24 GHz range. In the figure each colour matches to a single component. It should be noted that throughout this section phase noise is referred to the observed level at a measurement interface. Noise levels internal to PLL and clock distribution network may differ from this and implementation freedom is not limited.

For specific use cases where high data rates are targeted, the performance can be better as shown by the examples of component data. On the other hand, in cases where device size, power consumption and low cost are the highest priorities, the phase noise performance may be worse.

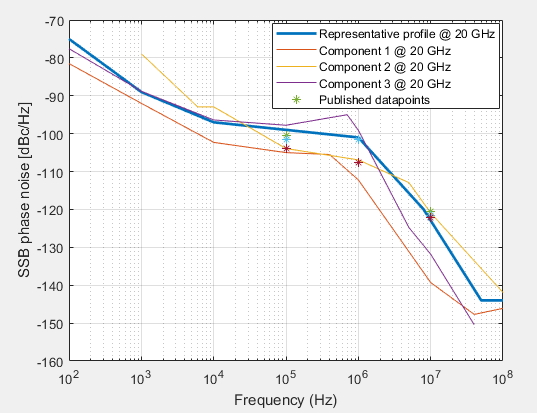


Figure 5.5.3-1: A representative phase noise profile for 7 – 24 GHz base stations

In figure 5.5.3-1 the phase noise profile is shown at 20 GHz example frequency. To adjust the model to a different frequency, the levels need to be scaled according to Leeson’s equation, i.e. halving the frequency reduces the noise power to one quarter of the original. When the profile is given at center frequency f0 and a given noise power P0, the correct noise power P at frequency f equals:

P = P0 \* 20 \* log10(f/f0)

In this example, P and P0 describe the full single side-band noise profile for which the unit is dBc/Hz.

More published phase noise characteristics can be found in Annex B.

TEXT PROPOSAL:

Annex B (informative):  
Phase noise characteristics

# B.1 Phase noise

Low phase noise is essential for low EVM enabling higher order modulation support as well as for low impact from receiver blockers due to reciprocal mixing between blocker signal and phase noise. At the same there are limits on attainable levels of phase noise for a given DC power budget and the carrier frequency being considered. The Phase Locked Loop (PLL) used to generate the LO signal has a voltage (or digitally) controlled oscillator, here referred to VCO. The VCO dominates power consumption and phase noise of the PLL and dimensioning for the remaining parts of the PLL.

The scaling of semiconductor technology has resulted in increased speed and reduced power consumption of digital circuits, leading to competitive digital PLL architectures. Also, analog PLLs architectures have seen advancements with technology, like sub-sampling PLLs. Today both analog and digital PLLs are viable choices to achieve state-of-the-art performance. Regardless of architecture the PLL phase noise characteristic will have a similar profile, facilitating the modelling. At low offset frequencies the phase noise will be dominated by that of the reference, as the PLL will multiply its frequency and track slow phase variations. The phase noise in that region will equal that of the reference plus 20.log() dB, where N is the frequency multiplication factor of the PLL. For a certain PLL output frequency , will be inversely proportional to the reference frequency (). A high reference frequency is thus beneficial as it reduces and consequently reference phase noise contribution. At higher offset frequencies the PLL will dominate the phase noise. The region below the PLL bandwidth, which can be chosen differently but is often of the order of 1 MHz in high performance PLLs for this frequency range, is called the in-band noise. The in-band noise will be due to noise of different building blocks in the PLL and will typically have a -10 dB/decade slope at lower offset frequencies due to flicker noise (1/f noise), and a zero slope at higher offsets due to thermal noise. Above the PLL bandwidth, the out-of-band noise is dominated by oscillator phase noise, typically thermal noise with a slope of -20 dB/decade. At very high offset frequencies the PLL phase noise reaches a floor with zero slope, but typically buffers or frequency dividers outside the PLL itself will dominate this floor in a transceiver. Figure B.1-1 shows the PLL phase noise profile and its regions.

Phase Noise (dBc/Hz)

Log frequency

Reference noise

In-band flicker noise

In-band thermal noise

Oscillator noise

Noise floor

PLL BW

**Figure B.1-1: PLL phase noise profile and regions**

With a bandwidth typically of the order of about 1 MHz, at 10 MHz offset the oscillator phase noise will dominate in most PLLs. Since the oscillator phase noise is well studied and there are fundamental relations derived this is a good starting point. At 10MHz offset the oscillator will likely be dominated by thermal noise, modelled in the classic paper by Leeson in 1966:

(Eq. B.1-1)

Where is the phase noise, the offset frequency, the noise factor, equal to 1 in an ideal oscillator, is Boltzmann’s constant equal to 1.38065∙10-23 J/K, is the temperature equal to 293 K in room temperature, is the power dissipation in the resonator, *f0* the oscillation frequency, and  is the resonator quality factor.

## B.1.1 Performance of PLLs

To find state-of-the-art, published papers on fractional-N PLLs published in leading IEEE conferences and journals since 2015 have been investigated. To support high level of integration circuits in CMOS technologies were selected, with a power consumption below 50 mW. To establish a level for state-of-the-art phase noise performance, circuits with a focus on phase noise is preferable, and thus papers with a jitter figure of merit equal to -230 dB and below was selected. The reference frequency should be less than 500 MHz. Since different transceiver frequency plans can be used, not only PLLs in the range of 7-24 GHz are part of the investigation, but also up to the 60 GHz band and frequencies down to 5 GHz. An extended frequency range also helps identifying performance trends with respect to frequency. Publications with less than 10% frequency tuning range were also excluded, to avoid circuits where the tuning range is very small to achieve the best possible phase noise, which would give the wrong picture of achievable phase noise in practice.

Below is a summary of the performance of the published fractional-N PLLs where Figure B.1.1-1 describes the power consumption over frequency. Figure B.1.1-2 represents the phase noise at 100 kHz offset over frequency while Figure B.1.1-3 and Figure B.1.1-4 represent the phase noise at 1 MHz and 10 MHz offset respectively.



**Figure B1.1-1: Power consumption versus upper operating frequency**

As can be seen in figure B.1.1-1 it is a clear trend that the power consumption increases with PLL output frequency.



**Figure B.1.1-2: Phase noise at 100kHz offset versus upper operating frequency**



**Figure B.1.1-3:** **Phase noise at 1MHz offset versus upper operating frequency**



**Figure B.1.1-4: Phase noise at 10MHz offset versus upper operating frequency**

In Figures B.1.1-2 to B.1.1-4 which are representing the phase noise at 100 kHz, 1 MHz and 10 MHz offset, respectively, versus output frequency, a curve is also shown with a slope of 20 dB per decade, corresponding to equal phase noise performance.

## B.1.2 State-of-the-art crystal oscillators

The PLLs above use reference frequencies of 40 MHz and above. Since the problem of reference noise increases at lower reference frequencies, due to an increased effective frequency multiplication factor, to be conservative the investigation was focused on low power crystal oscillators at about 40 MHz. There are not as many publications on crystal oscillator circuits as on PLLs, but the few papers from recent years in IEEE Journal of Solid-State Circuits was used to represent state-of-the-art in CMOS low power crystal oscillators at about 40 MHz. To span the design space, also the 491.25 MHz crystal oscillator is included in the table B.1.2-1 summarizing the crystal oscillator performance.

**Table** **B.1.2-1: Crystal oscillator performance**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Frequency (MHz)** | **491.25** | **39.25** | **48** | **39.25** |
| Core power (uW) | 840 | 181 | 1500 | 19 |
| Process (nm) | 28 | 180 | 28 | 65 |
| PN @ 1kHz (dBc/Hz) | -107 | -147 | -114 | -139 |
| PN @ 10 kHz (dBc/Hz) | -130 | -161 | -148 | -153 |
| PN @100 kHz (dBc/Hz) | -140 | -172 | -156 | -153 |
| PN @ 1MHz (dBc/Hz) | -148 | -175 | -158 | -153 |
| 20GHz PN @ 1kHz (dBc/Hz) | -75 | -93 | -62 | -85 |
| 20GHz PN @ 10 kHz (dBc/Hz) | -98 | -107 | -96 | -99 |
| 20GHz PN @100 kHz (dBc/Hz) | -108 | -118 | -104 | -99 |
| 20GHz PN @ 1MHz (dBc/Hz) | -116 | -121 | -106 | -99 |
| FoM (dBc/Hz) | -227 | -246 | -220 | -248 |

To translate the phase noise into equivalent phase noise at a PLL output, an amount equal to dB should be added. For a 20 GHz PLL with a 39.25 MHz reference, the amount to add is thus 54 dB, and with 48 MHz reference it is 52 dB, and with 491 MHz it is 32 dB. This has been done in the fields starting with 20 GHz in table B.1.2-1, where the phase noise of the different crystal oscillators can be compared directly in terms of their impact on a 20 GHz PLL output signal.

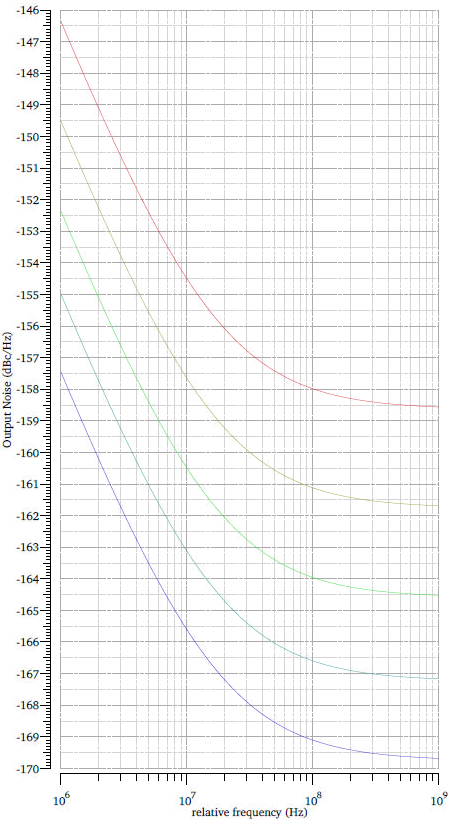
At 1 MHz offset the line in figure B.1.1-3 indicates that the phase noise of state-of-the-art PLLs is -102 dBc/Hz. This is close to the bandwidth of the PLL and it can thus be assumed that the reference noise is transferred to the PLL output without significant filter attenuation. The 20 GHz PN @ 1 MHz of the crystal oscillator should thus be well below -102 dBc/Hz not to affect the PLL performance.

At 100kHz offset figure B.1.1-2 indicates -95 dBc/Hz for a 20 GHz PLL, and all the crystal oscillators in the table B.1.2-1meet that. Below 100 kHz offset we assume that the PLL noise increases by 10 dB per decade due to in-band 1/f noise. At 10 kHz offset a 20 GHz PLL will then have -85 dBc/Hz phase noise, and all crystal oscillators are far below that. Assuming the crystal oscillators to have a -30 dB per decade slope at low offset frequencies due to 1/f noise, the frequency where the PLL and the crystal oscillator will have equal noise contribution can be calculated to be 1 kHz, 0.13 kHz, 4.5 kHz, and 0.32 kHz.

Given the above we assume that the crystal oscillator can be made non-dominant above 1 kHz offset frequency, and that the PLL output phase noise will have a slope of -30 dB/decade below that frequency. This is achievable with reference frequencies ranging from 40 MHz to 491 MHz, and power consumptions below 1 mW, using CMOS technologies as different as 28 nm and 180 nm.

## B.1.3 Noise floor

When it comes to the noise floor it is difficult to find published works that include measurements in this region. Circuit simulations have therefore been performed to find realistic levels of the noise floor. The noise floor is typically set not by the oscillator of the PLL, but by buffers and LO distribution. For this reason, the phase noise of a chain of inverters acting as buffers was simulated. Three equal sized cascaded inverters were used for each of the two differential signal halves, where minimum length devices in a 22 nm technology were used. The input signal was 1 V peak differential at 20 GHz, and different width of devices were investigated, corresponding to different amounts of power consumption. The phase noise is shown in figure B.1.3-1, where the lowest noise floor of close to -170 dBc/Hz was achieved with a 13.4 mW power consumption, the second-best curve was for 7.5 mW, the next was 4.2 mW, then 2.4 mW, and finally 1.3 mW. As can be seen -165 dBc/Hz can be reached at about 5 mW buffer power consumption. Taking attenuation in the LO distribution network into account, it is reasonable to add 10 dB to this level, making the low power achievable noise floor -155 dBc/Hz for a 20 GHz carrier.



**Figure B.1.3-1: Phase noise of simulated differential LO buffers in 22 nm technology, ranging from 1.3 mW to 13.4 mW power consumption**

# B.2 Example phase noise characteristics

The proposal is to use the trend curves in figure B.1.1-2 to B.1.1-4 as a starting point to define example phase noise performance. The levels for these curves at 20 GHz example frequency are -95 dBc/Hz, -102dBc/Hz, and -120 dBc/Hz, at 100 kHz, 1 MHz, and 10 MHz, respectively.

As can be seen, there are PLLs at different frequencies with this performance, and using both 28 nm and 65 nm technology, and different reference frequencies from 40 to 491 MHz, making it suitable as basis for the analysis.

Thus, using the above, a phase noise profile valid at other offset frequencies can be constructed. We then also include crystal oscillator phase noise and the noise floor. Below 1 kHz offset the crystal oscillator phase noise is dominant, with a slope of -30 dB/decade, and above 560 MHz the noise is at the -155 dBc/Hz floor.



**Figure B.2-1: State-of-the-art phase noise vs. offset from a 20 GHz example frequency**

Figure B.2-1 shows the phase noise versus offset from a 20 GHz carrier. When operating at other example frequencies an offset of 20log(*f*/20 GHz) is to be added. For instance, operating at 10 GHz 6 dB should be subtracted from the above curve, i.e. the entire curve is shifted down by 6 dB at all frequency offsets.

In addition, considering PVT (semi-conductor Process, Voltage and Temperature) variations, we propose to add a 10 dB margin to the state-of-the-art published performance. The resulting model for different example frequencies is shown in Figure B.2-2.



**Figure B.2-2: PLL phase noise characteristics for 10 GHz, 15 GHz, 20 GHz and 30 GHz (bottom to top)**

The analysis in this paper should be considered when in future WI, specific bands are specified within 7-24 GHz ranges where selection of numerology as well as signal quality requirements and the need for PT-RS and CPE compensation is concerned.

It should be noted that the example phase noise characteristics presented in Figure B.3-2 show quite similar performance compared to phase noise characteristics presented in Figure 5.5.3-1 in sub-clause 5.3.3 except for performance low frequency offsets. The difference at lower frequency offsets depends on inclusion of crystal oscillator phase noise into phase noise characteristics presented in this sub-clause and annex B.

To better adapt the model to calculations, an equation was fitted to the corresponding curves. The equation of the form below was used, using poles and zeros

(Eq. B.2-1)

Where *S* is the single sideband phase noise power spectral density, *fo* the offset frequency, *fz,1 .. fz,N*the zeros, *fp,1 .. fp,M*the poles, α*z,1 .. αz,N*the order of the zeros, and α*p,1 .. αp,M* the orders of the poles. To fit the equation to the curves in Figure B.2-2 the following parameters were used:

**Table B.2-1 Parameters of phase noise model equation**

|  |  |  |  |
| --- | --- | --- | --- |
| **Parameter** | **Value/expression** | **Parameter** | **Value** |
| *PSD0* |  |  |  |
| *fz,1* | 1000 | *αz,1* | 2 |
| *fz,2* | 500e3 | *αz,2* | 1 |
| *fz,3* | 560e6 | *αz,3* | 2 |
| *fp,1* | 1 | *αp,1* | 3 |
| *fp,2* | 1.26e3 | *αp,2* | 2 |

As can be seen the parameter PSD0 depends on the carrier frequency, whereas the other parameters are carrier frequency independent. At 20GHz PSD0 will be equal to 225, or 23.5dB. To compare the result of equation (Eq. B.2-1) to curves, *S* must be converted to a logarithmic scale:

dBc/Hz (Eq. B.2-2)

The comparison can be seen in Figure B.2-3 clearly demonstrating a good fit. Consequently, equation (Eq. B.2-1), together with the parameters in Table B.2-1, can be used to represent phase noise model examples.



**Figure B.2-3 Example phase noise model for 10GHz, 15GHz, 20GHz, and 30GHz together with the piece-wise linear model.**

The performance trends presented in Annex B, does not preclude other phase noise performance characteristics.