

Source: Motorola
Title: CPICH cancellation complexity
Agenda item: 9.1
Document for: Discussion

1.0 Introduction

A number of contributions [1]-[5] to 3GPP have pointed out the benefits of CPICH cancellation at the UE. Intel Corp. has presented a complexity analysis for such a hardware implementation [6]. Because any capacity improvement must be evaluated in regard to the increase in complexity to the UE, Motorola would like to add to the information regarding this issue.

2.0 Complexity basis

Complexity may be addressed in terms of an increase in hardware gate-count and/or an increase in DSP MIPS. Motorola has chosen to address the complexity increase in terms of a gate-count. Note that there are number of factors that affect such an estimate, including the number of branches (fingers) supported, the number of simultaneous channels (codes) supported, the number of CPICH signals cancelled, and the number of interference terms cancelled. Furthermore, the hardware design techniques and simplifications that are employed, including the amount of resource sharing that is used, will also impact the resulting gate-count estimates and may cause differences in the estimates presented by various companies. Nevertheless, "order-of-magnitude" estimates that are based on a reasonable set of assumptions are useful in assessing the performance/complexity trade-offs of implementing CPICH cancellation within the UE.

2.1 Complexity Increase

Using the model shown in Figure 1 (as presented by Intel), Motorola agrees with Intel that this is implementable in less than 100,000 gates. In addition, with proper resource sharing and other relatively straightforward design simplifications, Motorola believes the gate-count may be reduced even further.

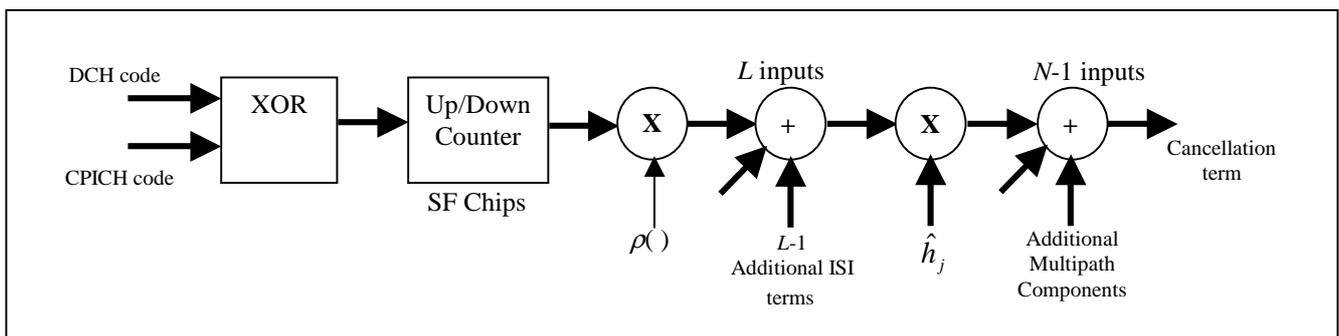


Figure 1. Generation of CPICH interference cancellation terms for one radio finger. L is the number of inter-symbol interference (ISI) terms cancelled (summation length), and N is the number of multipath rays. The XOR and up/down counter perform the cross-correlation between CPICH and DCH spreading codes, denoted as $R(\cdot)$, and $\rho(\cdot)$ is the convolution of the Tx and Rx filters. The implementation represents the computation of

$$\sum_{\substack{j=0 \\ j \neq i}}^{N-1} \hat{h}_j \cdot \sum_{l=-(L-1)/2}^{(L-1)/2} R(\Delta_{i,j} + l, n) \rho(l \cdot OS - \Omega_{i,j}).$$

See [1] for further discussion on the mathematics of CPICH cancellation.

3.0 Conclusion

A hardware complexity analysis by Motorola suggests that the complexity increase due to implementation of CPICH cancellation circuitry is less than 100,000 gates. This is in agreement with results presented by Intel. Motorola believes that such complexity numbers should be used by RAN4 to decide upon the requirement for CPICH cancellation given the capacity gains provided by this technique.

4.0 Reference

- [1] 3GPP TSGR1-00-1371, "CPICH interference cancellation as a means for increasing DL capacity," Intel Corporation, Nov. 2000.
- [2] 3GPP TSGR1-00-0030, "Further Results on CPICH Interference Cancellation as A Means for Increasing DL Capacity," Intel Corporation, Jan. 2001.
- [3] 3GPP TSGR4-01-0238, "CPICH Interference Cancellation as a Means for Increasing DL Capacity," Intel Corporation, Feb. 2001.
- [4] 3GPP TSGRP-01-077, "Mitigating the Effect of CPICH Interference at the UE," Intel Corporation," Mar. 2001.
- [5] 3GPP TSGR4-01-0967, "CPICH cancellation," Motorola, July 2001.
- [6] 3GPP TSGR4-01-0650, "On the Implementation Complexity of CPICH Interference Cancellation," May 2001.