**3GPP TSG-RAN WG4 Meeting #102-e R4-2200xxx**

**Electronic Meeting, 21th Feb – 3rd March, 2022**

**Agenda item:** 10.9.4.1, 10.9.4.2

**Source:** Moderator (Samsung)

**Title:** Email discussion summary for [102-e][320] NR\_HST\_FR2\_Demod\_Part1

**Document for:** Information

# Introduction

In RAN Plenary #89-e, the RAN4-led work item of NR support for high speed train (HST) scenario in FR2 has been approved [RP-202118] (which has been further revised to [RP-210800] with editorial revisions and updates on time schedule).

Based on the agreement captured in WF [R4-2203093], the test setup of UE demodulation was under discussion. For this meeting, companies are encouraged to further discuss the remaining issue for UE demodulation test set setup based on the FR2 HST deployment scenarios

In this email thread, the following agenda items will be discussed:

* 10.9.4..1 General
* 10.9.4.2 UE demodulation requirements
* 10.9.4.2.1 PDSCH requirements under Uni-directional scenario
* 10.9.4.2.2 PDSCH requirements under Bi-directional scenario

It is suggested to have the following target of 1st and 2nd round email discussion

* 1st round: Further discussion the remaining issue for UE demodulation test setup
* 2nd round: draft CR discussion and revised

# Topic #1: PDSCH requirement

*Main technical topic overview. The structure can be done based on sub-agenda basis.*

## Companies’ contributions summary

|  |  |  |
| --- | --- | --- |
| **T-doc number** | **Company** | **Proposals / Observations** |
| R4-2205754 | Huawei, HiSilicon, | Draft CR on minimum requirements for PDSCH HST-DPS (38.101-4) |
| R4-2206077 | Qualcomm | draft CR for FR2 HST - High speed Train Scenarios (B.3.4) |
| R4-2203541 | Samsung | Simulation results summary for Rel-17 FR2 HST UE demod |
| R4-2203543 | Samsung | Proposal 1: RAN4 define UE demodulation requirements with transmission schemes as   * Case 1: Uni-directional scenario A with DPS scheme 1b * Case 2: Bi-directional scenario B with DPS scheme 1a * Test applicable rule   + If UE is capable of more than 1 activated TCI state, UE should pass test both case 1 and case 2, otherwise, UE should only pass test of case 2   Proposal 2: RAN4 apply the following value for PDSCH allocation timeline for Uni-directional scenario A with DPS scheme 1b   * THARQ = 4 * TMAC = 24   Proposal 3: RAN4 apply the following test setup for Uni-directional scenario A with DPS scheme 1b   * Step 1: Two RRHs of RRH#(2k), RRH#(2k+1) are assumed, and SSB#(2k mod 4) and SSB#((2k+1 )mod 4) are transmitted for each TRPs, separately, where k is the RRH number with k =0, 1, 2, ….   + UE is configured with TCI#(2k mod 4) and TCI #((2k+1)mod 4) that are associated with TRS #(2k mod 4) and TRS#((2k+1)mod 4) transmitted from RRH#(2k) and RRH#(2k+1) respectively by RRC signalling tci-StatesToAddModList in the PDSCH-Config and tci-PresentInDCI is not configured;   + All the configured TCI states are known to UE. UE is configured with NZP-CSI-RS resource for L1-RSRP measurements by RRC signaling nzp-CSI-RS-ResourceSet within the CSI-ResourceConfig and periodic CSI reporting by setting reportConfigType to periodic and reportQuantity to cri-RSRP (Note: reported L1-RSRP mesurements are not tested) * Step 2: TE actives TCI #0 for PDCCH by “TCI State Indication for UE-specific PDCCH MAC CE”; * Step 3: PDSCH associated with TCI #0 is transmitted during the slots from 0 to [n-1 + THARQ + TMAC] * Step4 : In slot n TE start triggering TCI state switching command to TCI #1 by “TCI State Indication for UE-specific PDCCH MAC CE”; * Step 5: PDSCH associated with TCI #1 is transmitted in slots from n+1 + THARQ + TMAC to [N-1]. * PDSCH associated with TCI#(k mod 4) (k=1) is transmitted in slot from 0 to [n-1 + THARQ + TMAC] * PDSCH associated with TCI #(k mod 4) (k=2, 3,…) is transmitted in slot from [(k-1)\*n+1 + THARQ + TMAC] to [(k)n-1+ THARQ + TMAC], where n =57600 is the number of slots between the location of (k-1)Ds- DS\_offset and the location of (k)⋅DS-DS\_offset. And k is the RRH number in the channel model. * PDCCH and PDSCH are DTXed in other slots in which throughput statistics are not considered * The output of RRM discussion regarding FR2 HST TCI state switching time line can be considered to PDSCH requirement test setup. |
| R4-2203544 | Samsung | Proposal 1: RAN4 apply the following value for PDSCH allocation timeline for Bi-directional scenario B with DPS scheme 1a   * THARQ = 4 * TMAC proc = 24 * TfirstSSB = 80 * TSSB proc = 16 * TfirstTRSafterSSB  = 24 * TTRS proc = 16   **P**roposal 2: RAN4 apply the following test setup for Bi-directional scenario B with DPS scheme 1a   * Step 1: Three RRHs of RRH#(k-1), RRH#(k), RRH#(k+1) are assumed, and SSB#((2(k-1)+l)mod8), SSB#((2k+l)mod8), and SSB#((2(k+1)+l)mod8) are transmitted from each TRPs, separately, where k is the RRH number with k=1,2,3,…, l is the SSB index with l=0,1   + UE is configured with TCI#((2(k-1)+1) mod 8) (l=0,1) , TCI #((2k+1) mod 8) (l=0,1) and TCI#(((2k+1)+1)mod 8) (l=0,1) transmitted from RRH#(k-1), RRH#(k) and RRH#(k+1) respectively by RRC signalling tci-StatesToAddModList in the PDSCH-Config and tci-PresentInDCI is not configured;   + All the configured TCI states are known to UE. UE is configured with NZP-CSI-RS resource for L1-RSRP measurements by RRC signaling nzp-CSI-RS-ResourceSet within the CSI-ResourceConfig and periodic CSI reporting by setting reportConfigType to periodic and reportQuantity to cri-RSRP (Note: reported L1-RSRP measurements are not tested) * Step 2: TE actives TCI #2 for PDCCH by “TCI State Indication for UE-specific PDCCH MAC CE”; * Step 3: PDSCH associated with TCI #2 is transmitted during the slots from 0 to [n-1 + THARQ + TMAC ]; * Step 4: In slot n TE start triggering TCI state switching command to TCI #1 by “TCI State Indication for UE-specific PDCCH MAC CE”; * Step 5: PDSCH associated with TCI #1 is transmitted in slots from n+1 + THARQ + TMAC + TfirstSSB + TSSB proc + TfirstTRSafterSSB + TTRS proc to [2n-1+ THARQ + TMAC] * Step 6: In slot 2n TE start triggering TCI state switching command to TCI# 4 by “TCI State Indication for UE-specific PDCCH MAC CE” * Step 7: PDSCH associated with TCI #4 is transmitted in slots from [2n+1 + THARQ + TMAC + TfirstSSB + TSSB proc + TfirstTRSafterSSB + TSSB proc] to [3n-1+THARQ + TMAC] ; * PDSCH associated with TCI#(2k mod 8) (k=1) is transmitted in slot from 0 to [n-1 + THARQ + TMAC] * PDSCH associated with TCI #(2k mod 8) (k=2,3, …) is transmitted in slot from [(2k-2)n +1 + THARQ + TMAC + TfirstSSB + TSSB proc + TfirstTRSafterSSB + TTRS proc] to [(2k-1)n-1 + THARQ + TMAC] * PDSCH associated with TCI #((2k+1)mod 8) (k=0,1,2,…) is transmitted in slot from [(2k+1)n +1+ THARQ + TMAC + TfirstSSB + TSSB proc + TfirstTRSafterSSB + TTRS proc] to [(2(k+1)n-1+ THARQ + TMAC], where n =28800 slots is the half of the number of slots between two RRHs. * PDCCH and PDSCH are DTXed in other slots in which throughput statistic are not considered * The output of RRM discussion regarding FR2 HST TCI state switching time line can be considered to PDSCH requirement test setup. |
| R4-2204255 | CMCC | Observation 1: taking different scenario (scenario A and scenario B, uni-directional deployment and bi-directional deployment) and DPS transmission scheme into account, in total, there are 5 cases need to be considered:   * uni-directional scenario A with DPS scheme 1b (case 1) * uni-directional scenario A with DPS scheme 1a * uni-directional scenario B with DPS scheme 1b * uni-directional scenario B with DPS scheme 1a * bi-directional scenario B with DPS scheme 1a (case 2)   Observation 2: with the applicability rule of option 1, the performance of uni-directional scenario B with DPS scheme 1b and the performance of uni-directional scenario B with DPS scheme 1a are not guaranteed.  Observation 3: with the applicability rule of option 2, the performance of 5 cases summarized in observation 1 are guaranteed without introducing additional test cases.  Proposal 1: the applicability rule is proposed as following (option 2):   * If UE is capable of more than 1 activated TCI state, UE should pass test both case 1 and case 2, otherwise, UE should only pass test of case 2 * If UE passes case 1 (Uni-directional scenario A with DPS scheme 1b), the performance of Uni-directional scenario B with DPS scheme 1b are also guaranteed. |
| R4-2204387 | Intel | Proposal 1: Consider CSI-RS offset as 5 slots for CSI-RS for tracking resources 1, 2, 5 and 6. Consider CSI-RS offset as 6 slots for CSI-RS for tracking resources 3, 4, 7 and 8.  Proposal 2: Consider THARQ and TMAC Proc as 2 and 24 slots respectively for un-directional scenario A.  Proposal 3: For test case with bi-directional deployment consider: slot index per frame to carry MAC CE command is 2; THARQ as 2 slots; TMAC Proc as 24 slots; TfirstSSB as 134 slots; TSSB proc as 16 slots; TfirstTRSafterSSB as 69 slots; TTRS pro as 16 slots.  Proposal 4: Consider Option 1 as the test applicability rule.  Proposal 5: Schedule PDSCH in TDD special slots |
| R4-2204388 | Intel | DraftCR to TS 38.101-4: Applicability rules for HST FR2 PDSCH requirements |
| R4-2204432 | ZTE | Proposal 1: Option 1 is preferred for UE demodulation requirements.  Proposal 2: The following values can be considered as the excluded period for throughput statistics.   |  |  | | --- | --- | | **parameter** | **Value(# of slot)** | | **THARQ** | **8** | | **TMAC proc** | **8** | | **TfirstSSB** | **80** | | **TSSB proc** | **8** | | **TfirstTRSafterSSB** | **40** | | **TTRS pro** | **8** | |
| R4-2205083 | Ericsson | Proposal 1: Define UE demodulation requirements for Rel-17 FR2 HST-DPS with the applicability rule:   * Define FR2 PDSCH demodulation requirements with two cases:   + Case 1: Uni-directional scenario A with DPS scheme 1b   + Case 2: Bi-directional scenario B with DPS scheme 1a * If UE is capable of more than one activated TCI states, UE should pass both Case 1 and Case 2. If UE is capable of one activated TCI state, UE should pass Case 2 only.   Proposal 2: Configure NZP CSI-RS resources for CSI acquisition for all the TCI states so that the target TCI sate is known at the active TCI switching.  Proposal 3: Use the following parameters to derive the period after receiving MAC CE active TCI switching.   * THARQ = 2 (slots) * TMAC Proc = 3 (slots) * TSSB Proc = TTRS Proc = 2 (slots) * TfirstSSB and TfirstTRSafterSSB depending on the scheduling |
| R4-2205084 | Ericsson | draft CR: FRC for PDSCH demodulation requirement for FR2 HST |
| R4-2205756 | Huawei | Proposal 1: Agree the following applicability and do not any have impact on the specification.   * If UE passes case 1 (Uni-directional scenario A with DPS scheme 1b), the performance of Uni-directional scenario B with DPS scheme 1b are also guaranteed.   Proposal 2: For Uni-directional scenario with DPS scheme 1b, use same method as HST FR1 DPS to scheduling TCI state switching command using MCS4 in the slots where SSB transmitted, i.e. slot#57600n+56800 that is the closest SSB transmission slots. Then THARQ can be 4 slots based on specific “DDDSU” TDD pattern and TMAC Proc can be 24 slots that is corresponding to 3ms.  Proposal 3: Change the TRS configuration for TRS resource set 2 from l0=6/10 to l0=4/8. |
| R4-2205757 | Huawei | Proposal 1: For Bi-directional scenario with DPS scheme 1a, use same method as HST FR1 DPS to scheduling TCI state switching command using MCS4 in the slots where SSB transmitted, i.e. slot#28800n that is the closest SSB transmission slots. Then THARQ can be 4 slots based on specific “DDDSU” TDD pattern, TMAC Proc can be 24 slots that is corresponding to 3ms, TfirstSSB can be 132 slots that is calculated by min(SSB@slot#160n-THARQ-TMAC Proc), TSSB proc can be 16 slots that is corresponding to 2ms, TfirstTRSafterSSB can be 66 slots that is calculated by min(TRS@slot#(80n+2)-TSSB), TTRS proc can be 16 slots that is corresponding to 2ms.  Proposal 2: Change the TRS configuration for TRS resource set 2 from l0=6/10 to l0=4/8. |
| R4-2206073 | Qualcomm | Proposal 1: On the test applicability rules, we prefer to keep current agreement and support Option 1.  Proposal 2: Regarding the PDSCH timeline for bidirectional deployment, assume THARQ, TMAC proc, TSSB proc, TTRS proc, TfirstTRSafterSSB according to the computations above.   * THARQ Number of slots between PDSCH and corresponding HARQ-ACK information = 4 Slots (based on the agreed DDDSU TDD Pattern); * TMAC proc Number of slots for MAC CE processing = 24 Slots; (assuming 3ms); * TSSB proc Number of slots for SSB processing = 16 Slots (assuming 2ms); * TTRS proc Number of slots for TRS processing = 16 Slots (assuming 2ms); * TfirstTRSafterSSB Number of slots to the first TRS transmission occasion available after (TfirstSSB + TSSB proc) = 64 Slots (based on the agreed 10ms periodicity and TSSB proc=16);   Proposal 3: Regarding the PDSCH timeline, agree on the number of slots between adjacent TCI switch points on the tracks: n = 28800 Slots (assuming UE speed = 350km/h).  Observation 1: If the frame timing and the TCI switch pattern are aligned at t=0, x=0, then according to the values proposed in the previous section, TfirstSSB = 131 Slots.  Observation 2: If the frame boundary is not aligned with the UE at the start or only the first TCI switching command is offset with respect to the pattern, then TfirstSSB can be chosen during the design phase and reduced to optimize UE processing of target RS.  Proposal 4: RAN4 to consider how to set TfirstSSB depending on the two proposed approaches for alignment between TDD Frame and TCI switching timeline as described above and in the picture. |

## Open issues summary

Last RAN4 meeting agreements in the WF R4-2203093

List of open issues

* Sub-topic 1-1 Common setup
  + Issue 1-1-1: Test cases definition and test applicability rule
  + Issue 1-1-2: CSI-RS/TRS configuration
  + Issue 1-1-3: NZP CSI-RS resource configuration
  + Issue 1-1-4: Whether to schedule PDSCH in TDD special slots
* Sub-topic 1-2: PDSCH requirement for Uni-directional scenario
  + Issue 1-2-1: Slot for scheduling TCI switching command
  + Issue 1-2-2: PDSCH allocation timeline for Uni-directional scenario with DPS scheme 1b
  + Issue 1-2-3: Test setup for PDSCH allocation timeline for Uni-directional scenario
* Sub-topic 1-3: PDSCH requirement for Bi-directional scenario
  + Issue 1-3-1: Slot for scheduling TCI switching command
  + Issue 1-3-2: Method to set Tfirst SSB
  + Issue 1-3-3: PDSCH allocation time for Bi-directional scenario with DPS scheme 1a
  + Issue 1-3-4: Test setup for PDSCH allocation timeline for Bi-directional scenario

### Sub-topic 1-1: Common setup

**Issue 1-1-1: Test cases definition and test applicability rule**

* Observation
  + Observation 1(CMCC):
    - taking different scenario (scenario A and scenario B, uni-directional deployment and bi-directional deployment) and DPS transmission scheme into account, in total, there are 5 cases need to be considered:
* uni-directional scenario A with DPS scheme 1b (case 1)
* uni-directional scenario A with DPS scheme 1a
* uni-directional scenario B with DPS scheme 1b
* uni-directional scenario B with DPS scheme 1a
* bi-directional scenario B with DPS scheme 1a (case 2)
* PDCCH/PDSCH/PBCH SFN transmitted from two RRHs
  + - With current applicability agreed in last meeting, even if both case 1 (Uni-directional scenario A with DPS scheme 1b) and case 2 (Bi-directional scenario B with DPS scheme 1a) are tested, the performance of bi-directional scenario A with DPS scheme 1b and the performance of uni-directional scenario B with DPS 1a are not guaranteed.
    - With the applicability rule of option 2, the performance of 5 cases summarized in observation 1 are guaranteed without introducing additional test cases.
* Proposals
  + Option 1 (Intel, Samsung, ZTE, Qualcomm, Ericsson):
    - If UE is capable of more than 1 activated TCI state, UE should pass test both case 1 and case 2, otherwise, UE should only pass test of case 2
  + Option 2 (CMCC): Update the test applicability rule
    - If UE is capable of more than 1 activated TCI state, UE should pass test both case 1 and case 2, otherwise, UE should only pass test of case 2
    - If UE passes case 1 (Uni-directional scenario A with DPS scheme 1b), the performance of Uni-directional scenario B with DPS scheme 1b are also guaranteed.
  + Option 3 (Huawei): Agree the following applicability and do not have any impact on the specification.
    - If UE passes case 1 (Uni-directional scenario A with DPS scheme 1b), the performance of Uni-directional scenario B with DPS scheme 1b are also guaranteed.
* Recommended WF
  + RAN4 define UE demodulation requirements with transmission schemes with test applicable rule as
    - Case 1: Uni-directional scenario A with DPS scheme 1b
    - Case 2: Bi-directional scenario B with DPS scheme 1a
    - Test applicable rule
* If UE is capable of more than 1 activated TCI state, UE should pass test both case 1 and case 2, otherwise, UE should only pass test of case 2

**Issue 1-1-2: CSI-RS/TRS configuration**

* Proposals
  + Option 1(Huawei): Change the TRS configuration for TRS resource set 2 from l0=6/10 to l0 =4/8
  + Option 2(Intel): Consider CSI-RS offset as 5 slots for tracking resources 1,2, 5 and 6, and consider CSI-RS offset as 6 slots for CSI-RS for tracking resource 3,4,7 and 8
* Recommended WF
  + Encourage comments if any.

**Issue 1-1-3: NZP CSI-RS resources configuration**

* Proposals
  + Option 1(Ericsson): Configure NZP CSI-RS resources for CSI acquisition for all the TCI states so that the target TCI sate is known at the active TCI switching.
* Recommended WF
  + Option 1

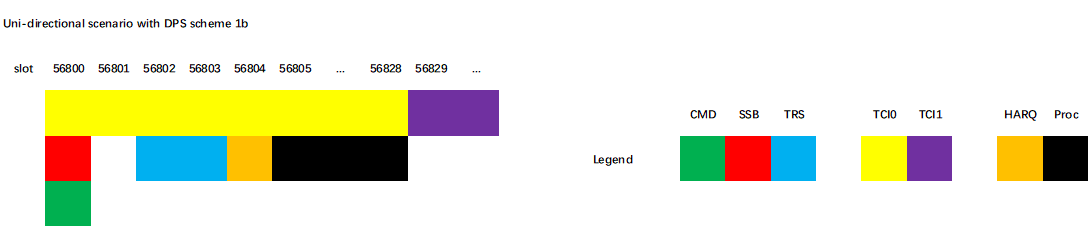
**Issue 1-1-4: Whether to schedule PDSCH in TDD special slots**

* Proposals
  + Option 1(Intel): Yes
* Recommended WF
  + Option 1

### Sub-topic 1-2: PDSCH requirement for Uni-directional scenario

**Issue 1-2-1: Slot for scheduling TCI switching command**

* Proposals
  + Option 1(Samsung): slot# 57600n slots (assuming UE speed =350km/h)
  + Option 2 (Huawei): slot#57600n+56800 slots



* Recommended WF
  + Encourage comments if any.

**Issue 1-2-2: PDSCH allocation timeline for Uni-directional scenario A with DPS scheme 1b**

* Proposals
  + Option 1(Samsung, Huawei, Qualcomm):
    - THARQ = 4 (slots)
    - TMAC proc = 24 (slots)
  + Option 2(ZTE):
    - THARQ = 8 (slots)
    - TMAC proc = 8 (slots)
  + Option 3(Ericsson):
    - THARQ = 2 (slots)
    - TMAC proc = 3 (slots)
  + Option 4(Intel):
    - THARQ = 2 (slots)
    - TMAC proc = 24 (slots)
* Recommended WF
  + RAN4 apply the following value for PDSCH allocation timeline for Uni-directional scenario A with DPS scheme 1b
    - THARQ = 4 (slots)
    - TMAC proc = 24 (slots)

**Issue 1-2-3: Test setup for PDSCH allocation timeline for Uni-directional scenario**

* Proposals
  + Option 1(Samsung):
    - Step 1: Two RRHs of RRH#(2k), RRH#(2k+1) are assumed, and SSB#(2k mod 4) and SSB#((2k+1 )mod 4) are transmitted for each TRPs, separately, where k is the RRH number with k =0, 1, 2, ….
* UE is configured with TCI#(2k mod 4) and TCI #((2k+1)mod 4) that are associated with TRS #(2k mod 4) and TRS#((2k+1)mod 4) transmitted from RRH#(2k) and RRH#(2k+1) respectively by RRC signalling tci-StatesToAddModList in the PDSCH-Config and tci-PresentInDCI is not configured;
* All the configured TCI states are known to UE. UE is configured with NZP-CSI-RS resource for L1-RSRP measurements by RRC signaling nzp-CSI-RS-ResourceSet within the CSI-ResourceConfig and periodic CSI reporting by setting reportConfigType to periodic and reportQuantity to cri-RSRP (Note: reported L1-RSRP mesurements are not tested)
  + - Step 2: TE actives TCI #0 for PDCCH by “TCI State Indication for UE-specific PDCCH MAC CE”;
    - Step 3: PDSCH associated with TCI #0 is transmitted during the slots from 0 to [n-1 + THARQ + TMAC]
    - Step4 : In slot n TE start triggering TCI state switching command to TCI #1 by “TCI State Indication for UE-specific PDCCH MAC CE”;
    - Step 5: PDSCH associated with TCI #1 is transmitted in slots from n+1 + THARQ + TMAC to [N-1].
    - PDSCH associated with TCI#(k mod 4) (k=1) is transmitted in slot from 0 to [n-1 + THARQ + TMAC]
    - PDSCH associated with TCI #(k mod 4) (k=2, 3,…) is transmitted in slot from [(k-1)\*n+1 + THARQ + TMAC] to [(k)n-1+ THARQ + TMAC], where n =57600 is the number of slots between the location of (k-1)Ds- DS\_offset and the location of (k)⋅DS-DS\_offset. And k is the RRH number in the channel model.
    - PDCCH and PDSCH are DTXed in other slots in which throughput statistics are not considered
    - The output of RRM discussion regarding FR2 HST TCI state switching time line can be considered to PDSCH requirement test setup.
* Recommended WF
  + Encourage comments if any.

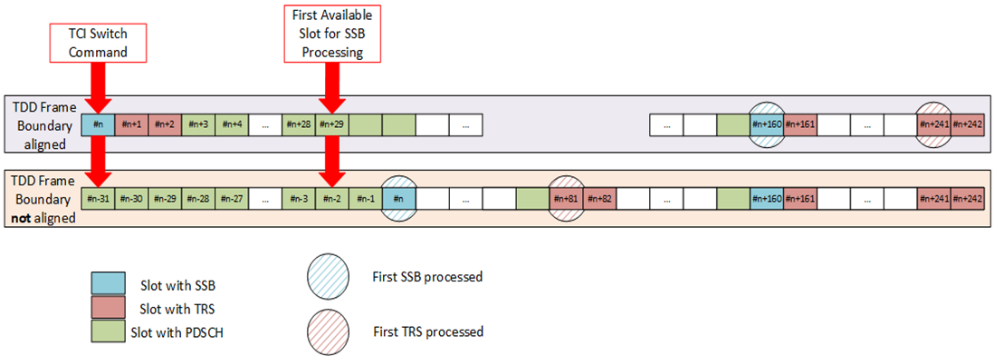
### Sub-topic 1-3: PDSCH requirement for Bi-directional scenario

**Issue 1-3-1: Slot for scheduling TCI switching command**

* Proposals
  + Option 1(Qualcomm, Huawei, Samsung): slot# 28800n slots (assuming UE speed =350km/h)
* Recommended WF
  + Option 1

**Issue 1-3-2: Method to set Tfirst SSB**

* Observations
  + Observation 1(Qualcomm):
    - If the frame timing and the TCI switch pattern are aligned at t=0, x=0, then according to the values proposed in the previous section, TfirstSSB = 131 Slots.
    - If the frame boundary is not aligned with the UE at the start or only the first TCI switching command is offset with respect to the pattern, then TfirstSSB can be chosen during the design phase and reduced to optimize UE processing of target RS.
* Proposals
  + Option 1(Qualcomm):
    - RAN4 to consider how to set TfirstSSB depending on the two proposed approaches for alignment between TDD Frame and TCI switching timeline as described above and in the picture



* Recommended WF
  + Encourage comments if any

**Issue 1-3-3: PDSCH allocation timeline for Bi-directional scenario B with DPS scheme 1a**

* Proposals
  + Option 1(Samsung):
    - THARQ = 4 (slots)
    - TMAC proc = 24 (slots)
    - TfirstSSB = 80 (slots)
    - TSSB pros  = 16 (slots)
    - TfirstTRSafterSSB = 24 (slots)
    - TTRSproc  = 16 (slots)
  + Option 2(ZTE):
    - THARQ = 8 (slots)
    - TMAC proc = 8 (slots)
    - TfirstSSB = 80(slots)
    - TSSB pros  = 80 (slots)
    - TfirstTRSafterSSB = 40 (slots)
    - TTRSproc  = 8 (slots)
  + Option 3(Intel)
    - THARQ = 2 (slots)
    - TMAC proc = 24 (slots)
    - TfirstSSB = 134 (slots)
    - TSSB pros  = 16 (slots)
    - TfirstTRSafterSSB = 69 (slots)
    - TTRSproc  = 16 (slots)
  + Option 4(Ericsson):
    - THARQ = 2 (slots)
    - TMAC proc = 3 (slots)
    - TSSB pros  = 2 (slots)
    - TTRSproc  = 2 (slots)
    - TfirstTRSafterSSB and TfirstSSB depending on the scheduling
  + Option 5(Huawei):
    - THARQ = 4 (slots)
    - TMAC proc = 24 (slots)
    - TfirstSSB = 132 (slots), based on min (SSB@slot#160n-THARQ-TMAC Proc)
    - TSSB pros  = 16 (slots)
    - TfirstTRSafterSSB = 66 (slots), based on min(TRS@slot#(80n+2)-TSSB)
    - TTRSproc  = 16 (slots)
  + Option 6(Qualcomm):
    - THARQ = 4 (slots) (based on agreed DDDSU TDD pattern)
    - TMAC proc = 24 (slots) (Assuming 3ms)
    - TSSB pros  = 16 (slots) (Assuming 2ms)
    - TTRSproc  = 16 (slots) (Assuming 2m)
    - TfirstSSB = 131 (slots), based on the alignment of TDD pattern and TCI switching timeline
    - TfirstTRSafterSSB = 64 (slots), based on the agreed 10ms periodicity and TSSB proc =16
* Recommended WF
  + RAN4 apply the following value for PDSCH allocation timeline for Bi-directional scenario A with DPS scheme 1a
    - THARQ = 4 (slots)
    - TMAC proc = 24 (slots)
    - TTRSproc  = 16 (slots)
    - TSSB pros = 16 (slots)
  + FFS on Value of TfirstSSB
    - Option 1 (Samsung): 80
    - Option 2 (ZTE): 80
    - Option 3 (Intel): 134
    - Option 4 (Ericsson): pending on the schedule
    - Option 5 (Huawei): 132
    - Option 6 (Qualcomm): 131
  + FFS on Value of TfirstTRSafterSSB
    - Option 1 (Samsung): 24
    - Option 2 (ZTE): 40
    - Option 3 (Intel ): 69
    - Option 4 (Ericsson): pending on the schedule
    - Option 5 (Huawei): 66
    - Option 6 (Qualcomm): 64

**Issue 1-3-4: Test setup for PDSCH allocation timeline for Bi-directional scenario**

* Proposals
  + Option 1(Samsung):
    - Step 1: Three RRHs of RRH#(k-1), RRH#(k), RRH#(k+1) are assumed, and SSB#((2(k-1)+l)mod8), SSB#((2k+l)mod8), and SSB#((2(k+1)+l)mod8) are transmitted from each TRPs, separately, where k is the RRH number with k=1,2,3,…, l is the SSB index with l=0,1
* UE is configured with TCI#((2(k-1)+1) mod 8) (l=0,1) , TCI #((2k+1) mod 8) (l=0,1) and TCI#(((2k+1)+1)mod 8) (l=0,1) transmitted from RRH#(k-1), RRH#(k) and RRH#(k+1) respectively by RRC signalling tci-StatesToAddModList in the PDSCH-Config and tci-PresentInDCI is not configured;
* All the configured TCI states are known to UE. UE is configured with NZP-CSI-RS resource for L1-RSRP measurements by RRC signalling nzp-CSI-RS-ResourceSet within the CSI-ResourceConfig and periodic CSI reporting by setting reportConfigType to periodic and reportQuantity to cri-RSRP (Note: reported L1-RSRP measurements are not tested)
  + - Step 2: TE actives TCI #2 for PDCCH by “TCI State Indication for UE-specific PDCCH MAC CE”;
    - Step 3: PDSCH associated with TCI #2 is transmitted during the slots from 0 to [n-1 + THARQ + TMAC ];
    - Step 4: In slot n TE start triggering TCI state switching command to TCI #1 by “TCI State Indication for UE-specific PDCCH MAC CE”;
    - Step 5: PDSCH associated with TCI #1 is transmitted in slots from n+1 + THARQ + TMAC + TfirstSSB + TSSB proc + TfirstTRSafterSSB + TTRS proc to [2n-1+ THARQ + TMAC]
    - Step 6: In slot 2n TE start triggering TCI state switching command to TCI# 4 by “TCI State Indication for UE-specific PDCCH MAC CE”
    - Step 7: PDSCH associated with TCI #4 is transmitted in slots from [2n+1 + THARQ + TMAC + TfirstSSB + TSSB proc + TfirstTRSafterSSB + TSSB proc] to [3n-1+THARQ + TMAC] ;
    - PDSCH associated with TCI#(2k mod 8) (k=1) is transmitted in slot from 0 to [n-1 + THARQ + TMAC]
    - PDSCH associated with TCI #(2k mod 8) (k=2,3, …) is transmitted in slot from [(2k-2)n +1 + THARQ + TMAC + TfirstSSB + TSSB proc + TfirstTRSafterSSB + TTRS proc] to [(2k-1)n-1 + THARQ + TMAC]
    - PDSCH associated with TCI #((2k+1)mod 8) (k=0,1,2,…) is transmitted in slot from [(2k+1)n +1+ THARQ + TMAC + TfirstSSB + TSSB proc + TfirstTRSafterSSB + TTRS proc] to [(2(k+1)n-1+ THARQ + TMAC), where n =28800 slots is the half of the number of slots between two RRHs.
    - PDCCH and PDSCH are DTXed in other slots in which throughput statistic are not considered
    - The output of RRM discussion regarding FR2 HST TCI state switching time line can be considered to PDSCH requirement test setup
* Recommended WF
  + Encourage comments if any.

## Companies views’ collection for 1st round

### Open issues

*One of the two formats, i.e. either example 1 or 2 can be used by moderators.*

Sub topic 1-1

|  |  |
| --- | --- |
| **Company** | **Comments** |
| CMCC | Issue 1-1-1:  Support option 2. Firstly, we would like to clarify that our intension is not to increase the number of test case, we are OK to only define test cases for case 1 and case 2, just want to update the applicability rule to guarantee the performance of more cases. The applicability rule of option 2 provides better test coverage without introducing additional test cases.  For scenario A, it was agreed to define requirements only for uni-directional. Considering DPS transmission schemes includes DPS 1a and DPS 1b depending on UE capability, there are two cases for scenario A: uni-directional scenario A with DPS scheme 1b, and uni-directional scenario A with DPS scheme 1a.  For scenario B, it was agreed to define requirements for uni-directional and bi-directional. While for DPS 1b, it is only applied to uni-directional case. There are three cases for scenario B: uni-directional scenario B with DPS scheme 1b, uni-directional scenario B with DPS scheme 1a, and bi-directional scenario B with DPS scheme 1a.  Taking above previous agreements into account, there are 5 cases:  • uni-directional scenario A with DPS scheme 1b (case 1)  • uni-directional scenario A with DPS scheme 1a  • uni-directional scenario B with DPS scheme 1b  • uni-directional scenario B with DPS scheme 1a  • bi-directional scenario B with DPS scheme 1a (case 2)  However, with the applicability rule of Option 1, the performance of uni-directional scenario B with DPS scheme 1b and the performance of uni-directional scenario B with DPS scheme 1a are not guaranteed (as highlighted in yellow as above).  Only defining test cases for case1 and case 2, with the applicability rule of option 2, the performance of all above 5 cases are guaranteed. What’s more, for the 2nd bullet of option 2, in our view, it is straightforward that if UE passes case 1 (Uni-directional scenario A with DPS scheme 1b), the performance of Uni-directional scenario B with DPS scheme 1b are also guaranteed, since the only difference is Dmin. |
| Ericsson | Issue 1-1-1:  Support the recommended WF.  Issue 1-1-2:  In general we agree we need to change the TRS symbols scheduling. We slight prefer Option 2 – schedule TRS in DL slots. This is related to Issue 1-1-4; if we schedule PDSCH in the special slots, we prefer not to schedule TRS in the special slots.  Issue 1-1-3:  Support the recommended WF.  Issue 1-1-4:  Support the recommended WF. |
| Intel | **Issue 1-1-1: Test cases definition and test applicability rule** We are fine with either Option 1 or Option 3. As we understood, Option 3 means the same as Option 1 but in addition to capture formal agreement that “If UE passes case 1 (Uni-directional scenario A with DPS scheme 1b), the performance of Uni-directional scenario B with DPS scheme 1b are also guaranteed” without implementing this to specification” that we believe common RAN4 understanding.  **Issue 1-1-2: CSI-RS/TRS configuration**  Both options are fine for us.  **Issue 1-1-3: NZP CSI-RS resources configuration**  Support the recommended WF. |
| Huawei | **Issue 1-1-1: Test cases definition and test applicability rule**  We prefer Option 3 to ensure the performance of Uni-directional scenario B with DPS scheme 1b also considering we don’t define performance requirement for this case.  **Issue 1-1-2: CSI-RS/TRS configuration**  We prefer Option 1. We think it is feasible to transmit TRS in special slot considering the AWGN channel model.  **Issue 1-1-3: NZP CSI-RS resources configuration**  Support the recommended WF.  **Issue 1-1-4: Whether to schedule PDSCH in TDD special slots**  Support the recommended WF. |

Sub topic 1-2

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| **Company** | **Comments** |
| XXX | Issue 1-2-1  Issue 1-2-2  Issue 1-2-3 |
| Ericsson | Issue 1-2-1  We think it depends on the UE start position. In the last meeting RAN4 agreed to set the following channel model for uni-directional channel model.    In our understanding, Option 1 is the case UE start position is the beginning of RRH coverage region. Option 2 is the case UE start positions is the closest location to RRH. (See the figure above also)  Firstly, we need to agree with the UE starting position. Considering the test setup discussed in Issue 1-2-3, we slight prefer Option 1 because the test setup becomes simple.  Issue 1-2-2  We support the recommended WF.  Issue 1-2-3  This test setup is the case of Option 1 in Issue 1-2-1. We are fine with this assumption if Option 1 is agreed in Issue 1-2-1. |
| Intel | **Issue 1-2-1: Slot for scheduling TCI switching command**  HST-SFN FR1 channel model assumes that the UE start position is near the RRH. In this case we slightly prefer Option 2 to have consistency with FR1 assumptions  **Issue 1-2-2: PDSCH allocation timeline for Uni-directional scenario A with DPS scheme 1b**  Assuming MAC CE command Tx in slot with SSB we are fine with recommended WF.  **Issue 1-2-3: Test setup for PDSCH allocation timeline for Uni-directional scenario**  This setup depends on issue 1-2-1 and should be updated in case Option 2 is agreed for issue 1-2-1.  Also, we suggest adding at the end of step 4 “with MCS 4”. |
| Huawei | **Issue 1-2-1: Slot for scheduling TCI switching command**  We think the two Options are equivalent. The only difference is the starting point offset and the corresponding RRH position and TCI switching point offset. We are fine with both Options.  **Issue 1-2-2: PDSCH allocation timeline for Uni-directional scenario A with DPS scheme 1b**  Support the recommended WF.  **Issue 1-2-3: Test setup for PDSCH allocation timeline for Uni-directional scenario**  Further update can be considered from our understanding.   * Step 3: PDSCH associated with TCI #0 is transmitted during the slots from 0 to n + THARQ + TMAC * PDSCH associated with TCI#(k mod 4) (k=1) is transmitted in slot from 0 to n + THARQ + TMAC * PDSCH associated with TCI #(k mod 4) (k=2, 3,…) is transmitted in slot from (k-1)\*n+1 + THARQ + TMAC to k\*n + THARQ + TMAC, where n =57600 is the number of slots between the location of (k-1)Ds- DS\_offset and the location of (k)⋅DS-DS\_offset. And k is the RRH number in the channel model. |

Sub topic 1-3

|  |  |
| --- | --- |
| **Company** | **Comments** |
| XXX | Issue 1-3-1  Issue 1-3-2  Issue 1-3-3  Issue 1-3-4 |
| Ericsson | Issue 1-3-1  Support the recommended WF.  Issue 1-3-2  It depends on the scheduling of active TCI states switching. We propose to conclude Issue 1-3-4 first and then discuss it.  Issue 1-3-3  We are fine to assume the following parameters:   * THARQ = 4 (slots) * TMAC proc = 24 (slots) * TTRSproc = 16 (slots) * TSSB pros = 16 (slots)   The first SSB and first TRS after SSB depends on the scheduling of the active TCI switching and TRS location discussed in Issue 1-3-2/1-3-4 and Issue 1-1-2.  We propose to discuss TfirstSSB and TfirstTRSafterSSB after we conclude Issues 1-1-2 and 1-3-2/1-3-4.  Issue 1-3-4  In our understanding TCI#2, TCI#1, and TCI#4 correspond to #1, #0, #2, respectively, in the figure below. If we assume UE starting point is the location closest to RRH#0, this scheduling looks fine. |
| Intel | **Issue 1-3-1: Slot for scheduling TCI switching command**  Support Option 1.  **Issue 1-3-2: Method to set Tfirst SSB**  We think network scheduler can be optimized to reduce Tfirst\_SSB in such way as Qualcomm mentioned (Approach 2). We support to postpone first TCI state switching command to additional 131 slots after 28800 slots to reduce TCI state switching delay.  **Issue 1-3-3: PDSCH allocation timeline for Bi-directional scenario B with DPS scheme 1a**  Support the recommended WF. TfirstSSB andTfirstTRSafterSSB can be calculated after resolving issue 1-3-2.  **Issue 1-3-4: Test setup for PDSCH allocation timeline for Bi-directional scenario**  Depends on the approaches mentioned in issue 1-3-2. Current setting assumes the first approach when TCI switch pattern and TDD frame boundary are aligned. This issue can be confirmed after resolving issue 1-3-2. Also, we suggest adding at the end of step 4 “with MCS 4”. |
| Huawei | **Issue 1-3-1: Slot for scheduling TCI switching command**  Support the recommended WF.  **Issue 1-3-2: Method to set Tfirst SSB**  We prefer to consider aligned TCI switch pattern with the frame timing.  **Issue 1-3-3: PDSCH allocation timeline for Bi-directional scenario B with DPS scheme 1a**  Support the recommended WF. We think there is some issues need to clarification.   * Assuming that SSB#0/1/2/3 and SSB#4/5/6/7 is transmitted in slot#x and slot#x+1   + Option 1: Tfirst SSB is corresponding to the slot#x+1 for all cases   + Option 2: Tfirst SSB is corresponding to the slot#x for the cases target SSB is SSB#0/1/2/3, Tfirst SSB is corresponding to the slot#x+1 for the cases target SSB is SSB#4/5/6/7 * Assuming that target TRS is transmitted in slot#x and slot#x+1   + Option 1: Tfirst TRS is corresponding to the slot#x that is same as HST FR1.   + Option 2: Tfirst TRS is corresponding to the slot#x+1 considering receive two consecutive TRS before TRS processing.   **Issue 1-3-4: Test setup for PDSCH allocation timeline for Bi-directional scenario**  Further update can be considered from our understanding.   * + - Step 3: PDSCH associated with TCI #2 is transmitted during the slots from 0 to n + THARQ + TMAC ;     - Step 5: PDSCH associated with TCI #1 is transmitted in slots from n+1 + THARQ + TMAC + TfirstSSB + TSSB proc + TfirstTRSafterSSB + TTRS proc to 2n+ THARQ + TMAC     - Step 7: PDSCH associated with TCI #4 is transmitted in slots from 2n+1 + THARQ + TMAC + TfirstSSB + TSSB proc + TfirstTRSafterSSB + TSSB proc to 3n+THARQ + TMAC ;     - PDSCH associated with TCI#(2k mod 8) (k=1) is transmitted in slot from 0 to n + THARQ + TMAC     - PDSCH associated with TCI #(2k mod 8) (k=2,3, …) is transmitted in slot from (2k-2)n +1 + THARQ + TMAC + TfirstSSB + TSSB proc + TfirstTRSafterSSB + TTRS proc to (2k-1)n + THARQ + TMAC     - PDSCH associated with TCI #((2k+1)mod 8) (k=0,1,2,…) is transmitted in slot from (2k+1)n +1+ THARQ + TMAC + TfirstSSB + TSSB proc + TfirstTRSafterSSB + TTRS proc to (2(k+1)n+ THARQ + TMAC), where n =28800 slots is the half of the number of slots between two RRHs. |

### CRs/TPs comments collection

*For close-to-finalize Wis and maintenance work, comments collections can be arranged for TPs and CRs. For ongoing Wis, suggest to focus on open issues discussion on 1st round.*

|  |  |
| --- | --- |
| **CR/TP number** | **Comments collection** |
| R4-2204388  (DraftCR to TS 38.101-4: Applicability rules for HST FR2 PDSCH requirements) | Ericsson: Same as HST FR1, we need to add applicability for ‘Support number of active TCI states per BWP per CC’ in 7.1.1.4, according to the conclusion. |
| Company B |
|  |
| R4-2205084  (draft CR: FRC for PDSCH demodulation requirement for FR2 HST) | Company A |
| Company B |
|  |
| R4-2205754  (Draft CR on minimum requirements for PDSCH HST-DPS (38.101-4)) | Company A |
| Company B |
|  |
| R4-2206077  (draft CR for FR2 HST - High speed Train Scenarios (B.3.4)) | Ericsson: Ds\_offset for Scenario A is agreed as 10m. |
| Company B |
|  |

## Summary for 1st round

### Open issues

*Moderator tries to summarize discussion status for 1st round, list all the identified open issues and tentative agreements or candidate options and suggestion for 2nd round i.e. WF assignment.*

|  |  |
| --- | --- |
|  | **Status summary** |
| **Sub-topic #1** | *Tentative agreements:*  *Candidate options:*  *Recommendations for 2nd round:* |

### CRs/TPs

*Moderator tries to summarize discussion status for 1st round and provides recommendation on CRs/TPs Status update*

*Note: The tdoc decisions shall be provided in Section 3 and this table is optional in case moderators would like to provide additional information.*

|  |  |
| --- | --- |
| **CR/TP number** | **CRs/TPs Status update recommendation** |
| XXX | *Based on 1st round of comments collection, moderator can recommend the next steps such as “agreeable”, “to be revised”* |

## Discussion on 2nd round (if applicable)

# Recommendations for Tdocs

## 1st round

**New tdocs**

|  |  |  |
| --- | --- | --- |
| **Title** | **Source** | **Comments** |
|  |  |  |
|  |  |  |

**Existing tdocs**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Tdoc number** | **Title** | **Source** | **Recommendation** | **Comments** |
|  |  |  |  |  |

Notes:

1. Please include the summary of recommendations for all tdocs across all sub-topics incl. existing and new tdocs.
2. For the Recommendation column please include one of the following:
   1. CRs/TPs: Agreeable, Revised, Merged, Postponed, Not Pursued
   2. Other documents: Agreeable, Revised, Noted
3. For new LS documents, please include information on To/Cc WGs in the comments column
4. Do not include hyper-links in the documents

## 2nd round

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Tdoc number** | **Title** | **Source** | **Recommendation** | **Comments** |
|  |  |  |  |  |

Notes:

1. Please include the summary of recommendations for all tdocs across all sub-topics.
2. For the Recommendation column please include one of the following:
   1. CRs/TPs: Agreeable, Revised, Merged, Postponed, Not Pursued
   2. Other documents: Agreeable, Revised, Noted
3. Do not include hyper-links in the documents

# Annex

Contact information

|  |  |  |
| --- | --- | --- |
| **Company** | **Name** | **Email address** |
| Moderator (Samsung) | Yunchuan Yang | yc0301.yang@samsung.com |
| Ericsson | Kazuyoshi Uesaka | kazuyoshi.uesaka@ericsson.com |

Note:

1. Please add your contact information in above table once you make comments on this email thread.
2. If multiple delegates from the same company make comments on single email thread, please add you name as suffix after company name when make comments i.e. Company A (XX, XX)