**3GPP TSG-RAN WG4 Meeting # 102-e R4-21XXXXX**

**Electronic Meeting, 21 February – 3 March 2022**

**Agenda item:** 11.4.1, 11.4.2, 11.4.3, 11.4.4, 11.4.5, 11.4.6

**Source:** Moderator (Qualcomm Incorporated)

**Title:** Email discussion summary for [102-e][141] FS\_NR\_Opt\_pi2BPSK

**Document for:** Information

# 1.0 Introduction

In this paper, RAN4 will treat the SI ‘Optimizations of pi/2 BPSK uplink power in NR’ in Rel-17.

Suggested email discussion for 1st round is as follows:

* 1st round: RAN4 to discuss:
  + Topic #1-1: Power boost
  + Topic #1-2: MPR
  + Topic #1-3: General and workplan

*Main technical topic overview. The structure can be done based on sub-agenda basis.*

## Company contributions summary

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| **T-doc number** | **Company** | **Proposals / Observations** |
| R4-2203682 | Apple | Proposal 1: Use conditions provided in Table 4 and the coefficients in Table 5 for classifying the RB regions    Proposal 2: In case the maximum power boost would be set to 1.5dB use MPR provided in Table 6    Proposal 3: In case the maximum power boost would be set to 1.0dB use MPR provided in Table 7    Proposal 4: Limit UL slots in radio frame to max 25% to guarantee SAR compliance and to reduce strain on amplifier |
| R4-2204012 | Qualcomm Incorporated | TR38.868 on optimizations of pi/2 BPSK UL power |
| R4-2204013 | Qualcomm Incorporated | TP for TR38.868 with company contributions from RAN4#101-bis-e |
| R4-2204016 | Qualcomm Incorporated | Proposal 1: PC2 power boost limited to 1 dB  Observation 1: Gain compression with output power causes PAs to require even larger input drives to achieve higher power boost values  Observation 2: Maintaining high boost powers at higher frequencies requires even larger PA input drive due to gain roll-off with frequency and gain compression with output power. This larger input drive will impact the reliability of the PA and the drive requirements of the RF transceiver.  Observation 3: Higher boost powers increase PA power consumption and leads to the need for higher current drive PMUs.  Observation 4: Larger PA bias currents leads to greater thermal dissipation and may lead to heating issues inside the UE and impact PA reliability  Observation 5: Thermal reliability of the front-end components must be evaluated to ensure they can withstand the higher PA powers  Observation 6: If a larger PC2 PA is adopted for obtaining higher gain boost then the MPRs all other modulations and waveform types using the same PA would have to be re-evaluated.  Observation 7: Our studies indicate that 1 dB of power boost is achievable with today’s hardware while boost > 1 dB would require redesign of the transceiver TX chain and PC2 PA and a comprehensive overhaul of the PC2 MPRs |
| R4-2204085 | Huawei, HiSilicon | Observation 1: For DFT-s-OFDM waveforms with Pi/2 BPSK modulation, it might be possible to boost the PC2 PA power by 1~2dB. However, the higher the power is boosted, the larger challenge it imposes on the PA/PMU, RFIC as well as other front-end components in terms of stability and sustainability.  Proposal 1: The minimum requirement on PC2 power boosting is ≤ 1dB, i.e. MPR ≥ 2dB w.r.t. 29dBm. And a UE is allowed to boost more than 1 dB if it’s able to.  Proposal 2: The percentage of the maximum number of uplink transmission slots in a radio frame is <= [25%].  Observation 2: For the inner centred region, the Tx power can be boosted with no/moderate filtering, while moderate/aggressive filtering is needed for other regions.  Observation 3: The loss of Rx performance (e.g. Rx SNR@10%BLER) increases with the aggressiveness of the filter. More than 1 dB loss was reported for the 3-tap filter [0.335, 1, 0.335].  Observation 4: The net gain for the inner centred region should be the most and it diminishes in other regions.  Observation 5: The study of power boosting has been focused on small number of RBs such as 2/4/8/16/64, which are the typical use cases for cell edge UEs.  Proposal 3: Adopt simpler RB classification scheme such as new-inner, new-outer and edge allocations. The exact definitions are left for the WI stage to allow more time for refinement and verification.  Proposal 4: Define the MPR requirements of Pi/2 BPSK for PC2 1Tx as in Table 1.    Proposal 5: Further study the power boosting requirements for PC2 with dual Tx. More measurements are needed. This can be done in the study phase of the future WI, or the SI is extended by one quarter, which can be discussed in RAN#95-e. |
| R4-2204414 | Intel Corporation | Based on TP [1] for the TR 38.868 from RAN4 101-bis-e, the following text proposals and modifications are made:   1. Section 5.5 – Addition of BLER figures to further support LLS tables already included 2. Section 6.2.3 – Inclusion of Tx + Rx Link margin analysis as noted in RAN4 101-bis-e meeting    1. New analysis of Tx+Rx link margin comparing filters 3. Section 8.4 – Update of power enhancement MPR curves.    1. Change of reference value from 29dBm to 26dBm to be more consistent with the rest of TR 38.868.    2. Additional MPR figures. |
| R4-2204415 | Intel Corporation | Observation 1: The moderately aggressive [0.28 1 0.28] filter also gives the highest performance for outer RB locations  Observation 2: for inner RB locations no filter or the least aggressive [0.2 1 0.2] filter is best for avoiding Rx performance degradation due to filtering.  Observation 3: The MPR values in the inner RBs for LCRB < 20, are the same for all filters including the no filter results. In this RB region, filtering provides no clear advantage. |
| R4-2204481 | MediaTek Inc. | Proposal 1: Option 1 is proposed. For 1Tx PC2 PAs, the power boost should be limited to within 1dB  Proposal 2: We support option 2: Update MPR tables (at least Table 6.2.2-2) in TS 38.101-1. Reclassification of RB regions for MPR shall be postponed to Rel-18 |
| R4-2204794 | Nokia, Nokia Shanghai Bell | Observation 1: There is not a single solution for all the evaluated cases. Depending on the allocation configuration, different filters (i.e., more or less aggressive) perform differently.  Observation 2: The required MPR depends on the filter, and there can be up to 1 dB difference in required MPR for different filters.  Observation 3: Current MPR regions could be used to define the MPR values.  Proposal 1: The MPR should be defined according to the filter requiring the largest MPR. |
| R4-2204795 | Nokia, Nokia Shanghai Bell | Observation 1:  The most aggressive filters have up to 0.6-0.8 dB loss with respect to the less aggressive filters in the small allocations  Observation 2: For allocation sizes ≤ 16 PRB, less aggressive filters perform better than aggressive filters in terms of achievable output power and link performance.  Observation 3: There is not a single solution for all the evaluated cases. Depending on the allocation configuration, different filters (i.e., more or less aggressive) perform differently.  Observation 4: Based on the previous agreement in RAN4#101bis-e [6], if spectrum flatness requirements are not tightened for small allocations, net gain cannot be guaranteed*.* |
| [R4-2204796](https://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_102-e/Docs/R4-2204796.zip) | Nokia, Nokia Shanghai Bell | Observation 1: Link loss due to more aggressive spectral shaping filtering is higher with small bandwidths.  Observation 2: For given number of PRBs, the performance difference between the used filters is quite similar for all the channel models. |
| R4-2204797 | Nokia, Nokia Shanghai Bell | Proposal 1: Due to practical considerations, the power boost should be limited to within 1dB.  Proposal 2: Discussion related to the percentage of maximum number of uplink transmission slots in a radio frame can be deprioritized in the current SI.  Proposal 3: Discussion related to further RB regions can be deprioritized in the current SI. |
| R4-2204937 | vivo | Proposal 1: For 1Tx PC2 PAs, the power boost should be limited to within 1dB. When the reference power of 0 dB MPR is 29dBm, the MPR value is more than 2dB. |
| [R4-2206139](https://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_102-e/Docs/R4-2206139.zip) | Skyworks Solutions Inc. | Observation 1: Practical considerations limit the maximum amount of power boosting to within 1dB above the PC2 0dB MPR power level for shaped Pi/2 BPSK waveforms. This corresponds to WF [1] option 1. Restrictions on the maximum number of uplink transmission slots is 25%.  Observation 4: 1dB boost may be supported with reasonable margins in the centred inner region triangle of width (1/3)NRB and summit (2/3)NRB. The inner triangle is illustrated in blue in Figure 4.  Proposal 1: Adopt the following new-inner, new-outer and edge allocation classification illustrated in Figure 6 for shaped Pi/2 BPSK PC2 and adopt maximum power reduction specifications with following text proposal.  “For UE power class 2, the allowed maximum power reduction (MPR) is defined in Table 6.2.2-2 for channel bandwidths ≤ 100 MHz.    Where the following parameters are defined to specify valid RB allocation ranges for Outer and Inner RB allocations:   * NRB is the maximum number of RBs for a given Channel bandwidth and sub-carrier spacing defined in Table 5.3.2-1; * RBStart,Low = Max(1, Floor(NRB/3 - LCRB/4);) and, * RBStart,High = NRB – RBStart,Low – LCRB.   where max() indicates the largest value of all arguments and floor(x) is the greatest integer less than or equal to x.  The RB allocation is an inner RB allocation if the following conditions are met:   * RBStart,Low ≤ RBStart ≤ RBStart,High AND and LCRB ≤ Ceil(2/3 NRB).   where Ceil(x) is the smallest integer greater than or equal to x.  An Edge RB allocation is one for which the RB(s) is (are) allocated at the lowermost or uppermost edge of the channel with LCRB ≤ 4 RBs.  The RB allocation is an Outer RB allocation for all other allocations which are not an Inner RB allocation or an Edge RB allocation.” |

## 1.2 Open issues summary

* + Topic #1-1: Power boost
  + Topic #1-2: MPR
  + Topic #1-3: General and workplan

### 1.2.1 Topic #1-1

*Topic description:* **Power boost**

**Issue 1-1-1:  *PC2 Power boosting above MPR0***

* Proposals
  + Option 1: For 1Tx PC2 PAs, the power boost should be limited to within 1dB. (R4-2204016, R4-2204085, R4-2204481, R4-2204797, R4-2204937, R4-2206139)
  + *Moderator WF: adopt option 1*

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| Company | Comments |
| Qualcomm | Support moderator WF |
| Nokia, NSB | Support moderator WF |
| Intel | We feel that the 1dB limit is overly pessimistic for the following reasons:  We don’t see high VSWR – While we agree that discrete Power Amplifiers are frequently tested at a 10:1 VSWR, as in R4-2204481, to account for real antenna impedance variations, this value does not match our agreed test setup. Our agreed test setup is for the PA to drive **4dB of attenuation** before reaching the antenna. Using the 4dB attenuator, if we sweep the antenna impedance at a 10:1 VSWR, the PA will only see a 1.97:1 VSWR which has significantly less variation upon device current and should not be a significant stress on the device. If we use data from R4-2202029 to extrapolate between 1dB/ 2dB with 12%/ 27% current increase respectively then we would expect 18% current increase with 1.5dB. Further adding current increase from 1.97:1 VSWR we believe this would still be an acceptable current increase. Therefor we propose a higher max power boost of 1.5dB as a reasonable compromise.    Not a data driven decision – We are not aware of any measurement data driving the 1dB limit. The recent Skyworks paper R4-2202029, with measurement results states in sec 2.2.1, that “practical considerations effectively restrict the maximum boosting that can be supported to 2dB maximum “.  Potential elimination of Pi/2BPSK SI value – If we limit the maximum Tx boost to 1dB and then additionally factor in the 0.5dB typical Rx loss (0.28 filter compared to no filter), this leads to a combined Tx+Rx link margin of only 0.5dB. With such small improvement, many companies will likely see no value in utilizing filtered Pi/2BPSK technology and this SI may conclude with no value added.  Based on these points, we propose a **compromise value of** **limiting power boost to 1.5dB**. |
| MediaTek | To Intel: VSWR 2:1 is too optimistic, even well matched PA output would easily exceed 2:1. Not only the 4dB front-end passive path loss, the phase/matching variation shall be considered also. Considering load-pull characteristics of PA, the optimized output impedance of PA is not matched to 50-ohm directly. For lower front-end loss device, it may be worse. With the reasons, nominal operation of PA loading impedance is set to VSWR=4:1 as rule of thumb. Plus there would be variation on passive matching components, usually 10~25%, and mass production process corner cases, we need to make sure PA can still alive under VSWR=10:1  We support moderator WF with above reasons. |
| OPPO | Support moderator WF |

**Issue 1-1-2:  *Uplink transmission slots***

* Proposals
  + Option 1: Limit UL slots in radio frame to max 25% to guarantee SAR compliance and to reduce strain on amplifier (R4-2203682, R4-2204085)
  + Option 2: Discussion related to the percentage of maximum number of uplink transmission slots in a radio frame can be deprioritized in the current SI (R4-2204797).
  + Option 3: Other, please detail

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| Company | Comments |
| Qualcomm | Option 2: Further discussion on this topic can be reserved for the WI phase where companies will have more time to investigate the thermal issues in greater detail. |
| Nokia, NSB | Option 2. |
| Intel | Option 2 |
| OPPO | Ok with Option 2. |
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**Issue 1-1-3:  *Power boost for PC2 with dual TX***

* Proposals
  + Option 1: Further study the power boosting requirements for PC2 with dual Tx. More measurements are needed. This can be done in the study phase of the future WI, or the SI is extended by one quarter, which can be discussed in RAN#95-e. (R4-2204085)
  + Option 2: Other, please detail

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| Company | Comments |
| Qualcomm | Option 2: It can be further discussed in the WI if it is deemed we need different requirements for 2 Tx. |
| Nokia, NSB | Option 2: Power boosting requirements for PC2 with dual Tx is deprioritized in the current SI. Dual Tx is not a coverage bottleneck because it can benefit from precoding gain. |
| Intel | Option 2: If there is a WI approved, we can explore further if needed. |
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### 1.2.2 Topic #1-2

*Topic description:* **MPR**

**Issue 1-2-1:  *MPR tables for various power boosts***

* Proposals
  + Option 1: In case the maximum power boost would be set to 1.5dB use MPR provided in Table 6 (R4-2203682)

Table

Description automatically generated

* + Option 2: In case the maximum power boost would be set to 1.0dB use MPR provided in Table 7 (R4-2203682)

Table

Description automatically generated

* + Option 3: Define the MPR requirements of Pi/2 BPSK for PC2 1Tx as in Table 1 (R4-2204085)

Table

Description automatically generated

* + Option 4: For UE power class 2, the allowed maximum power reduction (MPR) is defined in Table 6.2.2-2 for channel bandwidths ≤ 100 MHz. (R4-2206139)

Table

Description automatically generated

* + Option 5: Update MPR tables (at least Table 6.2.2-2) in TS 38.101-1. Reclassification of RB regions for MPR shall be postponed to Rel-18 (R4-2204481)
  + Option 6: The MPR should be defined according to the filter requiring the largest MPR (R4-2204794)
  + Option 7: Other, please detail

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| Company | Comments |
| Qualcomm | Option 7: The primary issue is to first agree on a maximum power boost value. Based on this value it can be decided in the WI phase whether it is more appropriate to update the existing MPR tables or redefine the current MPR regions and what MPRs to assign for each region. |
| Nokia, NSB | Option 6 and Option 7.  Option 7: define the MPR values in the WI  Based on our results different filters (i.e., more or less aggressive) perform differently depending on the allocation configuration. This means that required MPR depends on the filter, and there can be up to 1 dB difference in required MPR for different filters.  Due to practical considerations, we define maximum achievable power boost based on filter requiring the largest MPR. This will ensure sufficient flexibility for UE to select filter according to UE implementation and/or according to filter optimizing the net gain.  Based on our results, the maximum power boost   * It’s the biggest in inner RB allocations * It’s always at least 1dB.   For some channel bandwidths, it can be up-to ~1.5 dB. |
| Intel | Option 1 or Option 7, agree with QC, Nokia to first agree on maximum power boost and revisit MPR in a potential WI phase.  We think that at a minimum the proposed MPR should target to be 1.5dB better than the existing MPR for DFT-S-OFDM QPSK to show benefit over QPSK with the 0.5dB Rx implementation loss. For DFT-S-OFDM QPSK PC2 MPR is ≤1dB outer and 0dB inner with MPR0=26Bm. For filtered Pi/2BPSK a 1.5dB improvement would require ≤2.5dB outer and ≤1.5dB inner for MPR0=29dBm. We would prefer to further evaluate realistic MPR levels in a potential WI phase. |
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### 1.2.3 Topic #1-3

*Sub-topic description:* **General and workplan**

**Issue 1-3-1: *TP detailing company contributions from RAN4#101-bis-e for TR on optimization of pi/2 BPSK uplink power in NR (R4-2204013)***

* Proposals
  + Option 1: TP is agreeable.
  + Option 2: Needs further updating

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| Company | Comments |
| Qualcomm | Option 1 |
| Nokia, NSB | Option 1 |
| Intel | Option 1 |
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**Issue 1-3-2: *TP containing additional data and modification of previous data from Intel for TR on optimization of pi/2 BPSK uplink power in NR (R4-2204414)***

* Proposals
  + Option 1: TP is agreeable.
  + Option 2: Needs further updating

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| Company | Comments |
| Qualcomm | Option 1 |
| Nokia, NSB | Option 1 |
| Intel | Option 1 |
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**Issue 1-3-3: Latest revision of *TR on optimization of pi/2 BPSK uplink power in NR (R4-2204012)***

* Proposals
  + Option 1: TR on optimization of pi/2 BPSK uplink power is agreeable.
  + Option 2: Needs further updating

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| Company | Comments |
| Qualcomm | Option 1 |
| Nokia, NSB | Option 1 |
| Intel | Option 1 |
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## 1.3 Companies views’ collection for 1st round

### 1.3.1 CRs/TPs comments collection

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| **CR/TP number** | **Comments collection** |
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## 1.4 Summary for 1st round

### 1.4.1 Open issues

*Moderator tries to summarize discussion status for 1st round, list all the identified open issues and tentative agreements or candidate options and suggestion for 2nd round i.e. WF assignment.*

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## 1.5 Discussion on 2nd round

### 1.5.1 Open issues

RAN4 will further discuss based on the WF and revised TRs/CRs in 2nd round.

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| **T-doc number** | **Company** | **Comments** |
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# 2 Recommendations for Tdocs

1st round

**New tdocs**

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| --- | --- | --- |
| **Title** | **Source** | **Comments** |
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| LS on … | ZZZ | To: RAN\_X; Cc: RAN\_Y |
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**Existing tdocs**

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| **Tdoc number** | **Title** | **Source** | **Recommendation** | **Comments** |
| [**R4-2203682**](https://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_102-e/Docs/R4-2203682.zip) | PI/2 BPSK enhancements | Apple |  |  |
| [**R4-2204012**](https://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_102-e/Docs/R4-2204012.zip) | TR skeleton for SI on optimizations of pi\_2 BPSK uplink power | Qualcomm Incorporated |  |  |
| [**R4-2204013**](https://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_102-e/Docs/R4-2204013.zip) | TP for Pi/2 BPSK study item for TR38.868 | Qualcomm Incorporated |  |  |
| [**R4-2204016**](https://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_102-e/Docs/R4-2204016.zip) | PC2 power boost for Pi/2 BPSK | Qualcomm Incorporated |  |  |
| [**R4-2204085**](https://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_102-e/Docs/R4-2204085.zip) | On Remaining Issues for Optimisations of Pi/2 BPSK UL Power | Huawei, HiSilicon |  |  |
| [**R4-2204414**](https://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_102-e/Docs/R4-2204414.zip) | TP for TR 38.868: Filter Analysis Update | Intel Corporation |  |  |
| [**R4-2204415**](https://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_102-e/Docs/R4-2204415.zip) | Views on Tx+Rx link margin filter delta | Intel Corporation |  |  |
| [**R4-2204481**](https://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_102-e/Docs/R4-2204481.zip) | Discussion on Pi\_2\_BPSK power boosting | MediaTek Inc. |  |  |
| [**R4-2204794**](https://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_102-e/Docs/R4-2204794.zip) | Transmitter performance for pi/2 BPSK with spectral shaping | Nokia, Nokia Shanghai Bell |  |  |
| [**R4-2204795**](https://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_102-e/Docs/R4-2204795.zip) | Shaping filter characteristics including transmitter and link performance | Nokia, Nokia Shanghai Bell |  |  |
| [**R4-2204796**](https://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_102-e/Docs/R4-2204796.zip) | Receiver performance for pi/2 BPSK with spectral shaping | Nokia, Nokia Shanghai Bell |  |  |
| [**R4-2204797**](https://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_102-e/Docs/R4-2204797.zip) | Identify?potential changes for?RAN4 requirements | Nokia, Nokia Shanghai Bell |  |  |
| [**R4-2204937**](https://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_102-e/Docs/R4-2204937.zip) | Further discussion on pi/2 BPSK UE Tx power | vivo |  |  |
| [**R4-2206139**](https://www.3gpp.org/ftp/TSG_RAN/WG4_Radio/TSGR4_102-e/Docs/R4-2206139.zip) | MPR Proposal for PC2 Pi\_2 BPSK | Skyworks Solutions Inc. |  |  |

Notes:

1. Please include the summary of recommendations for all tdocs across all sub-topics incl. existing and new tdocs.
2. For the Recommendation column please include one of the following:
   1. CRs/TPs: Agreeable, Revised, Merged, Postponed, Not Pursued
   2. Other documents: Agreeable, Revised, Noted
3. For new LS documents, please include information on To/Cc WGs in the comments column
4. Do not include hyper-links in the documents

2nd round

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| **Tdoc number** | **Title** | **Source** | **Recommendation** | **Comments** |
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Notes:

1. Please include the summary of recommendations for all tdocs across all sub-topics.
2. For the Recommendation column please include one of the following:
   1. CRs/TPs: Agreeable, Revised, Merged, Postponed, Not Pursued
   2. Other documents: Agreeable, Revised, Noted
3. Do not include hyper-links in the documents