Agenda Item	
Source:	Motorola
Title:	Simulation results for UE downlink performance requirements
Document for	Discussion

## 1.0 Introduction

This paper provides link level simulation results in order to specify the performance requirements for Section 8 of TS25.101. Results are provided for the demodulation of the Dedicated Channel (DCH) in the static environment and the multi-path fading propagation conditions (Case 1/2/3) for 12.2 kbps, 64 Kbps, 144 Kbps and 384 Kbps

## 2.0 Simulation assumptions.

Simulation assumptions are listed in Annex A for reference and are inline with the agreed assumption in WG4#7 and the AH01 meeting in Noordwijkerhout.

#### **3.0** Simulation results

Results are plotted for both the BLER and BER for the agreed values of Ior/Ioc.These results for the DCH\_ Ec/Ior (dB at the agreed BLER rate and Ior/Ioc are summarised below for clarity. These results do not include any implementation margin which is for discussion in WG4. Some simulations for the 384 kbps information rate are in progress and will be provided during the meeting

Information rate	Static (AWGN)		Multi-path Case 1		Multi-path Case 2		Multi-Path Case 3			
	BLER	BLER	BLER	BLER	BLER	BLER	BLER	BLER	BLER	
	@E-1	@E-2	@E-1	@E-2	@E-1	@E-2	@E-1	@E-2	@E-3	
12.2 kbps	Ior/Ioc = -1 dB		Ior/Ioc = 9 dB		Ior/Ioc = -3 dB		Ior/Ioc = -3 dB			
DCH_Ec/Ior (dB)	-19.6	-18.6	-21.3	-17.6	-14.2	-10.8	-15.9	-14.8	-14.0	
64 kbps	Ior/Ioc	Ior/Ioc = -1 dB		Ior/Ioc = 9 dB		Ior/Ioc = -3 dB		Ior/Ioc = -3 dB		
DCH_Ec/Ior (dB)	-15.0	-14.8	-16.4	-12.5	-9.2	-5.7	-11.2	-10.5	-10.0	
144 kbps	Ior/Ioc = -1 dB		Ior/Ioc = 9 dB		Ior/Ioc = +3 dB		Ior/Ioc = +3 dB			
DCH_Ec/Ior (dB)	-11.9	-11.8	-13.10	-9.40	-10.8	-7.9	-12.10	-11.6	-11.2	
384 kbps	Ior/Ioc	Ioc = -1 dB $Ior/Ioc = 9 dB$		c = 9 dB	Ior/Ioc = +6 dB		Ior/Ioc = +6 dB		dB	
DCH Ec/Ior (dB)	-7.8	-7.7	-8.8	-5.0	-8.3	-6.0	-9.2			

# 4.0 Conclusion

In this document simulation results are presented for the UE performance test for section 8 of TS 25.101. Based on these results implementation margin would need to be considered for each test case in order to derive the values for the specification.







































# Annex A Simulation assumptions

Simulation assumptions are presented in Table 1

Parameter	Explanation/Assumption							
Chip Rate	3.84 Mcps							
Closed loop Power Control	OFF							
AGC	OFF							
Channel Estimation	Ideal							
Number of samples per chip	1							
Propagation Conditions	As specified in Annex B of TS 25.101 v.3.0.0.							
Number of bits in AD converter	Floating point simulations							
Number of Rake Fingers	Equals to number of taps in propagation condition models							
Downlink Physical Channels	$CPICHP\_Ec/Ior = -10 \text{ dB}$							
	PCCPCH_Ec/Ior = -12 dB							
	SCH_Ec/Ior	= - 1	= -12 dB					
and rower Levels		(Co	(Combined energy of Primary and Secondary SCH)					
	PICH_Ec/Ior	= - 1	= -15 dB					
	OCNS_Ec/Ior	$\begin{array}{c} = P \\ \text{to } 1 \end{array}$	= Power needed to get total power spectral density ( to 1.					
	DPCH_Ec/Ior	= p	= power needed to get meet the required BLER target					
BLER target	Thus results for BER / BLER from 0.5 to 10-3 are presented							
BLER calculation	BLER has been calculated by comparing with transmitted and received bits.							
PCCPCH model	Random symbols transmitted, ignored in a receiver							
PICH model	Random symbols transmitted, ignored in a receiver							
DCCH model	Random symbols transmitted, ignored in a receiver							
TFCI model	Random symbols, ignored in a receiver but it is assumed that receiver gets error free reception of TFCI information.							
Used OVSF and scrambling codes	Codes are chosen from the allowed set.							
	Information	Static	Multi-path			Moving	Birth /	
	data rate		Case1	Case 2	Case 3		death	
$\hat{I}_{or} / I_{oc}$ values	12.2 kbps	-1	9	-3	-3			
	64 kbps	-1	9	-3	-3			
	144 kbps	-1	9	+3	+3			
	384 kbps	-1	9	+6	+6			
Turbo decoding	MaxLogMap algorithm is used with 8 iterations							
SCH position	Offset between SCH and DPCH is zero chips meaning that SCH is overlapping with the first symbols in DPCH in the beginning of DPCH slot structure							
Measurement Channels	As specified in Annex A of TS 25.101 v3.0.0							

Table	1.	Simulation	assumptions
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