**3GPP TSG RAN WG1 Meeting #101-E R1-** **200xxxx**

**e-Meeting, May 25th – June 5th, 2020**

**Source: Moderator (Intel Corporation)**

**Title: Discussion #1 [101-e-NR-5G\_V2X\_NRSL-Mode-2-01]**

**Agenda item: 7.2.4.2.2**

**Document for:** **Discussion and Decision**

Introduction

This contribution provides discussion on critical issues for the first thread [101-e-NR-5G\_V2X\_NRSL-Mode-2-01].

[101-e-NR-5G\_V2X\_NRSL-Mode-2-01] Email discussion/approval with respect to processing times:

1a – Values for Tproc,0, Tproc,1, T3

1b – Sensing window size values in brackets

By 5/29, with potential TPs till 6/4 – Sergey (Intel)

Discussion

## Processing times

In order to facilitate decision, the discussion is split into several aspects.

First, although it is observed that majority of contributions proposes processing time values in slots, it is worth confirming that processing time values are further discussed in slots or in symbols / absolute time.

**Q1: Whether the processing time values are specified in slots or in absolute time using symbol level granularity?**

|  |  |  |
| --- | --- | --- |
| **Source** | **Short answer: in slots or in symbols/absolute time** | **Comments** |
| Intel | slots | Simple option consistent with LTE.  Other options are enhancements. Position of sidelink transmission does not change within slot and therefore no big value to use symbols. |
| Qualcomm | Either is workable | In either case, RAN1 needs to take care of slot boundary alignment. In specifications, a value of 0 means same slot as trigger (e.g. DCI and K0) and a value of 1 means the slot immediately after trigger. |
| Huawei/HiSilicon | In slots | Slot is the scheduling unit for NR-V2X.  Using symbol level granularity has no prominent benefits, but is complicated since we need to further consider slot boundary.  For reference, the congestion control processing time is also specified in slots (see clause 8.1.6 of TS 38.214). |
| Samsung | In slots | We share view with Intel and HW. |
| NTT DOCOMO | Slots | We share view with Intel and HW. |
| vivo | slots | We share view with Intel and HW |
| CATT | In physical slots. | Slot has been determined as the time-domain granularity for SL resource. The processing time is related to absolute time so it should not be defined in terms of logical slots. Therefore, we support that processing time values are specified in physical slots, considering processing time and slot boundary alignment. |
| Ericsson | Slots | All SL is slot based and there is no interaction with Uu |
| TCL | Slots | We share view with Intel and HW. Physical slots should be considered. |
| ZTE, Sanechips | Slot. |  |
| Apple | Slots | Since SL is based on slots, it is preferred to specify it in slots. |
| Nokia, NSB | slot |  |
| FUTUREWEI | slots | Both could work, but slot is cleaner |
| OPPO | Physical slots |  |
| NEC | Slot |  |
| LG Electronics | In slots | No strong benefit by defining the processing time value as a unit of symbols/absolute time |
| MediaTek | slots |  |

Second, many contributions assume there is relation between Tproc,0, Tproc,1 and T3. For example, T3 = Tproc,0 + Tproc,1 T3 = Tproc,1.

**Q2: Is there any relation between Tproc,0, Tproc,1 and T3? If yes, please specify.**

|  |  |  |
| --- | --- | --- |
| **Source** | **Short answer** | **Comments** |
| Intel | Yes | * Tproc,0 = 1 slot * Tproc,1 = T3 measured in slots and defined by the following table below |
| Qualcomm | No | T3 contains operations from both Tproc,0 and Tproc,1 and the sum of the two is a reasonable upper bound to use for T3. However, they should be defined independently, in line with their current use in specifications. |
| Huawei/HiSilicon | Support T3=T1 | If T3 is too large, the UE may miss the SCIs during time interval (m-T3, m) that cause collision, since UE may choose not to do re-evaluation during this time interval.  If T3 is too small, the re-selection window will be later than [m, m+T2-T1] and the reselected resource will be later than m, thus increasing latency.  T3=T1 is a good trade-off that can provide a large sensing range, and ensure the re-selection window is no later than [m, m+T2-T1]. |
| Samsung | Yes | T3 is T1 +1 slots where T1 is the selected processing time for resource selection by UE within upper bound Tproc,1. |
| Vivo | Yes | T3 is the processing time of resource selection, it should be no larger than T1. For simplicity, it is fine to set T3= Tproc,1 considering T1 is determined by implementation. |
| CATT | Yes.  T3 = Tproc,0 + Tproc,1 | Tproc,0 is related the sensing results preparation procedures including at least PSCCH decoding and SL-RSRP.  Tproc,1 is related resource (re)selection and transmission preparation procedures including PSCCH preparation and PSSCH preparation.  For T3, in order to ensure the re-evaluation and pre-emption performance, all the sensing results before m-T3 should be available. Then procedures within T3 should contain the sensing results preparation, potential resource reselection and PSCCH and PSSCH transmission preparation.  Therefore, we support T3 = Tproc,0 + Tproc,1. |
| Ericsson | T3 = Tproc,0 + 1  Tproc,1 is not related | T3 and Tproc,0 represent the same concept: the time that is necessary for decoding the transmissions received in one slot. However, there is a slight difference in how they are defined (a difference equivalent to using > or ≥) and 1 slot has to be added.  Tproc,1 is a preparation time not a processing time.  Regardless of the relationship between them, we think that it will be simplest to define them independently. |
| TCL | T3 = Tproc,0 + 1  or T3 = Tproc,0 + Tproc,1 | This allows the UE to process and understand whether reselection is needed. Timing for reselection can be applied separately.  Or, if we want to include a reselection without increasing latency, we need both decoding processing time and scheduling processing time. |
| Apple | T3 = Tproc,0 + Tproc,1 | The processing time T3 should include UE processing time of SCI decoding and sidelink measurement, as well as the resource selection procedure and PSCCH/PSSCH preparation time. |
| FUTUREWEI | Not necessarily | In our view, the restrictions on T3 is that it should be larger than Tproc, 0 and lower than T1. From our perspective, any value that works is acceptable. While we don’t see the need to link these parameters, we can accept such a decision if the group leans this way |
| OPPO | T3 = Tproc,0 + Tproc,1 | For T3, it is related to the case where a UE has detected one or more of its pre-selected or already reserved resources been indicated/pre-empted by another UE, and the UE is triggered to perform reselection of the affected resource(s). In our view, it is no different to the case where L1 receives a packet TB from the upper layer and needs to perform Step 1 and Step 2. As such, T3 should be equal to Tproc,0 + Tproc,1. |
| NEC | Yes, T3 = Tproc,0 + Tproc,1 | T3 should contains SCI decoding + measurement time and resource selection + PSCCH/PSSHC preparation time. |
| LG Electronics | Yes | T3 = Tproc,0 + Tproc,1 +1 |
| MediaTek | Yes  T3 = Tproc,0 + Tproc,1 | T3 processing operation includes both measurements and resource (re)-selection operations. T3 should be a combination of Tproc,0 and Tproc,1. |

Some contributions consider that there is no need to define Tproc,0 and Tproc,1 separately and it may be sufficient to keep a single value which absorbs both SCI processing / measurement time and resource selection + PSCCH/PSSHC preparation time.

**Q3: Is it necessary to introduce both Tproc,0 and Tproc,1, or one of the values is sufficient?**

|  |  |  |
| --- | --- | --- |
| **Source** | **Short answer** | **Comments** |
| Intel | No, it is not necessary | Only sum matters, therefore single value is enough |
| Qualcomm | Yes | Tproc,0 and Tproc,1 correspond to different aspects and functions and there could be tests for one value, independently of the other. This is also in line with current specifications. |
| Panasonic | No | We agree Intel. |
| Huawei/HiSilicon | Define Tproc,0 and Tproc,1 separately | is associated with the UE processing time on decoding the SCI and RSRP measurement.  corresponds to the scheduling time and the data preparation time (channel coding, QAM modulation, RE mapping and OFDM baseband signalling generation). It includes both MAC and PHY processing.  The UE operations accounted for by and are quite different, and thus have to be defined separately. Defining them together would force them both to be dimensioned for the lengthier set of processing, which would be unnecessary. |
| Samsung | Define Tproc,0 and Tproc,1 separately | Two processing times Tproc,0 and Tproc,1 are efinitely having different purpose as HW commented |
| NTT DOCOMO | No | We share view with Intel. |
| Vivo | Define Tproc,0 and Tproc,1 separately | One is corresponding to sensing window, the other is for selection window. Therefore, should be separated defined as in LTE. |
| CATT | Yes, it is necessary to introduce both Tproc,0 and Tproc,1. | Firstly, the procedures related to T\_(proc,0) and T\_(proc,1) are different.  Secondly, Tproc,0 is used to determine the sensing window and Tproc,1 is used to determine the maximum value of T1. |
| Ericsson | Both | See the answer to Q2 |
| TCL | Define Tproc,0 and Tproc,1 separately | Agree with Intel/HW. |
| ZTE, Sanechips | Define Tproc,0 and Tproc,1 separately | is up to UE implementation. |
| Apple | Yes, define Tproc,0 and Tproc,1 separately | Tproc,0 is considered as UE processing time of SCI decoding and sidelink measurement. This value is used to define sensing window.  Tproc,1 is considered as resource selection and PSCCH/PSSCH preparation processing time, and this value is used as a boundary of the resource selection window.  It is preferred to define them separately so as to clarify the sensing window and resource selection window separately. |
| Nokia, NSB | Yes, define them separately |  |
| FUTUREWEI | Separate definition |  |
| OPPO | Define Tproc,0 and Tproc,1 separately | Since these two UE processing times are relating to different operations and they are used for different purposes, it would actually be more confusing if they are combined and we can no longer distinguish between them in the spec. |
| NEC | Separately | Separately define for different meanings. |
| LG | Define Tproc,0 and Tproc,1 separately | Not technically convinced to have a same value for Tproc,0 and Tproc,1 since each value targets different processing operations. |
| MediaTek | Yes, define Tproc,0 and Tproc,1 separately |  |

Finally, based on all the above answers, the concrete values for Tproc,0, Tproc,1, and T3 are discussed in Q4a and Q4b.

**Q4a: If in Q1 your answer is “in slots”, please fill the following table, where for each processing time four values need to be provided:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Source** | **Tproc,0**  **{15, 30, 60, 120} kHz** | **Tproc,1**  **{15, 30, 60, 120} kHz** | **T3**  **{15, 30, 60, 120} kHz** | **Comments** |
| Intel | Tproc,0 is not specified | {3,3,4,5} | {3,3,4,5} | Sensing window [n –T0, n – Tproc,0] is replaced by sensing window  [n –T0, n – 1] (same as in LTE) |
| Qualcomm | 1/1/2/4 | 2/3/5/9 | 3/4/7/13 | It is very important to balance the values. Very small values increase implementation complexity.  If the values are too relaxed, the UE would be discarding substantial amount of sensing information. For example, 4ms in 60 kHz is 16 slots, half of W, which means that 50% of sensing information is not used. Large values would additionally degrade system performance because a UE is not reacting quickly (for any SCS).  For Tproc,0 the specification uses , which handles slots boundary.  This is not the case for Tproc,1 and our proposed values account for this. (2 is 1 full slot + time to align to next slot boundary) |
| Huawei/HiSilicon | 1/1/2/2 slots | *3 ms for all SCS, i.e. 3, 6, 12, 24 slots* | T3=T1 | is associated with the UE processing time on decoding the SCI and RSRP measurement. 1/1/2/2 slots are reasonable values.  consists of a “fixed” part and a “variable” part as follows:   * “Fixed” part: scheduling time. When the MAC PDU comes to physical layer, the following steps are needed:   + Physical layer needs to prepare the sensing results and report these results to MAC layer.   + MAC layer makes decision on how and which resource will be allocated.   + MAC layer indicates the scheduling results to the physical layer.   + Note: The scheduling time will be larger for aperiodic traffic since the TB size is not known in advance, so the UE needs to reschedule the potential Tx resource.   + Note: The scheduling time is a “fixed” value since it relates to MAC scheduling, MAC-PHY exchange, etc., and is independent of the value of SCS. 2 ms is proposed for this “fixed” part. * “Variable” part: data preparation time   + Including channel coding, QAM modulation, RE mapping and OFDM baseband signalling generation   + Note: The data preparation time is mainly about PHY processing, and is a “variable” that is highly dependent on UE capability now and in the future. And since the spec already allows any UE can go faster than , this “variable” part just needs to be an upper bound. 1 ms is proposed for this “variable” part.   In summary, 3 ms (2 ms + 1 ms) is proposed for for all SCS. |
| Samsung | 1/1/{1,2}/{1,2} | 4/8/16/32 | T3=T1+1 | - Tproc,0 is defined as 1 slot for SCS {15, 30}kHz and (pre-)configured between {1, 2} slots for SCS {60, 120} kHz. (One slot for *Tproc,0* may not be enough for larger SCS. Therefore, two slots for *Tproc,0* can be considered for larger SCS such as 60 kHz and 120 kHz.)  - Tproc,1­ defined as physical slots. (In LTE V2X, *Tproc,1* was defined as 4 subframes. In NR V2X, we can use this value. Since selection of *T1* is up to UE implementation subject to *T1 ≤ Tproc,1*, the fixed 4ms for *Tproc,1* is reasonable)  - T3 is T1 +1 slots where T1 is the selected processing time for resource selection by UE within upper bound Tproc,1. (T3 value should be decided considering required time for implementation related to re-evaluation procedure. Specifically, T3­ is the processing time related to resource re-selection after re-evaluation. Besides to resource selection time, T3­ needs to consider additional processing time for dropping previously reserved resource(s) as well as overlapping between previously reserved resource(s) and newly selected resource(s). Considering this aspect, 1 slot is added into T1 for T3­) |
| CATT | 1/1/2/2 physical slots | physical slots | physical slots | For Tproc,0, at least one slot is needed considering the processing time and slot boundary alignment. For the larger SCS of 60KHz and 120KHz, one additional physical slot should be introduced to ensure the sufficient processing time.  For Tproc,1, it corresponds to the LTE-V2X procedures within T\_1 (up to 4ms) with excluding the processing time of PSCCH decoding and SL measurements, which is . Note that Tproc,1 is a maximum value for T1, UE with stronger capability can determine a smaller T1 by its implementation. |
| Ericsson | {1,1,2,2} slots | {2,2,3,4} slots | Tproc,0 + 1 slots | Tproc,1 add 1 slot with respect to PUSCH times because the selection window is defined as [n+T1, n+T2]. |
| TCL | 1,1,2,2 |  | Tproc,0 + Tproc,1 | Tproc,1 should be an absolute time value as it is a fixed processing/scheduling time. 3 or 4ms is open for us. |
| ZTE, Sanechips | is up to UE implementation. | {3,3,4,5} | {3,3,4,5} |  |
| Apple | 1 for {15, 30} kHz;  2 for {60, 120} kHz | UE cap. 1:  2/2/4/8 slots for 15/30/60/120 kHz;  UE cap. 2:  2/4/8/16 slots for 15/30/60/120 kHz; | UE cap. 1:  3/3/6/10 slots for 15/30/60/120 kHz  UE cap. 2:  3/5/10/18 slots for 15/30/60/120 kHz | Since Tproc,1 serves as an upper bound of T1, it should be large enough to allow UE to finish CR/CBR evaluation.  Since CR/CBR processing time is based on UE capability, Tproc,1  and T3 are also based on UE capability. |
| Nokia, NSB | 1,1,2,2 | 2,2,3,4 | 3,3,5,6 |  |
| FUTUREWEI | 1 ,1, 2, 2 | 1, 1, 2, 3 | 2, 2, 4, 5 |  |
| MediaTek | {1, 1, 2, 2} slots | {3,7,14,30} slots | {4, 8, 16, 32} slots | SCI decoding, RSRP measurements, and (re)-selection procedures in total should be given 4ms as upper bound. This value is also in line with LTE V2X procedures.  UE can choose a smaller T1 value as it is up to UE implementation. In our view, 4ms is a large enough time to accommodate as an upper bound for processing times. |

**Q4b: If in Q1 your answer is “in symbols”, please fill the following table, where for each processing time four values need to be provided:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Source** | **Tproc,0 for**  **{15, 30, 60, 120} kHz** | **Tproc,1 for**  **{15, 30, 60, 120} kHz** | **T3 for**  **{15, 30, 60, 120} kHz** | **Comments** |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |

**Q5: Any other important aspects you would like to highlight with respect to processing times, e.g. necessity to introduce more than one capability, or FR1 vs FR2 differentiation.**

|  |  |
| --- | --- |
| **Source** | **Comments** |
| Intel | Single capability is enough. |
| Qualcomm | No need to introduce two capabilities. FR1 vs. FR2 is accounted for by using SCS-dependent values. |
| Panasonic | We agree Qualcomm that FR1 vs. FR2 is accounted for by using SCS-dependent values. |
| NTT DOCOMO | Agree with QC. |
| Vivo | No need |
| CATT | No need to introduce more than one capability. |
| Ericsson | No need |
| TCL | Agree with QC. |
| ZTE, Sanechips | Only one capability is sufficient. |
| Apple | Since we already introduced UE capability of CR/CBR evaluation, it is preferred to introduce UE capability of the processing times. |
| OPPO | Agree with QC |
| LG Electronics | Not necessary to define multiple capabilities |
| MediaTek | Agree with QC. |

From answers on Q1-Q3, Q5, the following conclusion can be drawn:

**Conclusion**

* Tproc,0, Tproc,1 and T3 are defined in slots
* All three values are defined in specification
* Single capability is defined for each processing time

For Tproc,0 which has the meaning of performing PSCCH decoding and RSRP measurements, the majority proposes values {1,1,2,2}.

Proposal 1-1

* Tproc,0 is {1, 1, 2, 2} slots for {15, 30, 60, 120} kHz sub-carrier spacing respectively

3,3,4,5 – Intel, ZTE/Sanechips

2,3,5,9 – Qualcomm

3,6,12,24 – HW/HiSi, TCL

4,8,16,32 – Samsung, [TCL]

3,7,14,30 – CATT

2,2,3,4 – Ericsson, Nokia/NSB

2,2[4],4[8],8[16] – Apple

1,1,2,3 – Futurewei

3,7,14,30 – MediaTek

Since Tproc,1 is mainly dominated by computation time independent of the numerology, i.e. resource selection and physical channel preparation, it needs to be almost unchanged in terms of absolute time. It would be reasonable to adopt around 2 ms total Tproc,1 time.

That results in {2, 4, 8, 16} slots. Comparing to e.g. numbers resulting from averaging of companies’ proposals, that is {3, 5, 8, 15}, it may be a reasonable choice.

Proposal 1-2

* Tproc,1 is {2, 4, 8, 16} slots for {15, 30, 60, 120} kHz sub-carrier spacing respectively

For T3, the decision seems dependent on Tproc,1. In FL understanding, T3 has the same meaning and component as Tproc,1 but may require consideration on slot boundary alignment. In other words, the re-evaluation or pre-emption trigger is identical to resource selection trigger ‘n’.

Proposal 1-3

* Down-select this meeting:
  + Option 1: T3 = Tproc,1
  + Option 2: T3 = Tproc,1 + 1

## Sensing window size

There are currently brackets around sensing window size values:

|  |
| --- |
| Agreement from RAN1#99:   * T0 is (pre)-configured between: 1000+[100]ms and [100]ms |

RAN1 RRC parameters list contains the following entry:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 5G\_V2X\_NRSL-Core | Resource allocation Mode 2 |  |  |  |  | t0\_SensingWindow | new | t0\_SensingWindow | Parameter that indicates the start of the sensing window | [100] ms, 1000+[100] ms |  | Per resource pool | UE specific, Cell specific | 36.331, 38.331 |  |

In order to finalize this aspect, it is proposed to simply confirm the values in brackets:

**Q6: Is it OK to confirm the values in brackets, so that the agreement becomes the following?**

* T0 is (pre)-configured between: 1000+~~[~~100~~]~~ms and ~~[~~100~~]~~ ms

|  |  |
| --- | --- |
| **Source** | **Comments** |
| Intel | Remove brackets |
| Qualcomm | Remove brackets |
| Panasonic | We agree to remove brackets. |
| Huawei/HiSilicon | Ok to confirm the values in brackets, i.e., remove brackets. |
| Samsung | Our preference is that T0 is (pre-)configured between 1000ms and 100ms.  In our understanding, there is no motivation to add another 100ms for T0 =1000ms |
| NTT DOCOMO | For shorter one, support to remove bracket.  For larger one. Either to remove or not is ok. We are also wondering what the motivation to add 100ms for T0=1000ms. |
| vivo | How 1100ms comes should be clarified before remove the brackets. |
| CATT | Remove brackets |
| Ericsson | Remove brackets |
| TCL | Agree to remove brackets. |
| ZTE, Sanechips | Ok to confirm. |
| Apple | Confirm the values in brackets. |
| Nokia, NSB | Confirm. |
| FUTUREWEI | Confirm |
| OPPO | Remove brackets |
| NEC | Confirm 1000+100 ms and 100ms |
| LG Electronics | Fine to confirm |
| MediaTek | OK to confirm |

It seems majority view is to confirm the values in brackets:

Proposal 1-4

* Confirm that sensing window size parameter T0 is (pre)-configured between two values: 1100 ms and 100 ms

References

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3. [R1-2003495](file:///C:\Users\wanshic\OneDrive%20-%20Qualcomm\Documents\Standards\3GPP%20Standards\Meeting%20Documents\TSGR1_101\Docs\R1-2003495.zip) Remaining details of sidelink resource allocation mode 2 Huawei, HiSilicon
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13. [R1-2003874](file:///C:\Users\wanshic\OneDrive%20-%20Qualcomm\Documents\Standards\3GPP%20Standards\Meeting%20Documents\TSGR1_101\Docs\R1-2003874.zip) On Mode 2 for NR Sidelink Samsung
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22. [R1-2004385](file:///C:\Users\wanshic\OneDrive%20-%20Qualcomm\Documents\Standards\3GPP%20Standards\Meeting%20Documents\TSGR1_101\Docs\R1-2004385.zip) Remaining issues on resource allocation mechanism mode 2 NTT DOCOMO, INC.
23. [R1-2004452](file:///C:\Users\wanshic\OneDrive%20-%20Qualcomm\Documents\Standards\3GPP%20Standards\Meeting%20Documents\TSGR1_101\Docs\R1-2004452.zip) Sidelink Resource Allocation Mode 2 Qualcomm Incorporated
24. [R1-2004531](file:///C:\Users\wanshic\OneDrive%20-%20Qualcomm\Documents\Standards\3GPP%20Standards\Meeting%20Documents\TSGR1_101\Docs\R1-2004531.zip) Remain details on mode-2 resource allocation for NR V2X ITL
25. [R1-2004544](file:///C:\Users\wanshic\OneDrive%20-%20Qualcomm\Documents\Standards\3GPP%20Standards\Meeting%20Documents\TSGR1_101\Docs\R1-2004544.zip) Resource allocation Mode 2 for NR SL Ericsson