**3GPP TSG RAN WG1 Meeting #100bis R1-200xxxx**

e-Meeting, April 20th – 30th, 2020

Source: CATT

Title: Draft Feature lead summary on AI 7.2.4.3 #2 Sidelink synchronization mechanism

Agenda Item: 7.2.4.3

Document for: Discussion and Decision

# Introduction

According to the timelines of the chairman’s guideline on feature lead summary, it can be referred as:

* Preparation phase (4/13-4/17):
* 4/13-4/14: Feature leads to summarize critical issues for each sub-agenda.
* 4/15-4/17: Email discussion to finalize the set of issues for each sub-agenda. Before 4/20, all critical issues (up to 4 threads) will be identified, and a revised feature lead summary on sidelink synchronization will be submitted in R1-2002396.
* Official email discussion/approval phase (4/20-4/30):
* 4/20-4/30: e-meeting.
* Deadline time reference: UTC 11:59pm
* Same as before (PSDT 4:59pm)
* Quiet Period
* 44 Hours: 8pm PST Friday (3am UTC Saturday) – 8am Japan time Monday (11pm UTC Sunday)

# Sidelink synchronization issue list

This feature lead summary document captures the remaining issues of sidelink synchronization mechanism aspects for NR-V2X based on the submitted contributions [4]-[22]. The issue list with priorities can be found as following subsection.

# Email discussion Round 1

|  |  |  |  |
| --- | --- | --- | --- |
| **Issue#** | **Descriptions** | **Tdocs** | **Email responses** |
| 1 | 1-1 PSBCH content: Indication of TDD configuration | [4, Huawei, HiSilicon] [5, ZTE, Sanechips] [6, vivo] [7, OPPO] [8, Nokia, NSB] [9, MediaTek] [11, LGE] [12, Intel] [14, CATT] [15, Samsung] [16, CMCC] [17, Ericsson] [18, Spreadtrum] [19, Apple] [21, NTT DOCOMO] | [CATT] [Samsung] [ZTE, Sanechips] [vivo] [NTT DOCOMO] [Ericsson] [Huawei, HiSilicon] [Apple] [Futurewei] [Qualcomm] [Sharp] [CMCC] [Intel] [LGE] [Fujitsu] [Nokia] [MediaTek] |
| 1-2 PSBCH content: Slot index vs. S-SSB index | [14, CATT] | [CATT] [Samsung] [ZTE, Sanechips] [NTT DOCOMO] [Ericsson] [Huawei, HiSilicon] [Apple] [Futurewei] [Qualcomm] [Sharp] [CMCC] [Intel] [Fujitsu] [MediaTek] |
| 2 | DM-RS sequence initialization for PSBCH | [4, Huawei, HiSilicon] [5, ZTE, Sanechips] [8, Nokia, NSB] [11, LGE] [12, Intel] [14, CATT] [15, Samsung] [17, Ericsson] [18, Spreadtrum] | [CATT] [Samsung] [ZTE, Sanechips] [NTT DOCOMO] [Ericsson] [Huawei, HiSilicon] [Apple] [Futurewei] [Qualcomm] [Sharp] [CMCC] [Intel] [LGE] [Fujitsu] [Nokia] [MediaTek] |
| 3 | QCL for S-SSB transmission | [4, Huawei, HiSilicon] [5, ZTE, Sanechips] [6, vivo] [11, LGE] [12, Intel] [13, Futurewei] [15, Samsung] [17, Ericsson] [20, Sharp] | [Samsung] [ZTE, Sanechips] [vivo] [Huawei, HiSilicon] [Futurewei] [Sharp] [CMCC] [Fujitsu] |
| 4 | 4-1 Sync procedure: SL SSIDs/sync resources for each priority | [14, CATT] | [CATT] [ZTE, Sanechips] [NTT DOCOMO] [Qualcomm] |
| 4-2 Sync procedure: Lower SLSS ID with higher priority for P6/P6’ UE | [11, LGE] [12, Intel] [21, NTT DOCOMO] [22, Qualcomm Incorporated, FirstNet, UK Home office, Kyocera, Continental Automotive GmbH, LGE, AT&T, OPPO, Panasonic, Ford Motor Company, Bosch, NTT DOCOMO, Fraunhofer HHI, Fraunhofer IIS] | [CATT] [ZTE, Sanechips] [NTT DOCOMO] [Qualcomm] [LGE] [Fujitsu] |
| 5 | Slot number/sidelink timing derived from GNSS | [4, Huawei, HiSilicon] [6,vivo] [9, MediaTek] [11, LGE] [20, Sharp] | [ZTE, Sanechips] [vivo] [Ericsson] [Huawei, HiSilicon] [Apple] [Sharp] [CMCC] [LGE] [Fujitsu] [MediaTek] |
| ~~6~~ | ~~PSBCH rate matching for ECP~~ | ~~[12, Intel]~~ | ~~[CMCC] [Intel]~~ |
| 7 | Resource sets for S-SSB transmission | [7, OPPO] [8, Nokia, NSB] [12, LGE] [14, CATT] | [CATT] [ZTE, Sanechips] [vivo] [NTT DOCOMO] [Apple] [Futurewei] [CMCC] [Intel] [Fujitsu] [Nokia] |
| 8 | Timing determination of S-SSB | [10, Fujitsu] [12, Intel] [15, Samsung] | [ZTE, Sanechips] [Ericsson] [CMCC] [Fujitsu] |
| 9 | Limitation on the S-SSB interval | [4, Huawei, HiSilicon] | [Huawei, HiSilicon] |
| 10 | Synchronization to multiple sources | [8, Nokia, NSB] | [Ericsson] [Nokia] |
| 11 | SL timing derived from eNB/gNB timing | [4,Huawei, HiSilicon] [9, MediaTek] | [ZTE, Sanechips] [Ericsson] [Huawei, HiSilicon] [MediaTek] |
| 12 | Timing offset between eNB and gNB synchronization sources | [4, Huawei, HiSilicon] |  |
| 13 | eNB/gNB type synchronization as UE capability | [4, Huawei, HiSilicon] | [Ericsson] |
| 14 | The number of timing references | [4, Huawei, HiSilicon] | [Ericsson] [Nokia] |
| 15 | In-device coexistence between LTE-V2X and NR-V2X | [11, LGE] | [LGE] |
| 16 | (Re-)selection of SyncRef in EN-DC/NE-DC network | [9, MediaTek] | [MediaTek] |
| 17 | Determination of In-coverage and out-of-coverage | [20, Sharp] |  |
| 18 | PSBCH-DMRS or S-SSS for SLSS RSRP measurement |  | [MediaTek] |

# Email discussion Round 2

|  |  |  |  |
| --- | --- | --- | --- |
| **Thread 1** | **Issue** | **Email support** | **NOT support** |
| Issue 1-1: PSBCH contents - Indication of TDD configuration | [Huawei, HiSilicon] [LGE] [Nokia] [Ericsson] [Qualcomm] [Samsung] [Futurewei] [CATT] [Intel] [Spreadtrum] |  |
| Issue 1-2: PSBCH contents - Slot index vs. S-SSB index | [Huawei, HiSilicon] [CATT] [Intel] | [LGE] [Nokia] [Ericsson] [Qualcomm] [Samsung] [Futurewei] [Spreadtrum] |
| Issue 1-3: PSBCH contents - SL resource configuration ID | [Huawei, HiSilicon] [CATT] [Intel] | [LGE] [Nokia] [Ericsson] [Qualcomm] [Samsung] [Futurewei] [ZTE] [Spreadtrum] |

|  |  |  |  |
| --- | --- | --- | --- |
| **Thread 2** | **Issue** | **Email support** | **NOT support** |
| Issue 2: DM-RS sequence initialization for PSBCH | [Huawei, HiSilicon] [LGE] [Nokia] [Ericsson] [Qualcomm] [Samsung] [Futurewei] [CATT] [Intel] [Spreadtrum] |  |
| Issue 3: QCL for S-SSB | [Huawei, HiSilicon] [Samsung] [Futurewei] [vivo] | [LGE] [Nokia] [Qualcomm] [CATT] [Intel] |

|  |  |  |  |
| --- | --- | --- | --- |
| **Thread 3** | **Issue** | **Email support** | **NOT support** |
| Issue 4-1: Sync procedure - SL SSIDs/sync resources for each priority | [Huawei, HiSilicon] [CATT] [Spreadtrum] | [LGE] [vivo] [Intel] |
| Issue 4-2: Sync procedure - Lower SLSS ID with higher priority for P6/P6’ UE | [LGE] [Qualcomm] [CATT] | [Huawei, HiSilicon] [Intel] |

|  |  |  |  |
| --- | --- | --- | --- |
| **Thread 4** | **Issue** | **Email support** | **NOT support** |
| Issue 5: Slot number/sidelink timing derived from GNSS | [Huawei, HiSilicon] [LGE] [Nokia] [Ericsson] [Spreadtrum] |  |
| Issue 7: Resource sets for S-SSB transmission | [Huawei, HiSilicon] [LGE] [Nokia] [Ericsson] [Futurewei] [Intel] |  |

|  |  |
| --- | --- |
| **Company** | **Comments** |
| LGE | Thread 1   * For Issue 1-2, as already discussed/commented, we don’t think that there will be a critical problem (in terms of system operation) even without changing the current WA. Note that we are now under the maintenance phase, so if there is no strong support/need to address a certain issue, then it would be reasonable not to include it in the scope of email discussion. Also we are not fully convinced whether Issue 1-3 is really critical one needed to be resolved. In summary, our preference is to delete Issue 1-2/1-3 in Thread 1.   Thread 3   * For Issue 4-1, we are wondering what additional agreement can be made in RAN1 side. To our understanding, the current RAN1 agreements are sufficient. If the main purpose of Issue 4-1 is to clarify the meaning of existing RAN1 agreement, then it would be better to discuss it in RAN2 CR discussion. Our preference is to delete Issue 4-1 in Thread 3. |
| ZTE | For thread 1, our understanding is that 1-3) SL resource configuration ID bits in PSBCH is kind of optimization work thus we prefer to delete this for this meeting. We would appreciate if the proponent could further clarify if there is any misunderstanding from our side. |
| vivo | Thanks for the discussion. I have a similar view as Seungmin on issue#4-1. The previous agreement on reusing the LTE mechanism is adequate and I don’t think any additional modifications would be required. If some modifications would be needed, I think we could discuss it in the RAN2 CR phase as suggested by Seungmin. |
| MediaTek | To avoid impact on the RAN4 progress and make the spec completed, we can add issue 18 into thread 2 as part of S-SSB discussion.  This issue is also related DMRS in issue 2. |
| Huawei, HiSilicon | We think the issue 9 should be put under Thread 2, since they are associated issues. We pointed in the previous email, we think: If we need combination multiple S-SSB within the periodicity (i.e. 160ms), the total configured S-SSB should be contained within a short window e.g. 10 or 20 ms similar with Uu link SSB(only 5ms SSB burst). Otherwise, the QCL relationship cannot be used to do the combination under the high UE speed and larger SCS.  For Thread 3, we think issue 8 and issue 11 is more critical than the current issue 4-2. Especially for issue 11, as pointed before: The sidelink timing definition for network type sync source haven’t been defined in 38.211 which has been captured in LTE-V2X with 36.211. If this is not defined, the sidelink cannot work when the network sync sources are configured. This is definitely essential issues, so we think it should be treated this meeting other than to discuss other optimization issue.  So our proposal for Thread 2 and 3 as following:             Thread 2  o    Issue 2: DM-RS sequence initialization for PSBCH  o    Issue 3: QCL for S-SSB  o    Issue 9:  Limitation on the S-SSB interval             Thread 3  o    Issue 4-1: Sync procedure - SL SSIDs/sync resources for each priority  o    Issue 11: SL timing derived from eNB/gNB timing  o    Issue 8:  Timing determination of S-SSB  We are ok with Thread 1 and 4. |
| Nokia | On issue 1-2 and issue 3 in thread 2, we agree with LGE that these would not be needed. On issue 1-3, we think that it  may be bit late stage to introduce new fields to MIB , but we could consider increasing the number of reserved bits to enable something like this introduced in future. For thread 3, we don’t have strong view, just observing that some aspects have been discussed in several meetings already. |
| Ericsson | Similar to LGE and Nokia we do not see the need of the discussion of some of the issues listed in the table.  For example in Issue 1-2, we have the WA of using the slot index for the PSBCH, so we think there is no need to discuss it any further. For Issue 1-3, we do not see the need of having this new field, but maybe some clarifications in this topic are needed. |
| Qualcomm | Issue 1-2, there is already a working in assumption in place, we prefer to not revisit.  Issue 3, QCL is not applicable due to the SFN-type transmissions of S-SSB. There is no need to discuss it. |
| Samsung | We have one further comment for QCL assumption for S-SSB. In our understanding, there are two sub-topics:  1)     QCL assumption for S-SSB with same index across S-SSB periods. In our view, this is the basic for S-SSB measurement and should be supported. We also believe this is already implied by the agreement “S-SSB transmission is periodic” from the UE point of view.  2)     QCL assumption configured for S-SSBs within the same S-SSB period. I understand this topic may be more controversial and there are companies supporting it and objecting it. More discussion may be needed in the email discussion.  So far, none of the above has been captured in the spec, and UE has zero information on the QCL relationship for S-SSB, which is the issue we believe. Especially, without 1), we believe the S-SSB based measurement is broken. |
| Futurewei | Please find Futurewei’s inputs below. No input means neutral. |
| CATT | We are OK with feature lead’s proposals.  Regarding thread 1, we think Issue 1-1 should be higher priority to finalize the TDD configuration.   For Issue 1-2, we would like to have a note on how to allow S-SSB combining for detection to achieve coverage extension for higher SCS if they are not discussed based on the comments by most companies that working assumption of slot index had being made.  We don’t think issue 3 of QCL for S-SSB is relevant to V2X.   QCL stands for “quasi-co-location”.   The QCL is used to identify the large-scale channel properties between RS’s transmitted from antenna, which might be co-located or non-co-located.  If all Tx antenna for a sync source are co-located, the large-scale channel properties are the same and no QCL needs to be discussed.  For V2X, is any non-co-located antenna?  We also think Issues 4-1 and 4-2 in thread 3 need to be discussed together.   In particular, the SL-SSID 337 could be in both priority 2 and 6.   For Issue 4-2, when UE detects SL-SSID 337, how does UE know SL-SSID 337 belongs to priority 2 or 6 for the lower SSID selection algorithm? |
| Intel | Issue 1-3: Support. We can accept to drop it to reduce scope and move forward. We think it is a technically superior solution, but seems we do not have enough time to finalize it in Rel16.  Appreciate FL proposal to finally discuss it.  Issue 4-1, 4-2: As it was agreed by RAN1, we assume LTE-V2X procedure is reused and these bullets looks as optimizations. Therefore we prefer to skip discussing them and give more time to other EDs. |
| Spreadtrum | Please find the preference in the above table. |

# PSBCH contents

In RAN1#99 meeting [2], the following fields in PSBCH contents were agreed.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Working assumption:   * PSBCH payload size is 56 bits including 24 bits of CRC.   Agreements:   * Note: “green” already earlier; “blue” new agreements, “brown” working assumption, “change marks” for updates  |  |  |  | | --- | --- | --- | | **PSBCH contents** | **Number of bits** | **Notes** | | DFN | 10 |  | | Indication of TDD configuration | 12 | System-wide information, e.g. TDD-UL-DL common configuration and/or potential SL slots | | Slot index | 7 | ~~Note: Up to 3 bits can be carried in DM-RS or in PBCH payload.~~ | | In-coverage indicator | 1 |  | | Reserve bits |  |  | | CRC | 24 |  | | Total bits | 56 |  | |

8 companies discussed TDD configuration indication in PSBCH content and proposed to confirm the working assumption of PSBCH payload size.

The proposals of PSBCH contents are as follows,

* Confirm the working assumption that TDD configuration is indicated by 12 bits. [4, Huawei, HiSilicon]
* Confirm the working assumption that slot index within a frame is indicated by 7 bits. [5, ZTE, Sanechips]
* PSBCH payload includes: [6, vivo]
* DFN: 10 bits
* SL-TDD-Config: 13 bits
* Pattern and Periodicity: 5 MSB
* Number of slots: 8 LSB
* Slot index: 7 bits
* In-coverage indication: 1 bit
* Reserved bits for future extension: 1 bit
* Following PSBCH fields are agreed. [11, LGE]

|  |  |  |  |
| --- | --- | --- | --- |
| PSBCH contents | MIB  # bits | Payload  # bits | Notes |
| DFN | 10 |  | Agreed |
| TDD configuration | 12 |  | WA is confirmed |
| Slot index within a frame |  | 7 | WA is confirmed |
| In-coverage indicator |  | 1 | Agreed |
| Reserved |  | 2 | For future extension |
| CRC |  | 24 | Agreed |
| Total bits |  | 56 |  |

* PSBCH content defines the following additional parameters: [12, Intel]
* Sidelink Resource Configuration ID.
* Reserved bits with pre-configurable number of bits and bit values.
* PSBCH for NR V2X should include DFN, S-SSB index, Indication of synchronization resource, Indication of TDD configuration and In-coverage indicator. Confirm the working assumption that PSBCH payload size is 56 bits including 24 bits of CRC. [14, CATT]

|  |  |  |
| --- | --- | --- |
| **PSBCH contents** | **bits** | **Notes** |
| Direct Frame Number | 10 | [0,1023] |
| Indication of TDD configuration | 11 | 11bits = 4bits (Period) + 7bits (UL Slot) |
| S-SSB index | 3 | 3 MSBs of 6 bits indicating S-SSB index come from PSBCH payload for FR2 |
| Indication of synchronization resource | 2 | 2bits indicate 3 candidate sets of synchronization resource |
| In-coverage Indicator | 1 | Carried by PSBCH Payload explicitly |
| Reserved | 5 | Reserved bits |
| CRC | 24 |  |
| **Total** | **56** |  |

* [15, Samsung]

|  |  |
| --- | --- |
| **PSBCH contents** | **Number of bits** |
| DFN | 10 |
| Indication of TDD configuration | 12 |
| Slot index | 7 |
| In-coverage indicator | 1 |
| Reserved bits | 2 |
| CRC | 24 |
| Total bits | 56 |

* Confirm the working assumption in RAN1#99 for the PSBCH contents for NR SL Rel-16. Moreover, 2 bits are used as reserve bits to complete the 56 bits of the PSBCH contents. [17, Ericsson]

## Indication of TDD configuration

In RAN1#100-e meeting [3], the following agreements on TDD configuration indication in PSBCH were achieved.

|  |
| --- |
| Agreements:   * Slot-level indication is supported in TDD configuration indication.   Agreements:   * The TDD configuration indication is done as follows: * X bits to indicate patterns + Y bits to indicate periodicity + Z bits to indicate UL slots. * FFS the values of X, Y and Z. * Total Z bits to indicate UL slots in pattern 1 and pattern 2 respectively if two patterns are configured. |

In NR Uu, the TDD configuration is of high flexibility and costs numbers of bits. 12 bits in PSBCH content cannot completely indicate TDD configurations. A simplified and reduced signaling overhead can be applied for TDD configuration in sidelink.

Slot-level indication is supported in TDD configuration indication while the 12 bits indication field in PSBCH can be divided into three parts to indicate patterns, periodicity and UL slots, separately. 15 companies discussed the potential solution on TDD indication with detailed design. By analyzing the proposals, the alternatives can be summarized as follows for further discussion and determination.

|  |  |  |  |
| --- | --- | --- | --- |
| **Alternatives** | **Overhead** | **Indication of Slot/symbol-level timing** | **Supporting companies** |
| Alt. 1 | 12 bits | 1bit (Pattern) + 4bits (Periodicity) + 7bits (UL slots) | [4, Huawei, HiSilicon] [5, ZTE, Sanechips] [8, Nokia, NSB] [11, LGE] [16, CMCC] [17, Ericsson] [21, NTT DOCOMO] |
| Alt. 2 | 0bit (Pattern) + 5bits (Periodicity) + 7bits (UL slots) | [7, OPPO] |
| Alt. 3 | 0bit (Pattern) + 4bits (Periodicity) + 8bits (UL slots) | [15, Samsung] |
| Alt. 4 | 1bit (Pattern) + 3bits (Periodicity) + 8bits (UL slots) | [12, Intel] |
| Alt. 5 | 11 bits | 0bit (Pattern) + 4bits (Periodicity) + 7bits (UL slots) | [14, CATT] |
| Alt. 6 | 13 bits | 1bit (Pattern) + 4bits (Periodicity) + 8bits (UL slots) | [6, vivo] [16, CMCC] [18, Spreadtrum] [19, Apple] |

***Proposal 1: Among the 12 bits for indication of TDD configuration:***

* ***X=1 bit indicates the number of patterns.***
* ***Y=4 bits indicate the periodicity information.***
* ***Z=7 bits indicate the UL slots.***

The proposal of TDD UL/DL configuration information were as follows,

* Among the 12 bits for indication of TDD configuration: [4, Huawei, HiSilicon]
* X=1 bit indicates the number of patterns.
* Y=4 bits indicate the periodicity information.
* If a single pattern is configured, Y=4 bits are the binary representation of a row index in Table 1-1,
* Otherwise, Y=4 bits are the binary representation of a row index in Table 1-2, which jointly indicate the periodicities of pattern1 and pattern2.
* The SL reference SCS configuration is derived by: [4, Huawei, HiSilicon]
* If a single pattern is configured, ,
* Otherwise, the mapping relation between each row index in Table 1-2 and the SL reference SCS is as follows:

|  |  |
| --- | --- |
| Index | SL Reference SCS configuration |
| 0 – 5 | 3 |
| 6 – 13 | 2 |
| 14 | 1 |
| 15 | 0 |

* Among the 12 bits for indication of TDD configuration: [4, Huawei, HiSilicon]
* Z=7 bits indicate the UL slots.
* If a single pattern is configured, Z bits indicate the UL slots in pattern1,
* Otherwise, Z bits jointly indicate the UL slots in pattern1 and pattern2.

------------------------------ Start of Text Proposal for TS 38.213----------------------------------------

---------------------------------- < Unchanged parts are omitted > -----------------------------------------

**16.1 Synchronization procedures**

---------------------------------- < Unchanged parts are omitted > -----------------------------------------

For reception of a S-SS/PSBCH block, a UE assumes a frequency location corresponding to the subcarrier with index 66 in the S-SS/PSBCH block [4, TS 38.211], is provided by *absoluteFrequencySSB-SL*. The UE assumes that an S-PSS symbol, an S-SSS symbol, and a PSBCH symbol have a same transmission power. The UE assumes a same numerology of the S-SS/PSBCH as for a SL BWP of the S-SS/PSBCH block reception, and that a bandwidth of the S-SS/PSBCH is within a bandwidth of the SL BWP. The UE assumes the subcarrier with index 0 in the S-SS/PSBCH block is aligned with a subcarrier with index 0 in the SL BWP.

For reception of a S-SS/PSBCH block, a UE assumes the following information is transmitted by means of the PSBCH payload:

- *sl-TDD-Config* – 12 bits as defined in [12, TS 38.331].

- *inCoverage* – 1 bit as defined in [12, TS 38.331].

- *directFrameNumber* – 10 bits as defined in [12, TS 38.331].

- *slotIndex* – 7 bits as defined in [12, TS 38.331].

- *reservedBits* – 2 bits as defined in [12, TS 38.331].

A bit sequence indicated by *sl-TDD-Config* provides the slot format over a number of slots:

- A number of patterns indicated by *TDD-UL-DL-ConfigCommon* as described in Subclause 11.1 by

- If, a *pattern1* is provided

- If, a *pattern1* and a *pattern2* are provided

- A period or two periods indicated by *dl-UL-TransmissionPeriodicity* by

- denotes an index in Table 16.1-1 if or Table 16.1-2 if

- A number of slots with only uplink symbols by

- if, a last slots in *pattern1* include only uplink symbols, where , and are defined in Subclause 11.1, and . The uplink slot indicator .

- if , a last slots in *pattern1* and a last slots in *pattern2* include only uplink symbols, where , , and are defined in Subclause 11.1, and is indicated by the index in Table 16.2. The uplink slot indicator.

- equal the binary representation of the USI according to

Table 16.1-1: Slot configuration period when one pattern is indicated

|  |  |
| --- | --- |
| Index | Slot configuration period of *pattern1*  (msec) |
| 0 | 0.5 |
| 1 | 0.625 |
| 2 | 1 |
| 3 | 1.25 |
| 4 | 2 |
| 5 | 2.5 |
| 6 | 4 |
| 7 | 5 |
| 8 | 10 |
| 9 – 15 | Reserved |

Table 16.1-2: Slot configuration period when two patterns are indicated

|  |  |  |  |
| --- | --- | --- | --- |
| Index | Slot configuration period  (msec) | Slot configuration period of *pattern1*  (msec) | Slot configuration period of *pattern2*  (msec) |
| 0 | 1 | 0.5 | 0.5 |
| 1 | 1.25 | 0.625 | 0.625 |
| 2 | 2 | 1 | 1 |
| 3 | 2.5 | 0.5 | 2 |
| 4 | 2.5 | 1.25 | 1.25 |
| 5 | 2.5 | 2 | 0.5 |
| 6 | 4 | 1 | 3 |
| 7 | 4 | 2 | 2 |
| 8 | 4 | 3 | 1 |
| 9 | 5 | 1 | 4 |
| 10 | 5 | 2 | 3 |
| 11 | 5 | 2.5 | 2.5 |
| 12 | 5 | 3 | 2 |
| 13 | 5 | 4 | 1 |
| 14 | 10 | 5 | 5 |
| 15 | 20 | 10 | 10 |

Table 16.2: The SL reference SCS when two patterns are configured

|  |  |
| --- | --- |
| Index | SL Reference SCS configuration |
| 0 – 5 | 3 |
| 6 – 13 | 2 |
| 14 | 1 |
| 15 | 0 |

---------------------------------- < Unchanged parts are omitted > -----------------------------------------

------------------------------------------ End of Text Proposal -----------------------------------------------

* Support 1 bit to indicate pattern and 4 bits to indicate periodicity, i.e., X=1 and Y=4. The potential sidelink slot number is divided into two parts to be indicated based on a scaled granularity. N1 bit(s) are used to indicate the integer part and N2 bit(s) indicate the fractional part. N1 + N2 = Z, 0 ≤ N1, N2 ≤ Z. [5, ZTE, Sanechips]
* Multiple periodicities are supported for SL-TDD-Config in PSBCH, the periodicity indicated by SL-TDD-Config should be the same as that of NR Uu TDD-config in SIB1. [6, vivo]
* 13 bits are used for SL-TDD-Config, where 5 MSBs are used to indicate the number of TDD pattern and periodicity, 8 LSBs are used for resource indication.
* When the indicator of periodicity and number of patterns=0~8, there is 1 TDD pattern, and the 8 LSBs indicate the number of slot for SL.
* When the indicator of periodicity and number of patterns=9~31, there are 2 TDD patterns, and the 8 LSBs indicate the number of SL resources as below:
* For P1 and P2 correspond to entry#9~22 in Table 3, indicator value =9~22, the granularity of resource indication is 1 slot.
* For P1=P2=5ms
* When SCS=15/30/60kHz, indicator value=23, the granularity of resource indication is 1 slot
* When SCS=120kHz, indicator value=23~25, the granularity of resource indication is 2 slots
  + - If indicator value=23, only 1 pattern contains SL resource
    - If indicator value=24~25, both patterns contain SL resource
* For P1=P2=10ms
* When SCS=15/30KHz, indicator value=24, the granularity of resource indication is 1 slot
* When SCS=60KHz, indicator value=24~25, the granularity of resource indication is 2 slots
  + - If indicator value=24, only 1 pattern contains SL resource
    - If indicator value=25, both patterns contain SL resource
* When SCS=120KHz, indicator value=26~30, the granularity of resource indication is 2 slots
  + - If indicator value=26, only 1 pattern contains SL resource
    - If indicator value=27~30, both patterns contain SL resource

Where P1 and P2 correspond to the periodicity of the first and second pattern respectively, granularity means the unit of resource indication.

* eNB and gNB provide X, Y and Z bits TDD configuration to UE through SL SIB, and UE sets the SL-TDD-Config bits in its PSBCH to the same values provided by network. [6, vivo]
* 15kHz is assumed to be referenceSubcarrierSpacing for TDD indication in PSBCH. For TDD configuration indication in PSBCH: [7, OPPO]
* X=0 bit to indicate the patterns;
* Y=5 bits to indicate the periodicities;
* Z=7 bits to indicate the number of UL slots in pattern 1 and pattern 2(if configured)
* For the Z=7 bits to indicate the number of UL slots in pattern 1 and pattern 2:
* In case of only one pattern, all code-points are used to indicate the number of UL slots within the pattern;
* In case of 2 patterns, P code-points is used to indicate the number of slots within the first pattern, and the remaining code-points are used to indicate the number of slots within the second pattern;
* It is up to editor to capture this in the specification.
* For UL-DL slot configuration in [8, Nokia, NSB]
* In order to indicate full possible TDD UL configurations 19bits would be needed. For NR UL-DL TDD slot configuration, option to have two patterns needs to be supported in SL slot configuration as well. On the 12 bits reserved of UL-DL slot configuration in PSBCH, use one bit, X=1, to indicate whether one pattern (P) or two patterns are assumed (P+P2).

For the indication of pattern times select among two options:

* If pre-configuration periods candidates is supported, use 3 bits, Y=3, to indicate the predefined pattern combination, or
* If pre-configuration periods candidates is not supported, use 4 bits, Y=4, to indicate the pattern combination among options indicated in Table 3 and increasing the UL-DL slot configuration size by 1 bit.
* Indicating only sub-set of full UL slots of each pattern could be used to restrict the number of bits needed for UL-DL TDD slot configuration signalling. This would result 16 different values for number of slots per pattern.
* In case single pattern (P) is indicated, number of SL slots in the pattern can be indicated directly by Z=8 bits.
* In case two patterns (P+P2) are indicated the number of SL slots for each pattern are indicated by 4 bits for each (Z=4+4). For higher sub-carrier spacings where 4 bits is not enough, higher granularity is used e.g. 2 for 60kHz and 4 for 120kHz.
* For slot index indication in [8, Nokia, NSB]
* Information regarding the UL slot locations can be used in S-SSB slot index information.
* Determine PSBCH information element for the slot index (slotIndex) so that it accounts the UL-DL slot configuration information, and logically indicates the index of the UL slot within the concatenated pattern.
* Reduce the number of bits for the slot index (slotIndex) to 6 bits (or to 5 bits).
* For the dual-period patterns with the same period for P1 and P2, UL slot indication for a reference pattern can be used to derive the UL slots for the other patterns with reduced signaling overhead. [9, MediaTek]
* TDD configuration field in PSBCH consists of 12 bits, where X=1 bit (pattern), Y=4 bits (periodicity), Z=7 bits (UL slots). Information indicated by X, Y, and Z bits is as follows. [11, LGE]

X value:

|  |  |
| --- | --- |
| X | Number of patterns |
| 0 | 1 |
| 1 | 2 |

Y value for X=0 (one pattern case):

|  |  |
| --- | --- |
| Y (in decimal) | Periodicity |
| 0 | 0.5 |
| 1 | 0.625 |
| 2 | 1 |
| 3 | 1.25 |
| 4 | 2 |
| 5 | 2.5 |
| 6 | 4 |
| 7 | 5 |
| 8 | 10 |

Y value for X=1 (two patterns case):

|  |  |  |
| --- | --- | --- |
| Y (in decimal) | Periodicity of pattern 1 | Periodicity of pattern 2 |
| 0 | 0.5 | 0.5 |
| 1 | 0.625 | 0.625 |
| 2 | 1 | 1 |
| 3 | 0.5 | 2 |
| 4 | 2 | 0.5 |
| 5 | 1.25 | 1.25 |
| 6 | 1 | 3 |
| 7 | 3 | 1 |
| 8 | 2 | 2 |
| 9 | 1 | 4 |
| 10 | 4 | 1 |
| 11 | 2 | 3 |
| 12 | 3 | 2 |
| 13 | 2.5 | 2.5 |
| 14 | 5 | 5 |
| 15 | 10 | 10 |

Z indicates the number of UL slots in pattern 1 and 2 with respect to the reference SCS as follows when NP1 and NP2 are the maximum number of UL slots in pattern 1 and 2 respectively for given X and Y value.

|  |  |  |
| --- | --- | --- |
| Z (in decimal) | #UL slots in pattern 1 | #UL slots in pattern 2 |
| 0, …, NP2-1 | 0 | 1,…, NP2 |
| NP2, …, 2\* NP2 | 1 | 0,…, NP2 |
| 2\* NP2+1, …, 3\* NP2+1 | 2 | 0,…, NP2 |
| … | … | … |
| k\* NP2+k-1, …, (k+1)\* NP2+k-1 | k | 0,…, NP2 |
| … | … | … |
| NP1\* NP2+ NP1-1, …, ( NP1+1)\* NP2+ NP1-1 | NP1 | 0,…, NP2 |

* The number of UL slots for a pattern is counted as the number of successive UL slots from the end of the periodicity of the pattern. The UL slot indicated by PSBCH TDD configuration includes the slot that contains at least Y-th, (Y+1)-th, ..., (Y+X-1)-th UL symbols, where X and Y are sl-LengthSymbols and sl-StartSymbol respectively. The ‘virtual’ UL slots based on the reference SCS signaled by TDD configuration in PSBCH should indicate only the ‘actual’ UL slots based on the SL SCS. TDD configuration field in PSBCH and the reference SCS is (pre-)configured by a higher layer signaling. [11, LGE]
* The following signalling can be used: up to 8bits for indication of UL slots and one bit to indicate number of patterns and remaining 3 bits for indication of periodicity. Joint encoding can be also use to maximize number of configurations. [12, Intel]
* The number of bits for indication of TDD configuration for two TDD patterns is so large that NR V2X PSBCH cannot accommodate these bits. Only inform the TDD configuration for one TDD pattern in order to reduce the overhead. Indication of TDD configuration occupies 11 bits in PSBCH payload. 11bits = 0bits (X, Pattern) + 4bits (Y, Periodicity) + 7bits (Z, UL Slots). [14, CATT]
* For TDD configuration, X = 0, Y = 4 and Z = 8, and support the following PSBCH contents and payload size. [15, Samsung]
* The detailed design of TDD configuration indication in PSBCH is as follows [16, CMCC]
  + For TDD configuration indication, X=1 bits to indicate patterns and Y=4 bits to indicate periodicities for single pattern or periodicity combinations for dual patterns.
  + If the working assumption of 12bits TDD configuration indication is to be confirmed, joint indication of UL slot in two patterns should be supported. Otherwise, if 13 bits can be considered leaving one reserved bit in PSBCH, independent indication of UL slots in two patterns can be supported.
  + For FR1, the number of UL slots in indicated using 60KHz as reference SCS with different granularities for different periodicity combinations as follow:
    - For periodicity combination other than 5ms+5ms and 10ms+10ms, one-slot granularity is used;
    - For 5ms+5ms periodicity, two-slot granularity is used;
    - For 10ms+10ms periodicity, three-slot granularity is used for independent indication of UL slots in two patterns with Z=8 bits and four-slot granularity is used for joint indication of UL slots in two patterns with Z=7 bits.
  + If the state that full periodicity are all UL slot is indicated, for FR2, the number of UL slots in indicated using 120KHz as reference SCS with different granularities for different periodicity combinations as follow:
    - For 0.5+0.5ms, 0.625+0.625ms, 1+1ms, 0.5+2ms, 2+0.5ms and 1.25+1.25ms periodicity combinations, one-slot granularity is used;
    - For 1+3ms, 3+1ms, 2+2ms, 1+4ms, 4+1ms, 2+3ms, 3+2ms and 2.5+2.5ms combinations, two-slot granularity is used;
    - For 5ms+5ms periodicity, three-slot granularity is used for independent indication with Z=8 bits and four-slot granularity is used for joint indication with Z=7 bits;
    - For 10ms+10ms periodicity, six-slot granularity is used for independent indication with Z=8 bits and eight-slot granularity is used for joint indication with Z=7 bits.
* In the PSBCH for NR SL the TDD configuration is as follows: [17, Ericsson]
  + X = 1 to indicate pattern 1 and pattern 2 following the structure in NR Uu
  + Y = 4 to indicate the periodicity following the possible values from NR Uu
  + Z = 7 to indicate the UL slots
* For TDD configuration indication in PSBCH, the following value is supported: X =1, Y =4, and Z=8. [18, Spreadtrum]
* For the indication of TDD configuration in PSBCH, the number of bits to indicate patterns is 1, the number of bits to indicate periodicity is 4, and the number of bits to indicate UL slots is 8. For the indication of TDD configuration in PSBCH, if two TDD patterns are configured, then the number of bits to indicate UL slots in each pattern is 4 bits, and the granularity of UL slot indication is slots, where is the total number of slots in a period for a given SCS [19, Apple]
* When two patterns are provided for TDD configuration, UL slots in both patterns can be used for SL communications. For TDD configuration indication in PSBCH, [21, NTT DOCOMO]
* X = 1 bit, 0 indicates one pattern; 1 indicates two patterns.
* Y = 4 bits, For one pattern, one value from {0.5, 0.625, 1, 1.25, 2, 2.5, 3, 4, 5, 10} is indicated; For two patterns, one combination from {(0.5, 0.5), (0.625, 0.625), (1, 1), (0.5, 2), (2, 0.5), (1.25, 1.25), (1, 3), (3, 1), (2, 2), (1, 4), (4, 1), (2, 3), (3, 2), (2.5, 2.5), (5, 5), (10, 10)} is indicated.
* Z = 7 bits, when the number of UL slot combinations in two patterns is more than 128, the UL slots are indicated with granularity of more than one slots.

## Slot index vs. S-SSB index

In RAN1#99 meeting [2], slot index with 7 bits are agreed as a working assumption in PSBCH for timing indication.

In [14, CATT], it is proposed to use S-SSB index to replace slot index in PSBCH for sidelink timing indication. Some drawbacks with slot index are: slot number of each S-SSB is not consecutive as S-SSB index, which will hinder the combining of multiple S-SSBs for PSBCH decoding; introduce more standardization efforts, as a lot of procedures are related to S-SSB index, such as PSBCH DM-RS sequence initialization and PSBCH scrambling; slot number cannot carry the information of beam index when beam sweeping was introduced in future release.

***Proposal 2: The indication mechanism of SSB index in NR Uu can be reused for the indication of S-SSB index in NR V2X.***

* ***For FR1, the 2 bits indicating S-SSB index are carried by DMRS sequence of PSBCH***
* ***For FR2, the 3 MSBs of 6 bits indicating S-SSB index are carried by PSBCH payload and the 3 LSBs of the S-SSB index by DMRS sequence of PSBCH.***

The proposals of using S-SSB index for indication are as follows,

* S-SSB index should be included into PSBCH payload instead of slot number for the case of S-SSB combining for sidelink coverage extension and beam sweeping for V2X in FR2. The indication mechanism of SSB index in NR Uu can be reused for the indication of S-SSB index in NR V2X. [14, CATT]
* For FR1, the 2 bits indicating S-SSB index are carried by DMRS sequence of PSBCH
* For FR2, the 3 MSBs of 6 bits indicating S-SSB index are carried by PSBCH payload and the 3 LSBs of the S-SSB index by DMRS sequence of PSBCH.

-------------------------------------------------Start of Text Proposal for 38.212-----------------------------------------------

8.1.1 PSBCH payload generation

Denote the bits in a transport block delivered to layer 1 by, where  is the payload size generated by higher layers. The lowest order information bit  is mapped to the most significant bit of the transport block.

Generate the following additional timing related PSBCH payload bits , where:

- if the frequency range of S-SSB is *FR2*,

are the 6th, 5th, and 4th bits of S-SSB index, respectively.

- else if the frequency range of S-SSB is *FR1*

are reserved.

- end if

----------------------------------------------- < Unchanged parts are omitted > -----------------------------------------------

--------------------------------------------------------End of Text Proposal -----------------------------------------------------

# DM-RS sequence initialization for PSBCH

In RAN1#100-e meeting [3], the following agreements on DM-RS sequence initialization for PSBCH were achieved. Two alternatives were left for further down selection. For Alt 1, it is beneficial to randomize the interference if the initialization contains S-SSB index information, and the effect of blind detection is minimized. For Alt 2, some companies think it is not applicable for SL to blind detect timing information from DM-RS, and there is no necessary to do randomization because UE is not combining the DM-RS sequence. It cannot help to have interference randomization since carrying timing information in DM-RS degrades the cross-correlation of the sequences.

|  |
| --- |
| Agreement:   * SL SSID is used for DM-RS sequence initialization in PSBCH.   Agreements:  The DM-RS sequence initialization for PSBCH is to be down-selected one from the following Alts:   * Alt 1: , where is 3 LSBs of S-SSB index. * Alt 2: |

9 companies discussed this issue in their contributions. Alt 1 is supported by 3 companies with modification on the definition of in [11, LGE] [12, Intel] [14, CATT]. Alt 2 is supported by 5 companies in [4, Huawei, HiSilicon] [5, ZTE, Sanechips] [15, Samsung] [17, Ericsson] [18, Spreadtrum]. 1 company proposed to apply priority level of the selected sync source in PSBCH DM-RS initialization in [8, Nokia, NSB], but it is not following the down selection rules from the two Alternatives as agreed in last meeting.

|  |  |  |
| --- | --- | --- |
| **Alternatives** | **DM-RS sequence initialization** | **Supporting companies** |
| Alt. 1 | , where is 3 LSBs of S-SSB index. | [11, LGE] [12, Intel] [14, CATT] |
| Alt. 2 |  | [4, Huawei, HiSilicon] [5, ZTE, Sanechips] [15, Samsung] [17, Ericsson] [18, Spreadtrum] |

***Proposal 3: The DM-RS sequence initialization for PSBCH can be:***

* , where is 3 LSBs of S-SSB index.

The proposals of DM RS sequence initialization for PSBCH are as follows,

* For The DM-RS sequence initialization for PSBCH: Overall there is no significant performance difference between Alt1 and Alt2. Considering an NR-V UE may maintain multiple sync sources simultaneously, the blind detection complexity resulting from Alt 1 may be significant. [4, Huawei, HiSilicon]
* Adopt Alt 2 with the following modification: For PSBCH DM RS, the scrambling sequence generator shall be initialized at the start of every PSBCH subframe with . [5, ZTE, Sanechips]
* (Logical) S-SSB index cannot be used in PSBCH DM-RS initialization. Account the priority level of the selected synchronization source in PSBCH DM-RS initialization. Adopt following text proposal to Section 8.4.1.4.1 of 38.211. [8, Nokia, NSB]

------------------------------ Start of Text Proposal for TS 38.211----------------------------------------

**8.4.1.4.1 Sequence generation**

The reference-signal sequence for an S-SS/PSBCH block is defined by

where is given by clause 5.2. The scrambling sequence generator shall be initialized at the start of each S-SS/PSBCH block occasion with

where is priority index corresponding to the S-SS/PBCH block transmission and is the physical layer sidelink identity.

------------------------------------------ End of Text Proposal -----------------------------------------------

* DM-RS sequence initialization is associated with S-SSB index and SLSSID, similar to NR Uu PBCH DM-RS. The text proposal is provided TP#1 in Appendix. [11, LGE]

,

where is S-SSB index mod 8.

------------------------------ Start of Text Proposal for TS 38.211----------------------------------------

**8.4.1.4.1 Sequence generation**

The reference-signal sequence for an S-SS/PSBCH block is defined by

where is given by clause 5.2. The scrambling sequence generator shall be initialized at the start of each S-SS/PSBCH block occasion with

*,*

where *is* the modulo-8 value of S-SS/PSBCH block index as defined in Subclause 16.1 of [5, TS38.213]*.*

------------------------------------------ End of Text Proposal --------------------------------------------------

* For PSBCH DMRS generation the Alt.1 is adopted with the following changes: the is represented by 6 LSBs of S-SSB index, where max S-SSB index depends on SCS and FR settings. [12, Intel]
* The PSBCH DM-RS sequence initialization should use the following formula: [14, CATT]

Where is 3 LSBs of S-SSB index.

-------------------------------------------------Start of Text Proposal for 38.211-----------------------------------------------

8.4.1.4 Demodulation reference signals for PSBCH

8.4.1.4.1 Sequence generation

The reference-signal sequence for an S-SS/PSBCH block is defined by

where is given by clause 5.2. The scrambling sequence generator shall be initialized at the start of each S-SS/PSBCH block occasion with

where

- is 3 LSBs of S-SSB index.

--------------------------------------------------------End of Text Proposal -----------------------------------------------------

* Support Alt 2 for DM-RS of PSBCH, and adopt the following TP for Section 8.4.1.4.1 of TS 38.211. [15, Samsung]

**====================== Start of TP for Section 8.4.1.4.1 of TS 38.211 ========================**

8.4.1.4.1 Sequence generation

The reference-signal sequence for an S-SS/PSBCH block is defined by

where is given by clause 5.2. The scrambling sequence generator shall be initialized at the start of each S-SS/PSBCH block occasion with

.

**====================== End of TP for Section 8.4.1.4.1 of TS 38.211 ========================**

* For the DM-RS sequence generation, use Alt.2: c\_init = N\_ID^SL. [17, Ericsson]
* The following DM-RS sequence initialization for PSBCH should be supported: Alt 2: . [18, Spreadtrum]

# QCL for S-SSB transmission

In order to guarantee the PSBCH coverage for higher SCS and to support beamforming for FR2, S-SSB repetition with the same QCL assumption should be supported.

9 companies discussed about the QCL for S-SSB with necessity in [4, Huawei, HiSilicon] [5, ZTE, Sanechips] [6, vivo] [11, LGE] [12, Intel] [13, Futurewei] [15, Samsung] [17, Ericsson] [20, Sharp], and 3 of them discussed about details on how to define QCLed in S-SSB.

Whether to support QCL for S-SSB transmission can be found in the following table from the contributions.

|  |  |  |
| --- | --- | --- |
| **Alternatives** | **QCL for S-SSB transmission** | **Supporting companies** |
| Alt. 1 | Do not support QCL mechanism for S-SSB transmissions in NR SL. | [5, ZTE, Sanechips] [11, LGE] [12, Intel] [13, Futurewei] [17, Ericsson] [20, Sharp] |
| Alt. 2 | Support a (pre-)configured parameter for determining the QCL assumption of S-SSB. | [4, Huawei, HiSilicon] [6, vivo] [15, Samsung] |

***Proposal 4: QCL mechanism is not used for S-SSB transmissions in NR SL.***

The proposals of whether/how to define QCL for S-SSB transmission are as follows,

* For the (pre-)configured actually transmitted S-SSB, a number of R neighboring S-SSBs are QCLed. For sidelink transmission, R neighboring S-SSBs are QCLed with each other by QCL-TypeA for FR1 and FR2. [4, Huawei, HiSilicon]

------------------------------ Start of Text Proposal for TS 38.213----------------------------------------

---------------------------------- < Unchanged parts are omitted > -----------------------------------------

**16.1 Synchronization procedures**

---------------------------------- < Unchanged parts are omitted > -----------------------------------------

A UE is provided, by *numSSBQCLwithinPeriod-SL*, *numSSBwithinPeriod-SL*, a number of S-SS/PSBCH blocks in a period of 16 frames. The UE assumes that a transmission of the S-SS/PSBCH blocks in the period is with a periodicity of 16 frames. The UE assumes that /*M* groups of S-SS/PBCH are QCLed within *numSSBwithinPeriod-SL*, where *M* is the value of *numSSBQCLwithinPeriod-SL*. The UE determines indexes of slots that include S-SS/PSBCH block as +, where

- index 0 corresponds to a first slot in a frame with SFN satisfying

- is a S-SS/PSBCH block index within the number of S-SS/PSBCH blocks in the period, with

- is a slot offset from a start of the period to the first slot including S-SS/PSBCH block, provided by *timeOffsetSSB-SL*

- is a slot interval between S-SS/PSBCH blocks, provided by *timeIntervalSSB-SL*

If a UE would transmit or receive an S-SS/PSBCH block or, for E-UTRA radio access, sidelink synchronization signals, and the transmission or reception would overlap in time with other transmissions and/or receptions on the sidelink, the UE transmits or receives the signal/channel with the higher priority.

---------------------------------- < Unchanged parts are omitted > -----------------------------------------

------------------------------------------ End of Text Proposal -----------------------------------------------

* A receiving UE cannot identify which UE is the transmitter of the S-SSB detected because multiple UEs in different locations may transmit S-SSB in the same S-SSB transmission resource. The receiving UE shall not assume other sidelink signals/channels and S-SSB to be quasi co-located. [5, ZTE, Sanechips]
* A subset of S-SSB in a periodicity can be assumed as QCLed. For example, the S-SSB with the same value of (S-SSB index MOD M) or (S-SSB index/M) can be assumed as QCLed, where M is a (pre-)configured QCL factor. [6, vivo]

**------------------------------------------------------ Start of Draft TP of 213-------------------------------------------------**

**16.1 Synchronization procedures**

**<Unchanged parts omitted>**

A UE is provided, by *numSSBwithinPeriod-SL*, a number of S-SS/PSBCH blocks in a period of 16 frames. The UE assumes that a transmission of the S-SS/PSBCH blocks in the period is with a periodicity of 16 frames. The UE determines indexes of slots that include S-SS/PSBCH block as +, where

- index 0 corresponds to a first slot in a frame with SFN satisfying

- is a S-SS/PSBCH block index within the number of S-SS/PSBCH blocks in the period, with

- is a slot offset from a start of the period to the first slot including S-SS/PSBCH block, provided by *timeOffsetSSB-SL*

- is a slot interval between S-SS/PSBCH blocks, provided by *timeIntervalSSB-SL*

The UE may assume that S-SS/PBCH blocks transmitted with the same on the same center frequency location are quasi co-located with respect to Doppler spread, Doppler shift, average gain, average delay, delay spread, and, when applicable, spatial Rx parameters, where is provided by high layer.

**---------------------------------------------------------- End of Draft TP -------------------------------------------------------**

* QCL configuration over S-SSB is not supported in Rel.16. [11, LGE]
* Do not define QCL signalling for S-SSB transmissions. [12, Intel]
* QCL is not defined within an S-SSB period. [13, Futurewei]
* Support a (pre-)configured parameter for determining the QCL assumption of S-SSBs (e.g. denoted as ), such that at least one of the following alternatives is supported, where is the S-SSB index: [15, Samsung]
* Alt 1: S-SSBs with same are assumed to be QCLed;
* Alt 2: S-SSBs with same are assumed to be QCLed.

**======================== Start of TP for Section 16.1 of TS 38.213 ========================**

16.1 Synchronization procedures

**============================== Unchanged Text Omitted =============================**

A UE is provided, by *numSSBwithinPeriod-SL*, a number of S-SS/PSBCH blocks in a period of 16 frames. The UE assumes that a transmission of the S-SS/PSBCH blocks in the period is with a periodicity of 16 frames. The UE determines indexes of slots that include S-SS/PSBCH block as +, where

- index 0 corresponds to a first slot in a frame with SFN satisfying

- is a S-SS/PSBCH block index within the number of S-SS/PSBCH blocks in the period, with

- is a slot offset from a start of the period to the first slot including S-SS/PSBCH block, provided by *timeOffsetSSB-SL*

- is a slot interval between S-SS/PSBCH blocks, provided by *timeIntervalSSB-SL*

The UE may assume that S-SS/PBCH blocks transmitted with the same S-SS/PBCH block index on the same center frequency location are quasi co-located with respect to Doppler spread, Doppler shift, average gain, average delay, delay spread, and, when applicable, spatial Rx parameters.

**============================== Unchanged Text Omitted =============================**

**======================== End of TP for Section 16.1 of TS 38.213 ========================**

* Due to the broadcast nature, i.e. no intended Rx, of S-SSB, it is not clear how to map one S-SSB to another S-SSB for QCL operation even within the same transmission period. Do not support QCL mechanism for S-SSB transmissions in NR SL. [17, Ericsson]
* QCL assumption for S-SSB transmission is not specified. [20, Sharp]

# Synchronization procedures

## SL SSIDs/sync resources for each priority

In LTE V2X, the different synchronization priority level can be differed by synchronization resource, SL-SSID and In\_Coverage flag. As LTE V2X, both SL-SSID and In-coverage Indicator should be used to indicate the times of SLSS relaying hops for NR V2X. For the SL-SSIDs used for each priority of synchronization reference in NR V2X, we believe that LTE V2X mechanism will be reused for NR V2X with the SL-SSIDs extended to 672, since LTE V2X had discussed a lot on this topic and developed a comprehensive mechanism. If we directly reuse the mapping rules from SL-SSID to priority levels of LTE V2X with the SL-SSIDs extended to 672, the following two Tables can be derived from LTE V2X related tables, which corresponding to gNB/eNB-based and GNSS-based synchronization priority levels for NR V2X, respectively.

**Table X: gNB/eNB-based synchronization priority levels for NR V2X**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Priority level** | **gNB/eNB-based synchronization** | **Sync resource** | **In-coverage indicator** | **NR V2X SL-SSID range** |
| P0’ | gNB/eNB |  |  |  |
| P1’ | UE1 directly sync with gNB/eNB | R1 | TRUE | [1,335] |
| P2’ | UE2 indirectly sync with gNB/eNB | R2 | FALSE | [1,335] |
| P3’ | GNSS |  |  |  |
| P4’ | UE3 directly sync with GNSS | R3 | TRUE | 0 |
| P5’ | UE4 indirectly sync with GNSS by UE3 | R2 | FALSE | 337 |
| P6’ | UE5( >= 2 hops sync with gNB/eNB by UE2) | R1/R2 | FALSE | [337,671] |
| UE6(>=2 hops sync with GNSS by UE4) | R1/R2 | FALSE | 337 |
| UE7(standalone) | R1/R2 | FALSE | [338,671] |

**Table Y: GNSS-based synchronization priority levels for NR V2X**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Priority level** | **GNSS-based synchronization** | **Sync resource** | **In-coverage indicator** | **NR V2X SL-SSID range** |
| P0 | GNSS |  |  |  |
| P1 | InC UE1 directly sync with GNSS | R1 | TRUE | 0 |
| OoC UE2 directly sync with GNSS | R3 | FALSE | 0 |
| P2 | UE3 indirectly sync with GNSS by InC UE(UE1) | R2 | FALSE | 0 |
| UE4 indirectly sync with GNSS by OoC UE(UE2) | R2 | FALSE | 337 |
| P3 | gNB/eNB |  |  |  |
| P4 | InC UE5 directly sync with gNB/eNB | R1 | TRUE | [1,335] |
| P5 | UE6 indirectly sync with gNB/eNB by InC UE(UE5) | R2 | FALSE | [1,335] |
| P6 | UE7(>=2 hops sync with GNSS by InC UE) | R1/R2 | FALSE | 336 |
| UE8(>=2 hops sync with gNB/eNB by InC UE) | R1/R2 | FALSE | [337,671] |
| UE9(>=2 hops sync with GNSS by OoC UE) | R1/R2 | FALSE | 337 |
| UE10(standalone) | R1/R2 | FALSE | [338,671] |

***Proposal 5: the following corrections shall be applied in current synchronization mechanism to solve the issues of ambiguity:***

* ***Reserve a SL-SSID for InC UE directly synch with GNSS, e.g. SL-SSID=1.***
* ***Then the SL-SSID set for In\_C UE directly synch with gNB/eNB is SL-SSID= [2,335].***
* ***For UE OoC sync to UE OoC, distinguish 2 cases:***
* ***If sync Ref UE is directly sync to GNSS (i.e., SL-SSID=0, and transmitting on resource 3).***
* ***Resource 2: InC = 0. SL-SSID=0.***
* ***Other cases:***
* ***Resource 1 or 2 (different from Sync Ref):***
* ***If the SL-SSID of Sync Ref UE is 0, SL-SSID = 336 and InC = 0;***
* ***Else, SL-SSID is from Sync Ref and InC = 0.***

The proposal to solve this problem can be found as follows:

* For SSIDs used for each priority, LTE V2X mechanism will be reused for NR V2X with the SSIDs extended to 672 and corrections to solve the issues of ambiguity. [14, CATT]
* The following corrections shall be applied in current synchronization mechanism to solve the issues of ambiguity: [14, CATT]
* Reserve a SL-SSID for InC UE directly synch with GNSS, e.g. SL-SSID=1.
* Then the SL-SSID set for In\_C UE directly synch with gNB/eNB is SL-SSID= [2,335].
* For UE OoC sync to UE OoC, distinguish 2 cases:
* If sync Ref UE is directly sync to GNSS (i.e., SL-SSID=0, and transmitting on resource 3).
* Resource 2: InC = 0. SL-SSID=0.
* Other cases:
* Resource 1 or 2 (different from Sync Ref):
* If the SL-SSID of Sync Ref UE is 0, SL-SSID = 336 and InC = 0;
* Else, SL-SSID is from Sync Ref and InC = 0.

## Lower SLSS ID with higher priority for P6/P6’ UE

The proposals/analysis of lower SLSS ID with higher priority for P6/P6’ UE are as follows:

* NR SyncRef UE (re)selection procedure is enhanced if UE selects SynchRefUE with lower SLSS ID (as long as RSRP>threshold to ensure quality of the SyncRef UE is above a threshold as per current specification) within the out-of-coverage SSB ID set ([336, 671]). [11, LGE]
* If this enhancement is (pre)configured, it replaces the RSRP-based SynchRefUE selection only for P6 and P6’ priority case
* We would like to point out that in any distributed system with hierarchical design the formation of sync clusters is unavoidable. The only solution to that problem is the use of global synchronization source like GNSS or network timing. Therefore, instead of optimization of sidelink sync procedure (that in any case will not be perfect) it is better to utilize infrastructure-based solutions and either deploy gNBs or sync sources that will relay timing from network or GNSS. [12, Intel]
* Cluster merge by synchronization based on lower SLSS ID for P6/P6’ UE should be discussed and supported. [21, NTT DOCOMO]
* [22, Qualcomm Incorporated, FirstNet, UK Home office, Kyocera, Continental Automotive GmbH, LGE, AT&T, OPPO, Panasonic, Ford Motor Company, Bosch, NTT DOCOMO, Fraunhofer HHI, Fraunhofer IIS]
  + If (pre)-configured in a carrier, the mechanism given below replaces the RSRP-based SynchRefUE selection only for P6 and P6’ priority case.
    - For the prioritization among references of the same priority for P6/P6’ UE, UEs select the lowest SLSS ID SynchRefUE among the SyncRefUEs with RSRP>threshold.
  + Future work on sidelink enhancements should aim to avoid formation of clusters.

***Proposal 6: RAN1 should discuss whether UE can be (pre-)configured with P6 sync source with SSID-based selection as the alternative of RSRP-based mechanism in Rel-16.***

# Slot number/sidelink timing derived from GNSS

In LTE V2X, the DFN and SFN is derived from current timing, reference timing and DFN offset when UE selects GNSS as the sync reference. The corresponding definition is captured in 36.331. When this mechanism is reused in NR V2X, the slot number (DFN) can also be defined in the same way. In NR V2X, various SCS is supported besides 15KHz. Different slot length less than 1 ms should also be taken into consideration.

5 companies discussed this issue in their contributions to have further clarification on the definition of slot number derived from GNSS [4, Huawei, HiSilicon] [6,vivo] [9, MediaTek] [11, LGE] [20, Sharp].

***Proposal 7: When UE selects GNSS as the synchronization reference and offsetDFN is provided, the following TP is supported.***

**------------------------------------------------------ Start of Draft TP of 38.331--------------------------------------------------**

**5.8.12 DFN derivation form GNSS**

When the UE selects GNSS as the synchronization reference source, the DFN used for NR sidelink communication is derived from the current UTC time, by the following formulae:

*DFN*= Floor (0.1\*0.001\* (*Tcurrent* – *Tref – offsetDFN*)) mod 1024

*SubframeNumber*= Floor (0.001\*(*Tcurrent* –*Tref – offsetDFN)*) mod 10

*SlotNumber=* Floor (0.001\*(*Tcurrent – Tref – OffsetDFN*)\*2μ) mod 2μ

Where:

***Tcurrent*** is the current UTC time that obtained from GNSS. This value is expressed in ~~milliseconds~~ microseconds;

***Tref*** is the reference UTC time 00:00:00 on Gregorian calendar date 1 January, 1900 (midnight between Thursday, December 31, 1899 and Friday, January 1, 1900). This value is expressed in ~~milliseconds~~ microseconds;

***OffsetDFN*** is the value *sl-OffsetDFN* if configured, otherwise it is zero. This value is expressed in ~~milliseconds~~ microseconds;

μ=0/1/2/3 corresponding to the 15/30/60/120 khz SCS for SL respectively.

**-------------------------------------------------------- End of Draft TP of 38.331-------------------------------------------------**

The proposals of SL timing derived from GNSS are as follows,

* For NR-V2X, both synchronous and asynchronous deployment scenarios between gNB and eNB should be supported. If GNSS type synchronization source is (pre-)configured, the slot number of sidelink should be defined as: [4,Huawei, HiSilicon]

SlotN = Floor (0.1\*(Tcurrent –Tref–offsetDFN)\*2μ) mod (10\*2μ)

Where the value μ depends on the SCS of the sidelink.

* When UE selects GNSS as the synchronization reference and offsetDFN is provided, the slot number in a subframe can be derived from the current UTC time, by the following formula: [6,vivo]

SlotNumber= Floor (0.001\*(Tcurrent – Tref - OffsetDFN)\* 2μ) mod 2μ

Where μ=0/1/2/3 corresponding to the 15/30/60/120 khz SCS for SL respectively, Tcurrent, Tref and OffsetDFN are defined in microseconds.

**------------------------------------------------------ Start of Draft TP of 331--------------------------------------------------**

**<Unchanged parts omitted>**

**5.8.12 DFN derivation form GNSS**

When the UE selects GNSS as the synchronization reference source, the DFN used for NR sidelink communication is derived from the current UTC time, by the following formulae:

*DFN*= Floor (0.1\*0.001\* (*Tcurrent* – *Tref – offsetDFN*)) mod 1024

*SubframeNumber*= Floor (0.001\*(*Tcurrent* –*Tref – offsetDFN)*) mod 10

*SlotNumber=* Floor (0.001\*(*Tcurrent – Tref – OffsetDFN*)\*2μ) mod 2μ

Where:

***Tcurrent*** is the current UTC time that obtained from GNSS. This value is expressed in ~~milliseconds~~ microseconds;

***Tref*** is the reference UTC time 00:00:00 on Gregorian calendar date 1 January, 1900 (midnight between Thursday, December 31, 1899 and Friday, January 1, 1900). This value is expressed in ~~milliseconds~~ microseconds;

***OffsetDFN*** is the value *sl-OffsetDFN* if configured, otherwise it is zero. This value is expressed in ~~milliseconds~~ microseconds.

**---------------------------------------------------------- End of Draft TP-------------------------------------------------------**

* It is proposed in [9, MediaTek]
* When GNSS is selected as SyncRef, the slot timing for NR SL operation can be derived from GNSS as such:

slotNumber = Floor (0.001\*(Tcurrent-Tref-OffsetDFN)\*2u) mod 2u,

Wherein u=0,1,2,3 corresponding to the usage or (pre-)configuration of 15, 30, 60, 120khz SCS for SL-SSB respectively.

* When GNSS is selected as SyncRef, OffsetDFN indicates the timing offset for the UE to determine DFN timing for alignment with eNB/gNB timing.
* OffsetDFN is provided per frequency layer.
* DFN for NR sidelink communication is derived by the following formula when GNSS is selected as a synchronization reference. [11, LGE]

DFN= Floor (0.1\*(Tcurrent –Tref–offsetDFN)) mod 1024

SubframeNumber= Floor (Tcurrent –Tref–offsetDFN) mod 10

SlotNumber= Floor ((Tcurrent –Tref–offsetDFN)\*2μ) mod (10\*2μ),

where

Tcurrent is the current UTC time that obtained from GNSS. This value is expressed in milliseconds;

Tref is the reference UTC time 00:00:00 on Gregorian calendar date 1 January, 1900 (midnight between Thursday, December 31, 1899 and Friday, January 1, 1900). This value is expressed in milliseconds;

OffsetDFN is the value sl-OffsetDFN if configured, otherwise it is zero. This value is expressed in milliseconds.

* For DFN derivation from GNSS in NR SL, the formulae for DFN and SubframeNumber are reused from LTE V2X. Slot number is derived as follows, [20, Sharp]

SlotNumber = Floor ( \* (Tcurrent – Tref – offsetDFN)) mod

Send an LS to request RAN2 to capture the above in TS 38.331.

# PSBCH rate matching for extended CP

This issue has been captured in the latest CR.

1 companies [12, Intel] proposed to have the correction on the TS 38.212. In current TS 38.212, the rate matching length for PSBCH in an S-SSB slot with extended CP is 1188 which should be corrected to 1386. The calculation can be found as follows.

* Normal CP: 9 symbols \* 11RBs \* 12RBs \* 3/4 \* 2 (QPSK) = 1782
* Extended CP: 7 symbols \* 11RBs \* 12RBs \* 3/4 \* 2 (QPSK) = 1386

***Proposal 8: For ECP, the output sequence length after PSBCH rate matching should be changed from E=1188 to E=1386.***

------------------------------------------ Start of Draft TP for TS 38.212 ----------------------------------------------

**8.1 Sidelink broadcast channel**

The processing for SL-BCH transport channel follows the BCH according to subclause 7.1, with the following changes:

- Subclause 7.1.1 for PBCH payload generation is replaced by Subclause 8.1.1.

- Subclause 7.1.2 for scrambling is not performed.

- In subclause 7.1.5, the rate matching output sequence length E = 1386 when higher layer paramter *cyclicPrefix-SL* is configured, otherwise, E = 1782.

-------------------------------------------- End of Draft TP for TS 38.212 -------------------------------------------------

# Resource sets for S-SSB transmission

In LTE-V2X, RAN1 agreed that up to 2 or 3 sync resource sets can be configured, and the synchronization procedure is described in RAN2 specifications. For example, if 2 sync resource sets are configured, the UE receives S-SSB in one of the 2 sync resource and transmits S-SSB in another sync resource. In NR V2X, it also needs to clarify that the N S-SSB transmission is only within one sync resource set.

The proposals of resource sets for S-SSB transmission is as follows,

* The number of synchronization resource set is same as LTE-V2X. How to use the sync resource set follows the same mechanism as LTE-V2X. [7, OPPO]
* RAN1 decides whether the configuration of three time-domain resources for SSB transmission is supported in NR. [8, Nokia, NSB]
* Clarify that UE can be configured with two or three synchronization resources, where each NR V2X synchronization resource is (pre)-configured from multiple S-SSBs within S-SSB period in accordance with SCS and FR settings. Use of NR-V2X synchronization resource follows the same mechanism as in LTE-V2X. [12, LGE]
* Indication of synchronization resource should be carried by PSBCH to indicate the set of synchronization resource which the S-SSB belonging to. [14, CATT]

# Timing determination of S-SSB

A UE should be able to determine the frame timing, slot timing, and symbol timing from a received S-SSB, and the specification reflecting this aspect is still not complete.

3 companies discussed about the timing determination of S-SSB in [10, Fujitsu] [12, Intel] [15, Samsung]. 2 companies proposed to complete the current specification by adding the missing component for timing in [10, Fujitsu] [15, Samsung], while [12, Intel] proposed that there is no necessary to introduce additional solution because PSBCH carries DFN and slot index.

The proposals of timing determination of S-SSB are as follows,

* The procedure of UE determining the indexes of slots that include S-SS/PSBCH block in TS 38.213 subclause 16.1 should include the determination of both the SFN that includes S-SS/PSBCH block(s) and the slot index in this SFN that includes S-SS/PSBCH block. [10, Fujitsu]

---------------------------------Start of text proposal-----------------------------------------------------

16.1 Synchronization procedures

----------------------------------------Unchanged parts omitted------------------------------------------

A UE is provided, by *numSSBwithinPeriod-SL*, a number of S-SS/PSBCH blocks in a period of 16 frames. The UE assumes that a transmission of the S-SS/PSBCH blocks in the period is with a periodicity of 16 frames. The UE determines SFNs ~~indexes of slots~~ that include S-SS/PSBCH block by using ~~as~~ +, with the SFN satisfying,

-

and the UE determines the slot indexes in the frame with the SFN including S-SS/PSBCH block according to

-

where,

~~- index 0 corresponds to a first slot in a frame with SFN satisfying~~

- is an ~~a~~ S-SS/PSBCH block index within the number of S-SS/PSBCH blocks in the period, with

- is a slot offset from a start of the period to the first slot including S-SS/PSBCH block, provided by *timeOffsetSSB-SL*

- is a slot interval between S-SS/PSBCH blocks, provided by *timeIntervalSSB-SL*

- is the slot number within a frame for subcarrier spacing configuration μ

----------------------------------------Unchanged parts omitted------------------------------------------

--------------------------------------End of text proposal---------------------------------------------------

* PSBCH carries information on DFN and slot index. Therefore, the full timing information will be available for each S-SSB transmission and thus no additional solutions are needed. [12, Intel]
* Adopt the following TP for Section 16.1 of TS 38.213. [15, Samsung]

**======================== Start of TP for Section 16.1 of TS 38.213 ========================**

16.1 Synchronization procedures

**============================== Unchanged Text Omitted =============================**

A UE is provided, by *numSSBwithinPeriod-SL*, a number of S-SS/PSBCH blocks in a period of 16 frames. The UE assumes that a transmission of the S-SS/PSBCH blocks in the period is with a periodicity of 16 frames. The UE determines indexes of slots that include S-SS/PSBCH block as +, where

- index 0 corresponds to a first slot in a frame with SFN satisfying

- is a S-SS/PSBCH block index within the number of S-SS/PSBCH blocks in the period, with

- is a slot offset from a start of the period to the first slot including S-SS/PSBCH block, provided by *timeOffsetSSB-SL*

- is a slot interval between S-SS/PSBCH blocks, provided by *timeIntervalSSB-SL*

Upon reception of a S-SS/PSBCH block, a UE determines the S-SS/PSBCH block index of the received S-SS/PSBCH block according to

,

where and are an index of a frame and an index of a slot within the frame including received S-SS/PBCH block, provided by the payload of PSBCH of the received S-SS/PBCH block, and is as defined in [4, TS 38.211].

**============================== Unchanged Text Omitted =============================**

**======================== End of TP for Section 16.1 of TS 38.213 ========================**

# Limitation on the S-SSB interval

The proposal on how to define the S-SSB interval is as follows,

* All the (pre-)configured actually transmitted S-SSBs should be within M radio frames [4, Huawei, HiSilicon]
* The value of the interval between neighboring S-SSBs is no more than slots, where μ= 0, 1, 2, 3 for SCS 15, 30, 60, and 120kHz respectively, x is the number of actually transmitted S-SSBs,
* M=1 for dedicated carrier, and M=1 or 2 up to network (pre-)configuration for shared carrier.

# Synchronization to multiple sources

The proposal of synchronization to multiple sources is as follows,

* SL UEs are capable to maintain synchronization to two different synchronization sources. [8, Nokia, NSB]

# SL timing derived from eNB/gNB timing

The proposals of SL timing derived from eNB/gNB are as follows,

* For sidelink transmissions, uplink timing is used for both mode 1 and mode 2 in the carrier where Uu link and sidelink transmission coexist. Otherwise, downlink timing is used. [4,Huawei, HiSilicon]

------------------------------ Start of Text Proposal for TS 38.211----------------------------------------

---------------------------------- < Unchanged parts are omitted > -----------------------------------------

**8.5 Timing**

Transmission of a sidelink radio frame number  from the UE shall start  seconds before the start of the corresponding timing reference frame at the UE. The UE is not required to receive sidelink transmissions earlier than the value of , which is given in [TS 38.133], after the end of a sidelink transmission.

For sidelink transmissions:

If the UE has a serving cell fulfilling the S criterion according to [TS 38.304, clause 8.2]

- The timing of reference radio frame  equals that of downlink radio frame  in the cell with the same uplink carrier frequency as the sidelink and

-  is given by clause 4.2 of [TS 38.213],

Otherwise

- The timing of reference radio frame  is implicitly obtained from [TS 38.213] and

- .

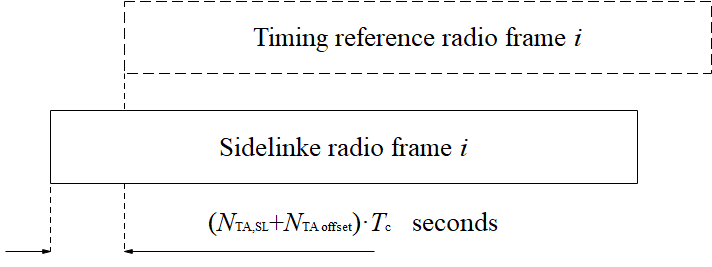


Figure 8.5-1: Sidelink timing relation.

The quantity  differs between channels and signals according to

---------------------------------- < Unchanged parts are omitted > -----------------------------------------

------------------------------------------ End of Text Proposal -----------------------------------------------

* It is proposed in [9, MediaTek]
  + The complexity is very high for sidelink UE to communicate with asynchronous UEs based on multi-cluster synchronization mechanism in NR V2X. Do not introduce multiple-cluster synchronization in NR V2X.
  + Configure the timing difference between eNB and gNB is not feasible especially for the multiple operators’ scenario
* For Scenario 1 (i.e., UEs are synced to GNSS and/or intra/inter-frequency BSs wherein BSs are synced within the same frequency layer and across the frequency layers), the existing signaling OffsetDFN can be used to align GNSS towards BS timing for the common SL timing on V2X frequency layer.
* For Scenario 2 and 3 (i.e., UEs are synced to GNSS and/or intra/inter-frequency BSs wherein BSs are asynced either within the same frequency layer or asynced across the frequency layers), the new signaling, OffsetCommonGNSS (including DFN offset, slot offset and/or symbol offset), is provided by BSs for the corresponding V2X frequency layer to derive the common SL timing from the current serving cell timing based on a common reference GNSS timing.

# Timing offset between eNB and gNB synchronization sources

Since the timing offset between the eNB and gNB cannot always be aligned, and the UE will use eNB or gNB as its synchronization source according to the signal quality, then a timing offset *offetDFN* should be indicated to sidelink UE to align the DFN.

The proposals of timing offset between eNB and gNB sync. source are as follows,

* If a network type synchronization source (eNB or gNB) is (pre-)configured, a timing offset offsetDFN’ between eNB and gNB should be indicated to the sidelink UE such that a unified DFN timing can be derived by sidelink UE. [4, Huawei, HiSilicon]

# eNB/gNB type synchronization as UE capability

With more deployment of SA network over time, it is not suitable to make the eNB as a mandatory synchronization of NR-V2X., becuase the chipset cost will be permanently higher if there is only gNB deployed. It should also be possible to implement a sidelink-only UE which operates using (pre-)configuration without access to Uu-based networks. For such UEs, only GNSS and S-SSB based synchronization sources need be present.

The proposal is as follows,

* Support of eNB and gNB synchronization source for NR V2X UEs should be optional UE capabilities. [4, Huawei, HiSilicon]

# The number of timing references

According to RAN4 discussion, timing between {gNBs and gNBs} or {eNBs and gNBs} will not be aligned in general, and each may be different than GNSS. Thus the network needs to know how much different timing the UE can be configured with. If the UE has to support multiple sidelink timing, the complexities in UE side will be increased with the number of timing. This should depend on the UE implementation and capabilities. The timing number, i.e. no more than 4, is aligned with proposal in UE capability.

The proposal is as follows,

* The supported number of timing for sidelink TX/RX should be an optional UE capability, where the candidate value of timing number could be no more than 4. [4, Huawei, HiSilicon]

# In-device coexistence between LTE-V2X and NR-V2X

The proposal of in-device coexistence between LTE-V2X and NR-V2X is as follows,

* When a UE is configured to operate the in-device coexistence between LTE-V2X and NR-V2X, UE does not transmit NR S-SSB signal. The SL transmission timing and DFN of NR-V2X are derived from those of LTE-V2X. Send LS to RAN2 to define a relevant NR SL synchronization procedure in TS38.331. [11, LGE]

# (Re-)selection of SyncRef in EN-DC/NE-DC network

The proposal of syncRef reselection is as follows,

* The rule of selecting the synchronous reference source is ambiguous for UEs with EN/NE-DC operations. UEs in the EN/NE-DC operation shall always select gNB (or always select eNB) as synchronization reference source by (pre-)configuration when both PCell and PSCell’s RSRP values are higher than a threshold (pre-)configured by network. [9, MediaTek]

# Determination of In-coverage and out-of-coverage

The proposal of determination of IC and OOC is as follows:

* RAN1 further discusses how a UE determines the DL carrier frequency (to perform measurements) based on the pre-configured SL carrier frequency. [20, Sharp]

# Other issues

* Sidelink synchronization under asynchronous cells is considered as an essential leftover issue in Rel.17. [11, LGE]
* For S-SSB RSRP measurement, PSBCH DM-RS and S-SSS can be used as a source. Details are up to UE implementation. [11, LGE]
* For consistency in terminology on downlink pathloss, the following editorial correction is accepted in CR. [11, LGE]

|  |
| --- |
| [dBm],  where   * + - as described in Subclause 7.1.1 |

* Introduce modifications into the RRC specification to implement the agreed reuse of the LTE procedures for NR SL synchronization. [17, Ericsson]
* The same SL BWP should be (pre)configured for both RRC idle (or out of coverage NR V2X UEs) and RRC connected UEs. [18, Spreadtrum]
* Not support that the UE assumes the subcarrier with index 0 in the S-SS/PSBCH block is aligned with a subcarrier with index 0 in the SL BWP. [18, Spreadtrum]

**------------------------------------------------------ Start of Draft TP of 213--------------------------------------------------**

16.1 Synchronization procedures

<Unchanged parts omitted>

For reception of a S-SS/PSBCH block, a UE assumes a frequency location corresponding to the subcarrier with index 66 in the S-SS/PSBCH block [4, TS 38.211], is provided by absoluteFrequencySSB-SL. The UE assumes that a S-PSS symbol, a S-SSS symbol, and a PSBCH symbol have a same transmission power. The UE assumes a same numerology of the S-SS/PSBCH as for a SL BWP of the S-SS/PSBCH block reception, and that a bandwidth of the S-SS/PSBCH is within a bandwidth of the SL BWP.

**---------------------------------------------------------- End of Draft TP -------------------------------------------------------**

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