

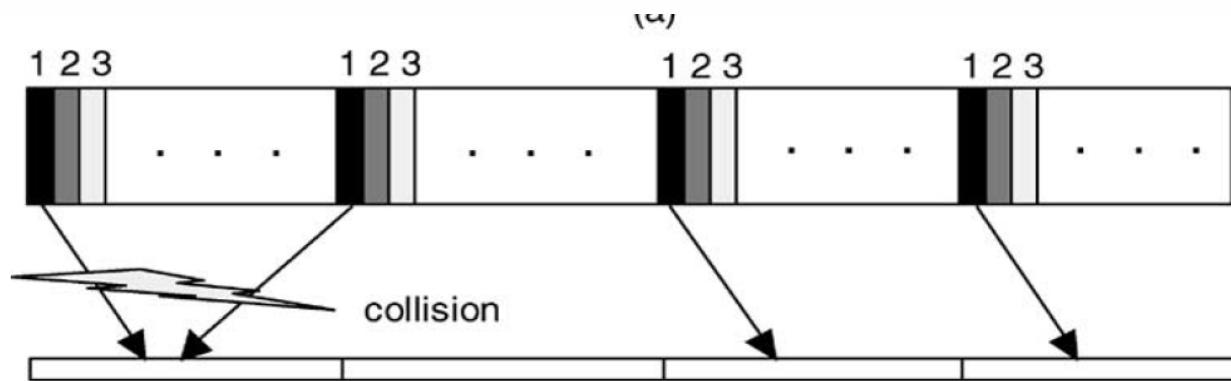
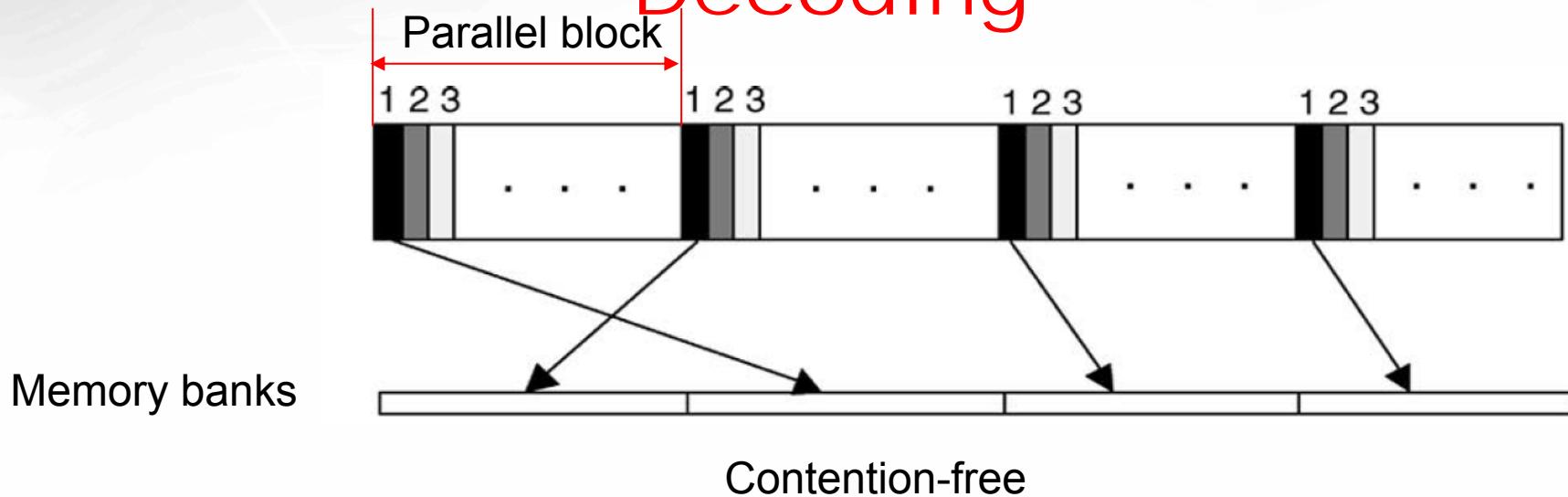


A Contention-Free Memory Mapping for ARP interleaved Turbo Codes of Arbitrary Sizes

Outline

- Parallel turbo decoding and contention-free memory mapping
- Contention-free check on existing memory mappings for ARP
- A general and algebraic, contention-free memory mapping for ARP of all information sizes

Memory Mapping on Parallel Decoding



Partition for Parallel Decoding

Interleave index set $I = \{0, 1, \dots, L - 1\}$ # parallel processors: C (i.e. $L = CW$)

Parallel window 0

0	1	2
W	W+1	W+2

.....

W: window size

Parallel window 1

.....

W+W-1

Parallel window C-1

(C-1)W	(C-1)W+1	(C-1)W+2
.....		

.....

(C-1)W+W-1

Decoding Cycle 0 Decoding Cycle 1 Decoding Cycle 2

Decoding Cycle W-1

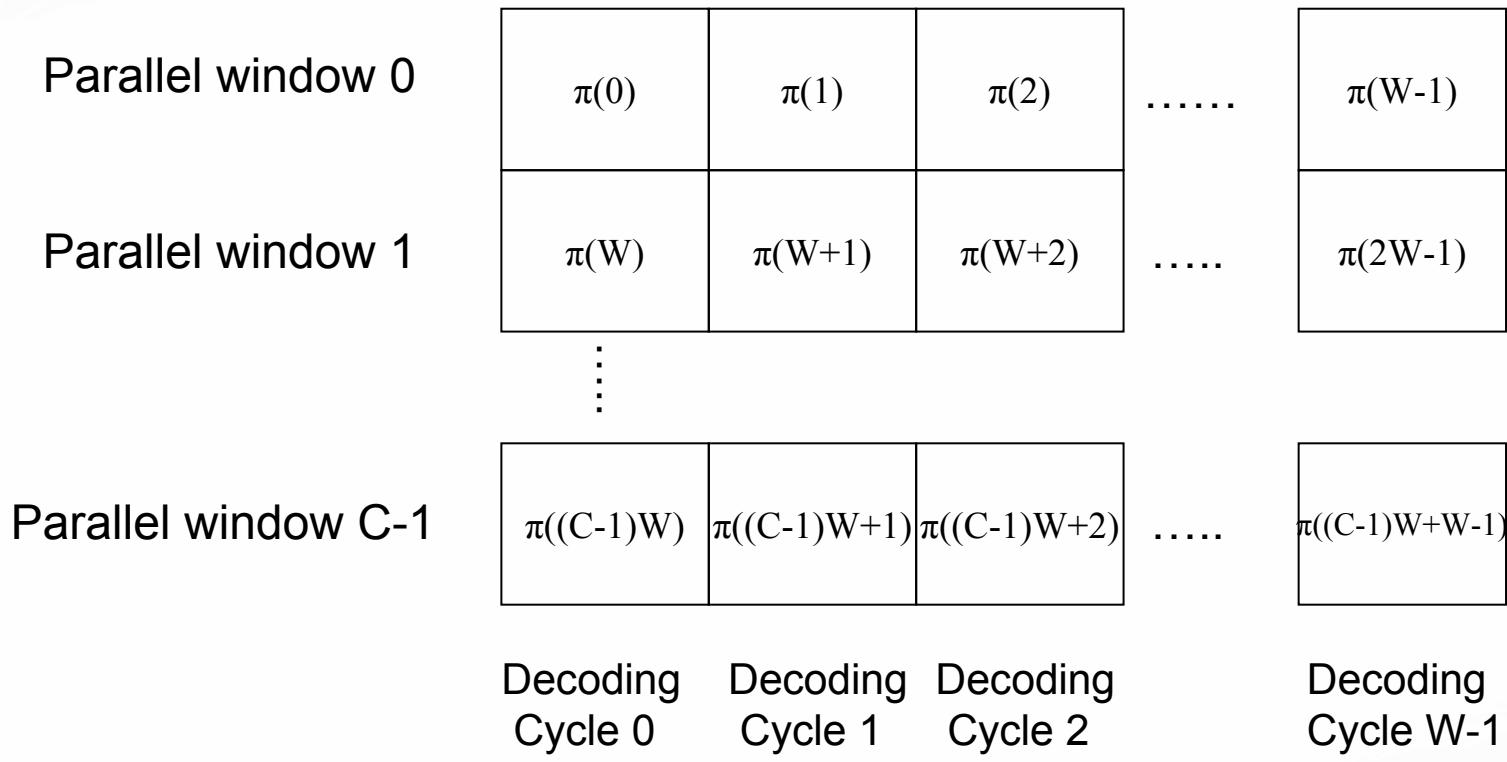
Index set at the i-th decoding cycle

$$E_0 = \{0, W, \dots, (C-1)W\}$$

$$E_i = \{i, W+i, \dots, (C-1)W+i\}$$

Partition for Interleaved Block (π)

Interleave index set $\pi(I) = \{\pi(0), \pi(1), \dots, \pi(L-1)\}$ # parallel processors: C (i.e. L=CW)



Index set at the i-th decoding cycle

$$\hat{E}_0 = \{\pi(0), \pi(W), \dots, \pi((C-1)W)\}$$

$$\hat{E}_i = \{\pi(i), \pi(W+i), \dots, \pi((C-1)W+i)\}$$

Contention Free Memory Mapping

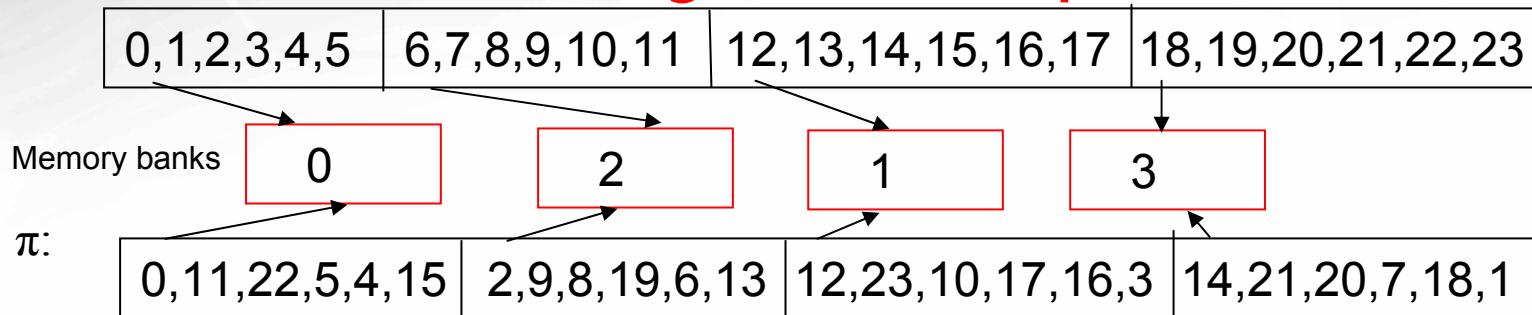
Memory mapping \mathcal{M} is contention-free if

$$j, j' \in E_i \Rightarrow \mathcal{M}(j) \neq \mathcal{M}(j')$$

$$j, j' \in \hat{E}_i \Rightarrow \mathcal{M}(j) \neq \mathcal{M}(j')$$

The elements in the index set of the i-th cycle
should be mapped to different memory banks

Toy Example



Memory mapping on index sets of decoding cycles

Index set of
memory banks

Index set of
memory banks

$$E_0 = \{0,6,12,18\} \rightarrow \{0,2,1,3\}$$

$$\hat{E}_0 = \{0,2,12,14\} \rightarrow \{0,2,1,3\}$$

$$E_1 = \{1,7,13,19\} \rightarrow \{1,3,2,0\}$$

$$\hat{E}_1 = \{11,9,23,21\} \rightarrow \{3,1,0,2\}$$

$$E_2 = \{2,8,14,20\} \rightarrow \{2,0,3,1\}$$

$$\hat{E}_2 = \{22,8,10,20\} \rightarrow \{3,0,2,1\}$$

$$E_3 = \{3,9,15,21\} \rightarrow \{3,1,0,2\}$$

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$$E_4 = \{4,10,16,22\} \rightarrow \{0,2,1,3\}$$

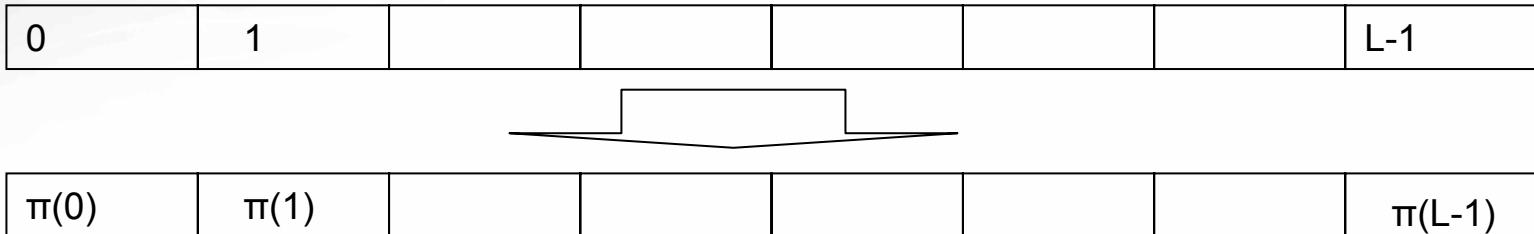
$$\hat{E}_4 = \{4,6,16,18\} \rightarrow \{0,2,1,3\}$$

$$E_5 = \{5,11,17,23\} \rightarrow \{1,3,2,0\}$$

$$\hat{E}_5 = \{15,13,3,1\} \rightarrow \{0,2,3,1\}$$

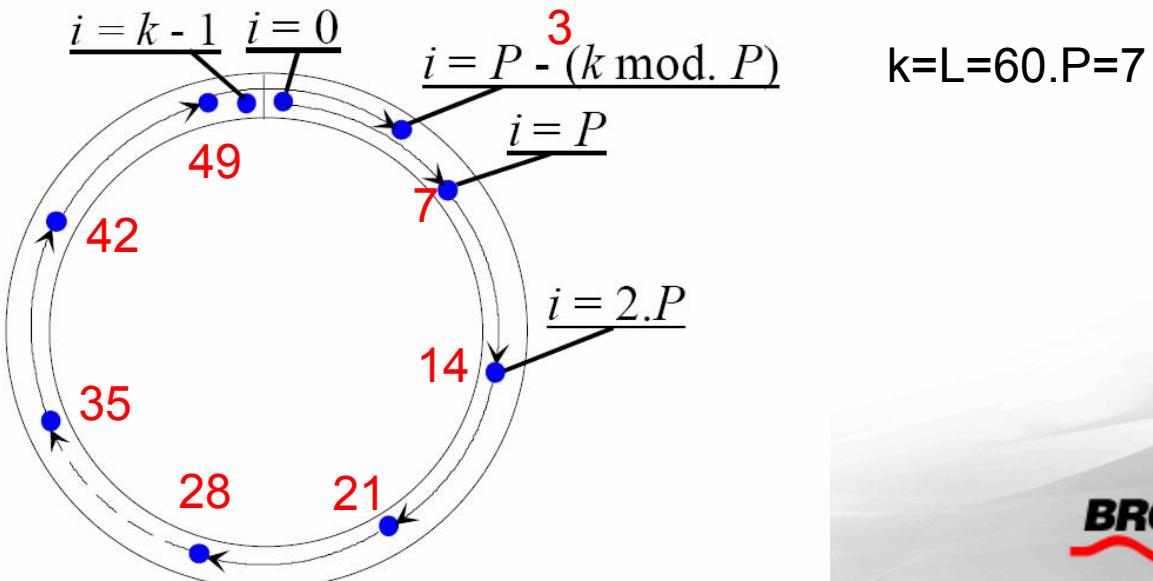
Contention-free

Regular Permutation



Regular (circular) permutation: $i=\pi(j)=Pj \text{ mode } N, 0 \leq i,j \leq L-1$

N is the information frame size, $\gcd(P,L)=1 \rightarrow \pi(j) \neq \pi(j') \text{ if } j \neq j'$



Almost Regular Permutation (ARP)

[1] C. Berrou, Y. Saouter, C. Douillard, S. Kerouédan, and M. Jézéquel,
“Designing good permutations for turbo codes: towards a single model,”
2004 IEEE International Conference on Communications (ICC),
Vol.: 1, pp: 341- 345, 20-24 June 2004.

$$i = \pi(j) = Pj + C[\alpha(j)P + \beta(j)](\text{mod } L)$$

$$C|L \text{ (thus } \gcd(C,P)=1\text{)} \longrightarrow \pi(j) \neq \pi(j'), j \neq j'$$

If $L < 2000$, $C=4$, otherwise larger C is necessary

Example: $C=4$

$$4[\alpha(4l+u)P + \beta(4l+u)] = \begin{cases} 0 & \text{if } u = 0 \\ 4P + 4\beta_1 & \text{if } u = 1 \\ 4\beta_2 & \text{if } u = 2 \\ 4P + 4\beta_3 & \text{if } u = 3 \end{cases}$$



The Toy Example is ARP

$$L = 24, C = 4 \quad P = 7$$

$$\pi(j) = \begin{cases} jP \bmod L & \text{if } j = 0 \bmod 4 \\ (jP + 4) \bmod L & \text{if } j = 1 \bmod 4 \\ (jP + 4P + 4) \bmod L & \text{if } j = 2 \bmod 4 \\ (jP + 4P + 4) \bmod L & \text{if } j = 3 \bmod 4 \end{cases}$$

0,1,2,3,4,5, x 6,7,8,9,10,11, x 12,13,14,15,16,17, x 18,19,20,21,22,23

π

0,11,22,5,4,15,x 2,9,8,19,6,13, x 12,23,10,17,16,3, x 14,21,20,7,18,1



A General Definition Of ARP

L :Information block size, P : Prime to L , C : a factor of L ($L = CW$)

$$w = W \bmod C \quad \theta \in \{0, \dots, C-1\}$$

$A(x)$ and $B(x)$ be integer functions defined on $\{0, \dots, C-1\}$ such that

$$(A(x)P + B(x)) \bmod C = (A(y)P + B(y)) \bmod C \quad \text{if } x = y \bmod w$$

An ARP π of size L is defined by

$$\pi(j) = [Pj + A(j \bmod C)P + B(j \bmod C) + \theta] \bmod L, j \in \{0, \dots, L-1\}$$

C is called period of the ARP



ARP Special Cases

Case 1: $A(x) = C\alpha(x)$ $B(x) = C\beta(x)$

- When $\theta=0$, equations (10), (11) and (12) in [1]
- When $\theta=3$, $C=4$, [2] France Telecom, GET, “Enhancement of Rel. 6 turbo Code,” 3GPP TSG RAN WG1#43, R1-051310, 2005
- When $\theta=3$, $C=4$ and 8, Table 1, [3] Motorola, “A contention-free interleaver design for LTE codes,”, 3GPP TSG RAN WG1#47

Case 2: equations (13) in [1]

DIV Memory Mapping

Division mapping defined by

[4] A. Nimbalker, T. E. Fuja, D. J. Costello, Jr. T. K. Blankenship and B. Classon, "Contention-Free Interleavers," *IEEE ISIT 2004*, Chicago, USA, June 27 – July 2, 2004

$$\mathcal{M}_{DIV} : i \mapsto \lfloor i/W \rfloor$$

(W is the window size of parallel decoding)

Index set at the i -th decoding cycle is $E_i = \{i, W + i, \dots, (C - 1)W + i\}$

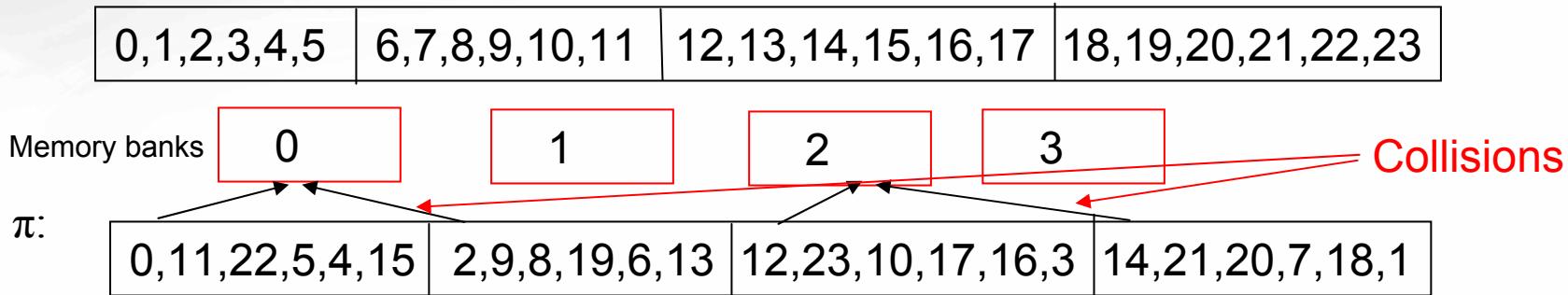
(C is the period of the ARP)

One can prove only when $\gcd(W, C) = W$ or C , this map on ARP is contention-free

Examples on [3] and [4] do not have this property.



Apply DIV Mapping to Toy Example



DIV mapping on index sets of decoding cycles ($\text{gcd}(W,C) \neq W,C$)

$$E_0 = \{0,6,12,18\} \rightarrow \{0,1,2,3\}$$

$$\hat{E}_0 = \{0,2,12,14\} \rightarrow \{0,0,2,2\}$$

$$E_1 = \{1,7,13,19\} \rightarrow \{0,1,2,3\}$$

$$\hat{E}_1 = \{11,9,23,21\} \rightarrow \{1,1,3,3\}$$

$$E_2 = \{2,8,14,20\} \rightarrow \{0,1,2,3\}$$

$$\hat{E}_2 = \{22,8,10,20\} \rightarrow \{3,1,1,3\}$$

$$E_3 = \{3,9,15,21\} \rightarrow \{0,1,2,3\}$$

$$\hat{E}_3 = \{5,19,17,7\} \rightarrow \{0,3,2,1\}$$

$$E_4 = \{4,10,16,22\} \rightarrow \{0,1,2,3\}$$

$$\hat{E}_4 = \{4,6,16,18\} \rightarrow \{0,1,2,3\}$$

$$E_5 = \{5,11,17,23\} \rightarrow \{0,1,2,3\}$$

$$\hat{E}_5 = \{15,13,3,1\} \rightarrow \{2,2,0,0\}$$

Collisions

parallel processors C=4, window size W=6

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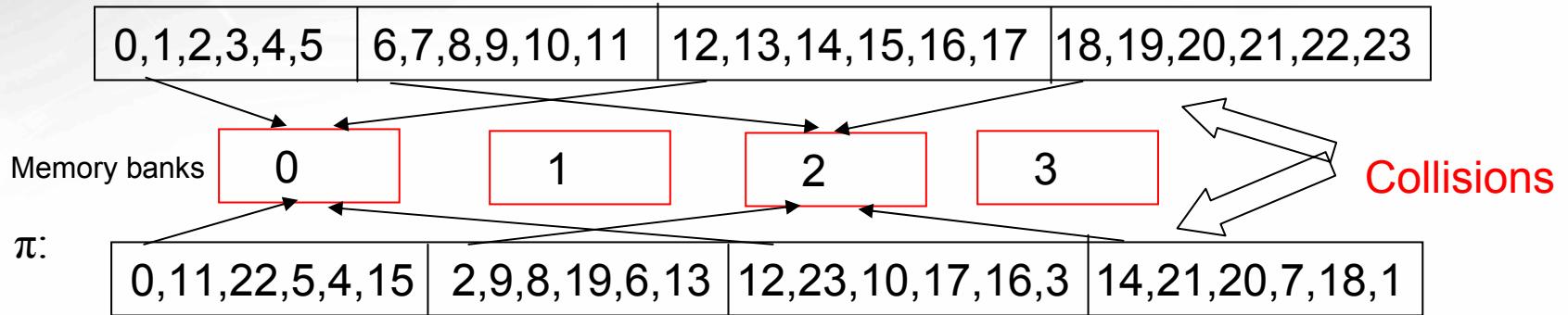
MOD Memory Mappings

Modular mapping suggested in:

- [3] C. Berrou, Y. Saouter, C. Douillard, S. Kerouédan, and M. Jézéquel, "Designing good permutations for turbo codes: towards a single model," *2004 IEEE International Conference on Communications (ICC)*, Vol.: 1, pp: 341- 345, 20-24 June 2004.
- [4] France Telecom, GET, "Enhancement of Rel. 6 Turbo Code," 3GPP TSG RAN WG1#43, R1-051310, 2005

$$\mathcal{M}_{_{MOD}} : i \mapsto i \bmod C$$

Apply MOD Mapping to Toy Example



MOD mapping on index sets of decoding cycles ($W=6$, $C=4$, $\text{gcd}(W,C)\neq 1$)

$$E_0 = \{0,6,12,18\} \rightarrow \{0,2,0,2\}$$

$$E_1 = \{1,7,13,19\} \rightarrow \{1,3,1,3\}$$

$$E_2 = \{2,8,14,20\} \rightarrow \{2,0,2,0\}$$

$$E_3 = \{3,9,15,21\} \rightarrow \{3,1,3,1\}$$

$$E_4 = \{4,10,16,22\} \rightarrow \{0,2,0,2\}$$

$$E_5 = \{5,11,17,23\} \rightarrow \{1,3,1,3\}$$

$$\hat{E}_0 = \{0,2,12,14\} \rightarrow \{0,2,0,2\}$$

$$\hat{E}_1 = \{11,9,23,21\} \rightarrow \{3,1,3,1\}$$

$$\hat{E}_2 = \{22,8,10,20\} \rightarrow \{2,0,2,0\}$$

$$\hat{E}_3 = \{5,19,17,7\} \rightarrow \{1,3,1,3\}$$

$$\hat{E}_4 = \{4,6,16,18\} \rightarrow \{0,2,0,2\}$$

$$\hat{E}_5 = \{15,13,3,1\} \rightarrow \{3,1,3,1\}$$



Collisions

Contention-Free Condition For MOD Memory Mapping

Proposition: if $\text{gcd}(W,C) \neq 1$ $\mathcal{M}_{\text{MOD}} : i \mapsto i \bmod C$ is not contention-free with C processors.

L is interleave size, C is the period of the ARP, $L = CW$

W is the window size of parallel decoding)

Suppose: $\text{gcd}(W, C) = a > 1 \longrightarrow C = aC' \quad (C' < C)$

$\longrightarrow C'W \bmod C = 0$

$\longrightarrow \mathcal{M}_{\text{MOD}}(i) = \mathcal{M}_{\text{MOD}}(i + C'W) \quad \text{i.e. a collision}$

$i, i + C'W \in E_i = \{i, W + i, \dots, (C - 1)W + i\}$

Index set at the i -th decoding cycle

Examples on [3] and [4] all satisfy $\text{gcd}(W, C) \neq 1$ (causing collisions)



A Contention-free Mapping For ARP

We propose the following memory mapping for ARP of arbitrary size

$$\mathcal{M}_B : x \mapsto (x + \left\lfloor \frac{x}{qW} \right\rfloor) \bmod C$$

C: period of ARP, W: window size of parallel decoding

q: the smallest positive integer with property $qW=0 \bmod C$

We proved that this mapping is contention-free for ARP of any size with and C parallel processors

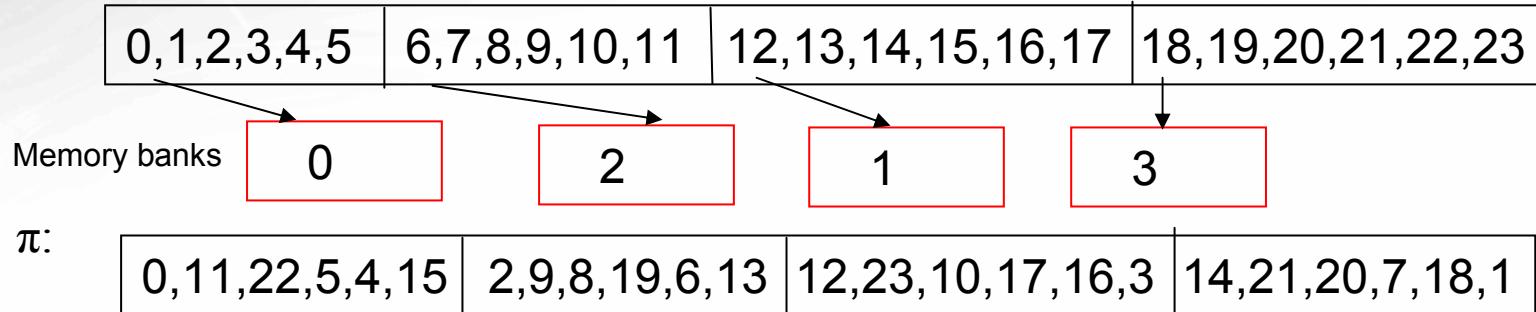
It maps index sets at the i-th decoding cycle to different memory banks

$$E_i = \{i, W+i, \dots, (C-1)W+i\} \mapsto \{0, \dots, C-1\}$$

$$\hat{E}_i = \{\pi(i), \pi(W+i), \dots, \pi((C-1)W+i)\} \mapsto \{0, \dots, C-1\}$$



Application on Toy Example



C=4, W=6, q=2, qW=12

Memory mapping on index sets of decoding cycles

$$E_0 = \{0,6,12,18\} \xrightarrow{\text{mod } 4} \{0,2,0,2\} \quad E_0 = \{0,6,12,18\} \xrightarrow{\lfloor \frac{x}{12} \rfloor} \{0,0,1,1\}$$

$$E_1 = \{1,7,13,19\} \xrightarrow{\text{mod } 4} \{1,3,1,3\} \quad E_1 = \{1,7,13,19\} \xrightarrow{\lfloor \frac{x}{12} \rfloor} \{0,0,1,1\}$$

$$E_2 = \{2,8,14,20\} \xrightarrow{\text{mod } 4} \{2,0,2,0\} \quad E_2 = \{2,8,14,20\} \xrightarrow{\lfloor \frac{x}{12} \rfloor} \{0,0,1,1\}$$

$$E_3 = \{3,9,15,21\} \xrightarrow{\text{mod } 4} \{3,1,3,1\} \quad E_3 = \{3,9,15,21\} \xrightarrow{\lfloor \frac{x}{12} \rfloor} \{0,0,1,1\}$$

$$E_4 = \{4,10,16,22\} \xrightarrow{\text{mod } 4} \{0,2,0,2\} \quad E_4 = \{4,10,16,22\} \xrightarrow{\lfloor \frac{x}{12} \rfloor} \{0,0,1,1\}$$

$$E_5 = \{5,11,17,23\} \xrightarrow{\text{mod } 4} \{1,3,1,3\} \quad E_5 = \{5,11,17,23\} \xrightarrow{\lfloor \frac{x}{12} \rfloor} \{0,0,1,1\}$$

$$E_0 = \{0,6,12,18\} \xrightarrow{\text{mod } 4} \{0,2,1,3\} \quad E_0 = \{0,6,12,18\} \xrightarrow{x + \lfloor \frac{x}{12} \rfloor} \{0,2,1,3\}$$

$$E_1 = \{1,7,13,19\} \xrightarrow{\text{mod } 4} \{1,3,2,0\} \quad E_1 = \{1,7,13,19\} \xrightarrow{x + \lfloor \frac{x}{12} \rfloor} \{1,3,2,0\}$$

$$E_2 = \{2,8,14,20\} \xrightarrow{\text{mod } 4} \{2,0,3,1\} \quad E_2 = \{2,8,14,20\} \xrightarrow{x + \lfloor \frac{x}{12} \rfloor} \{2,0,3,1\}$$

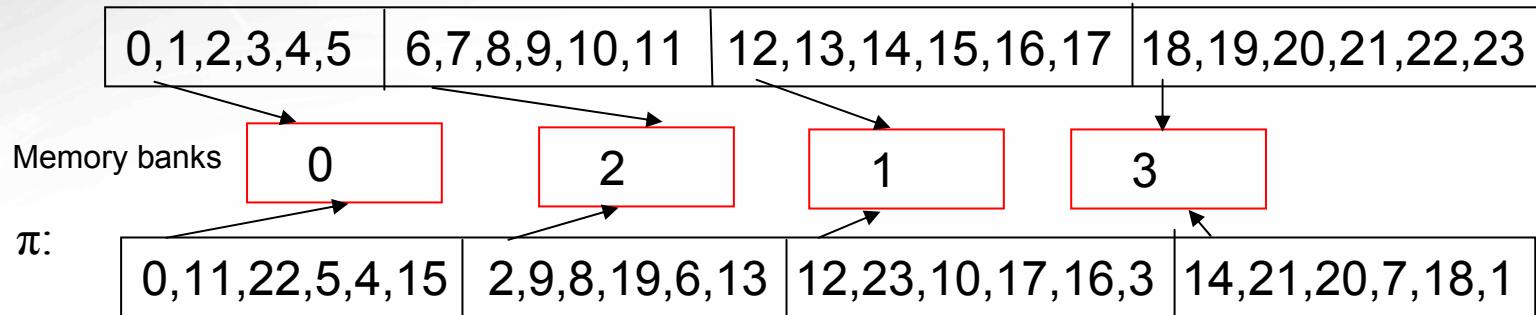
$$E_3 = \{3,9,15,21\} \xrightarrow{\text{mod } 4} \{3,1,0,2\} \quad E_3 = \{3,9,15,21\} \xrightarrow{x + \lfloor \frac{x}{12} \rfloor} \{3,1,0,2\}$$

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$$E_5 = \{5,11,17,23\} \xrightarrow{\text{mod } 4} \{1,3,2,0\} \quad E_5 = \{5,11,17,23\} \xrightarrow{x + \lfloor \frac{x}{12} \rfloor} \{1,3,2,0\}$$

Contention-free

Application on Toy Example



$C=4, W=6, q=2, qW=12$

Memory mapping on index sets of decoding cycles

$$\hat{E}_0 = \{0,2,12,14\} \xrightarrow{\text{mod } 4} \{0,2,0,2\} \quad \hat{E}_0 = \{0,2,12,14\} \xrightarrow{\lfloor \frac{x}{12} \rfloor} \{0,0,1,1\}$$

$$\hat{E}_1 = \{11,9,23,21\} \xrightarrow{\text{mod } 4} \{3,1,3,1\} \quad \hat{E}_1 = \{11,9,23,21\} \xrightarrow{\lfloor \frac{x}{12} \rfloor} \{0,0,1,1\}$$

$$\hat{E}_2 = \{22,8,10,20\} \xrightarrow{\text{mod } 4} \{2,0,2,0\} \quad \hat{E}_2 = \{22,8,10,20\} \xrightarrow{\lfloor \frac{x}{12} \rfloor} \{1,0,0,1\}$$

$$\hat{E}_3 = \{5,19,17,7\} \xrightarrow{\text{mod } 4} \{1,3,1,3\} \quad \hat{E}_3 = \{5,19,17,7\} \xrightarrow{\lfloor \frac{x}{12} \rfloor} \{0,1,1,0\}$$

$$\hat{E}_4 = \{4,6,16,18\} \xrightarrow{\text{mod } 4} \{0,2,0,2\} \quad \hat{E}_4 = \{4,6,16,18\} \xrightarrow{\lfloor \frac{x}{12} \rfloor} \{0,0,1,1\}$$

$$\hat{E}_5 = \{15,13,3,1\} \xrightarrow{\text{mod } 4} \{3,1,3,1\} \quad \hat{E}_5 = \{15,13,3,1\} \xrightarrow{\lfloor \frac{x}{12} \rfloor} \{1,1,0,0\}$$

Contention-free

$$\hat{E}_0 = \{0,2,12,14\} \xrightarrow{x+\lfloor \frac{x}{12} \rfloor} \{0,2,1,3\}$$

$$\hat{E}_1 = \{11,9,23,21\} \xrightarrow{x+\lfloor \frac{x}{12} \rfloor} \{3,1,0,2\}$$

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Extension of the Contention-free Mapping

Let m be any positive integer such that $(mC)|L$

$$\mathcal{M}_{EB} : x \mapsto \left(x + \left\lfloor \frac{x}{q_m W_m} \right\rfloor \right) \bmod mC$$

$W_m = L/(mC)$ window size of parallel decoding

q_m is the smallest positive integer with property $q_m W_m = 0 \bmod mC$

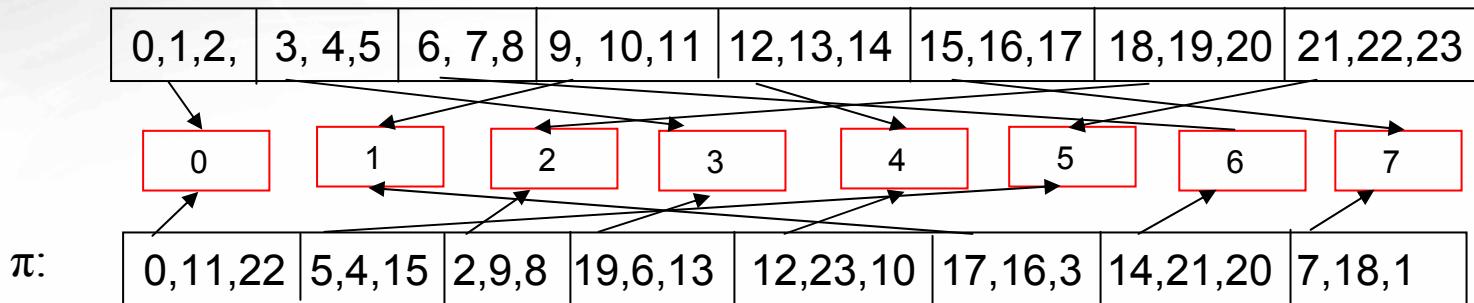
We proved that this mapping is contention –free mapping for ARP of any size with mC parallel processors

It maps index sets at the i -th decoding cycle to the different memory banks

$$E_i(m) = \{i, W_m + i, \dots, (mC - 1)W_m + i\} \mapsto \{0, \dots, mC - 1\}$$

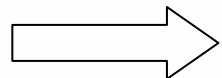
$$\hat{E}_i(m) = \{\pi(i), \pi(W_m + i), \dots, \pi((mC - 1)W_m + i)\} \mapsto \{0, \dots, mC - 1\}$$

ECF Mapping on Toy Example



$$m=2, 2C=8, W_2=3, q_2=8, q_2W_2=24$$

since $q_2W_2 > L-1$, we have $\lfloor x/24 \rfloor = 0, x < L$



$$\mathcal{M}_{EB} : x \mapsto x \bmod 8$$

Memory mapping on index sets of decoding cycles

$$E_0 = \{0,3,6,9,12,15,18,21\} \xrightarrow{\bmod 8} \{0,3,6,1,4,7,2,5\}$$

$$\hat{E}_0 = \{0,5,2,19,12,17,14,7\} \xrightarrow{\bmod 8} \{0,5,2,3,4,1,6,7\}$$

$$E_1 = \{1,4,7,10,13,16,19,22\} \xrightarrow{\bmod 8} \{1,4,7,2,5,0,3,6\}$$

$$\hat{E}_1 = \{11,4,9,6,23,16,21,18\} \xrightarrow{\bmod 8} \{3,4,1,6,7,0,5,2\}$$

$$E_2 = \{2,5,8,11,14,17,20,23\} \xrightarrow{\bmod 8} \{2,5,0,3,6,1,4,7\}$$

$$\hat{E}_2 = \{22,15,8,13,10,3,20,1\} \xrightarrow{\bmod 8} \{6,7,0,5,2,3,4,1\}$$

Contention-free

Conclusion

- We provide a contention-free memory mapping for parallel decoding with ARP of arbitrary size
- Combining this mapping with the one proposed by Motorola, parallel decoding of an ARP interleaved turbo code is now possible using any number of processors M , provided that M is either a multiple of C or M is a factor of L/C .
- ARP interleave is suitable for turbo codes of 3GPP LTE

