
Agenda item : AH24: HSDPA

Source: Texas Instruments

Title: Frame error rate based comparison of full bit level channel interleaving, split bit level channel interleaving and symbol based channel interleaving.

Document for: Discussion and Approval

1. Introduction

In [1] Samsung presented results for enhanced symbol mapping wherein the channel interleaver is split into two by which the systematic bits at the output of the Turbo decoder are allocated the MSB position in 16 QAM modulation and the parity bits are allocated the LSB position. All the results presented in [1] were based upon bit error rate (BER) and performance gains for 16 QAM, rate $\frac{1}{2}$ coding were shown to be on the order of ***0.4 dB for AWGN channels and 1.5 dB for fading channels.***

In this submission we show that in terms of frame error rate (FER) comparison, the gains obtained by the scheme in [1] are lower in the order of ***0.2 dB both for AWGN and fading channels.***

We then propose a scheme to further enhance the FER gains obtained in [1]. We propose

- A symbol level channel interleaver wherein the systematic and the parity bits employ the same channel interleaving for rate $\frac{1}{2}$, 16 QAM.
- A split Turbo code interleaver, one for the odd bits and another interleaver for the even bits.
- This enables to output the systematic bit alternately from the two Turbo encoders. This allows a full symbol level decoding at the receiver.

The performance gains by our proposed scheme in terms of FER for 16 QAM, rate $\frac{1}{2}$ coding over the current HSDPA scheme is 0.35 dB in AWGN, 3 Kmph and 30 Kmph channels and 0.15 dB over the scheme proposed in [1].

2. Performance comparison of split/Full bit level channel interleavers

We refer to the current HSDPA scheme as a full bit level channel interleaver while we refer to the scheme proposed in [1] as the split channel interleaver, because it splits the channel interleaving into systematic and parity bits. The simulation assumptions are given in table1 below:

Table 1: Simulation assumptions comparing the performance of full and split bit level channel interleavers

	Full bit level channel interleaver	Split bit level channel interleaver [1]
Carrier frequency	2 GHz	2 GHz
Chip rate	3.84 Mcps	3.84 Mcps
Frame length	3.33 ms (5-TS)	3.33 ms (5-TS)
Channel coding/decoding	16 QAM rate ½ Max-Log-Map decoding (8 iterations)	16 QAM rate ½ Max-Log-Map decoding (8 iterations)
Channel model	AWGN, 3 Kmph flat fading, 30 Kmph, flat fading	AWGN, 3 Kmph flat fading, 30 Kmph, flat fading
Channel interleaving	Not split: Systematic bits can be either LSB or MSB	Split: Systematic bits always MSB, parity always LSB according to [1]
Turbo interleaver	HSDPA interleaver	HSDPA interleaver
Turbo coding	HSDPA coding	HSDPA coding
Puncturing	HSDPA puncturing	HSDPA puncturing
Channel estimation	Perfect Channel Estimation (PCE)	Perfect Channel Estimation (PCE)
Performance gain over full bit channel interleaving (AWGN)		In BER: ~ 0.4 dB <i>In FER: ~ 0.2 dB</i>
Performance gain over full bit channel interleaving (3 Kmph)		In BER: ~ 1 dB <i>In FER: ~ 0.2 dB</i>
Performance gain over full bit channel interleaving (30 Kmph)		In BER: ~ 1 dB <i>In FER: ~ 0.2 dB</i>

Figures 1-6 give the performance comparison of full and split channel interleavers in terms of BER and FER. From table 1 and figure 1-6 we can see that the gains in terms of BER match those reported in [1]. However, [1] did not report performance gains in terms of FER. We can see that the gains in terms of FER for split bit level channel interleaving over the full bit level channel interleaving are approx. 0.2 dB for all the cases.

We now propose a scheme, which further enhances the FER performance over the split bit level channel interleaving.

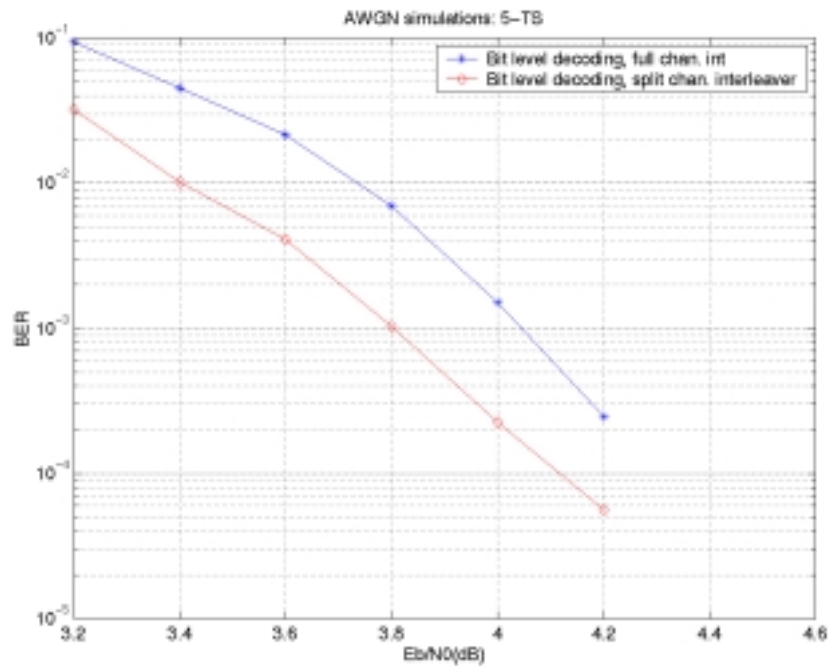


Figure 1: BER comparison of full versus split bit level channel interleaver[1] in AWGN.

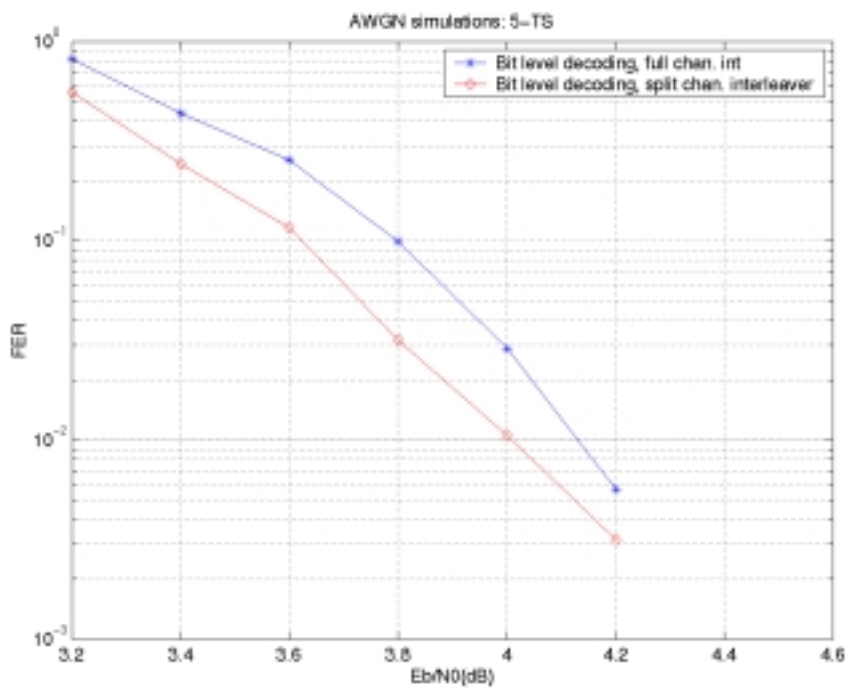


Figure 2: FER comparison of full versus split bit level channel interleaver[1] in AWGN.

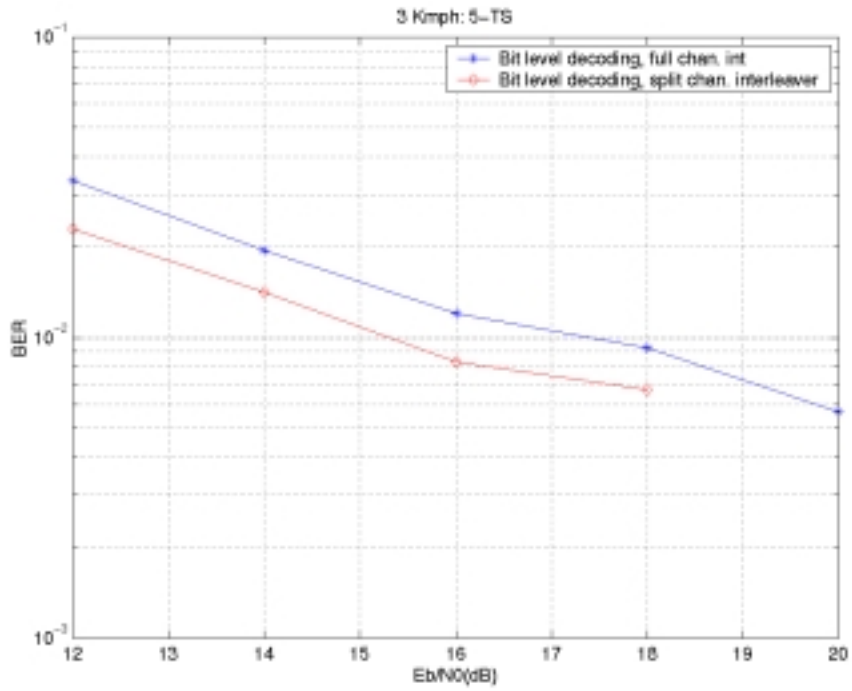


Figure 3: BER comparison of full versus split bit level channel interleaver[1] for 3 Kmph.

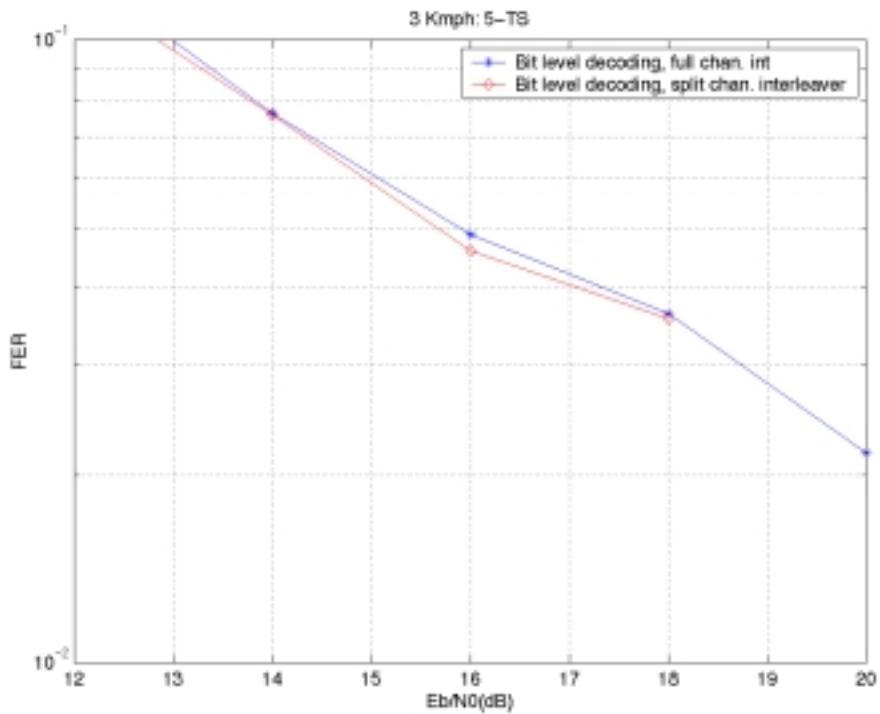


Figure 4: FER comparison of full versus split bit level channel interleaver[1] for 3 Kmph.

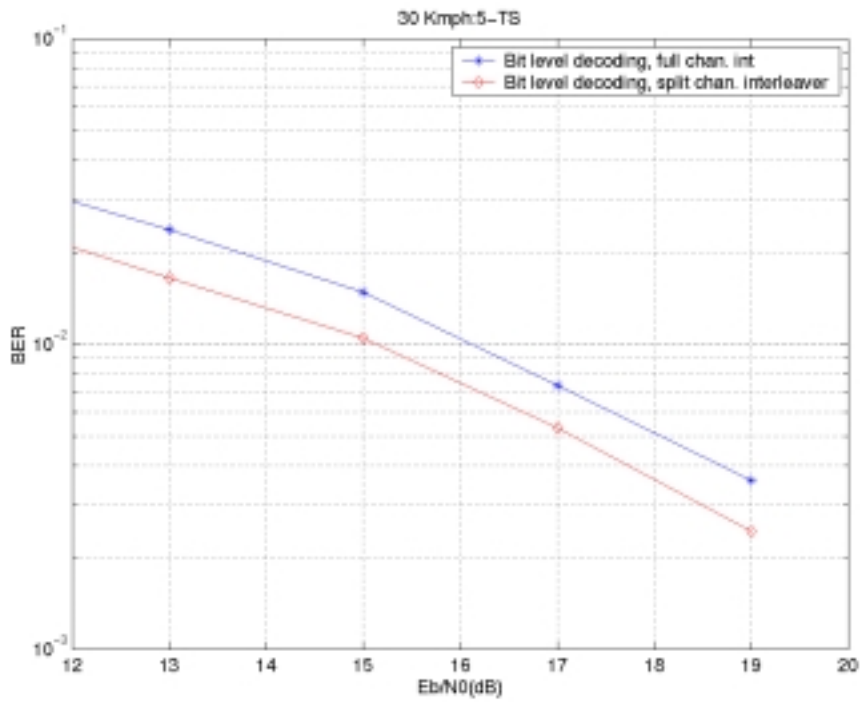


Figure 5: BER comparison of full versus split bit level channel interleaver[1] for 30 Kmph.

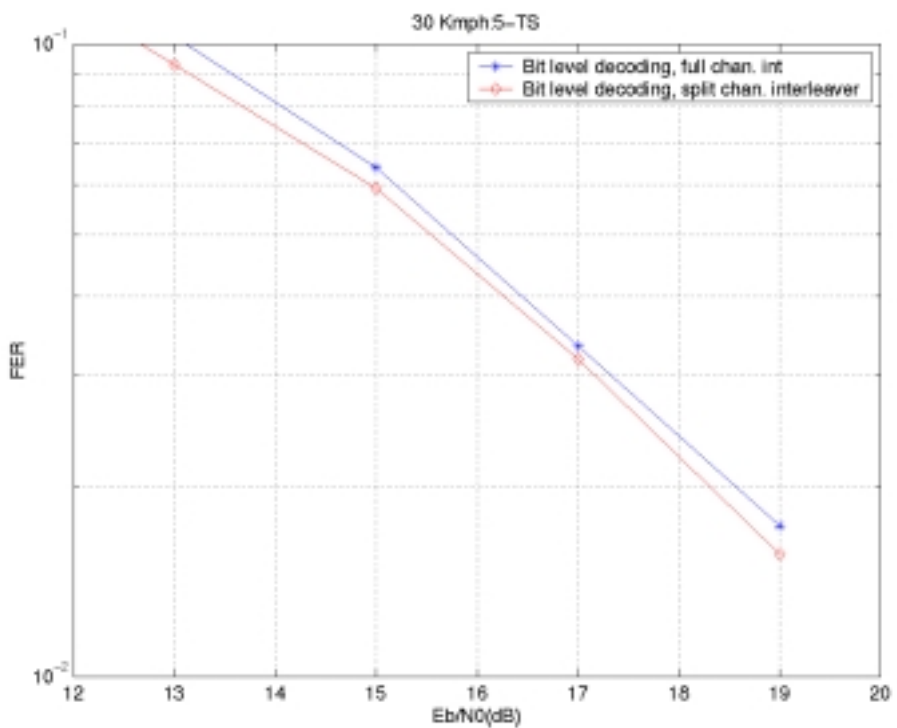


Figure 6: FER comparison of full versus split bit level channel interleaver for[1] 30 Kmph.

3. Symbol level channel interleaving

We now propose to make the following changes for the 16 QAM, rate 1/2 coding in HSDPA:

- (1) We first propose to split the Turbo code interleaver into two half-sized interleavers which are different from each other. This is shown in figure 7 below. Other than splitting the Turbo interleaver, the Turbo code is exactly the same as the current 3Gpp code.

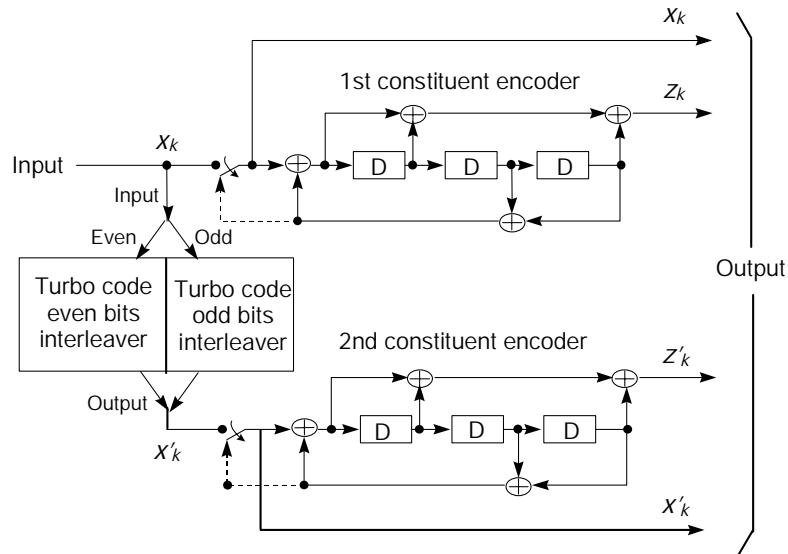


Figure 7: The proposed splitting of the Turbo interleaver is shown.

- (2) Next, we propose to change the puncturing pattern for rate 1/2 coding and employ the following puncturing for rate 1/2 coding:

$$P = \begin{bmatrix} 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 0 \end{bmatrix}$$

The first row is the systematic bit, the second row is the first parity bit and the third row is the second parity bit output from the first component convolutional encoder for the Turbo code. The fourth row is the interleaved systematic bit, the fifth row is the first parity bit and the sixth row is the second parity bit output from the second component convolutional encoder for the Turbo code. Notice that because of splitting the Turbo interleaver as shown in figure 7 and the puncturing employed above, the systematic and parity bits come from the same encoder all the time. This allows the receiver to do a full symbol level decoding without doing bit level demodulation.

(3) We propose to split the channel interleaver in terms of systematic and parity as proposed in [1]. However, we further propose that the two interleavers of the systematic and the parity bits be exactly the same.

4. Simulation comparison of symbol level interleaving, split bit level interleaving and full bit level interleaving

Table 2 below summarizes the simulation parameters and the results. Figures 8-10 show the simulation results.

	Full bit level channel interleaver	Split bit level channel interleaver [1]	Proposed symbol level interleaving
Carrier frequency	Same as in table 1	Same as in table 1	Same as in table 1
Chip rate	Same as in table 1	Same as in table 1	Same as in table 1
Frame length	Same as in table 1	Same as in table 1	Same as in table 1
Channel coding/decoding	Same as in table 1	Same as in table 1	<i>Symbol level, 16 QAM rate 1/2 Max-Log-Map decoding (8 iterations)</i>
Channel model	Same as in table 1	Same as in table 1	Same as in table 1
Channel interleaving	Same as in table 1	Same as in table 1	<i>Symbol level</i>
Turbo interleaver	Same as in table 1	Same as in table 1	<i>Split (figure 7)</i>
Turbo coding	Same as in table 1	Same as in table 1	Same as 3Gpp
Puncturing	Same as in table 1	Same as in table 1	<i>Pattern P in section 3</i>
Channel estimation	Same as in table 1	Same as in table 1	Same as in table 1
Performance gain over full bit level channel interleaving (AWGN)		<i>In FER: ~ 0.2 dB</i>	<i>In FER: ~ 0.4 dB</i>
Performance gain over full bit level channel interleaving (3 Kmph)		<i>In FER: ~ 0.2 dB</i>	<i>In FER: ~ 0.35 dB</i>
Performance gain over full bit channel interleaving level (30 Kmph)		<i>In FER: ~ 0.2 dB</i>	<i>In FER: ~ 0.35 dB</i>

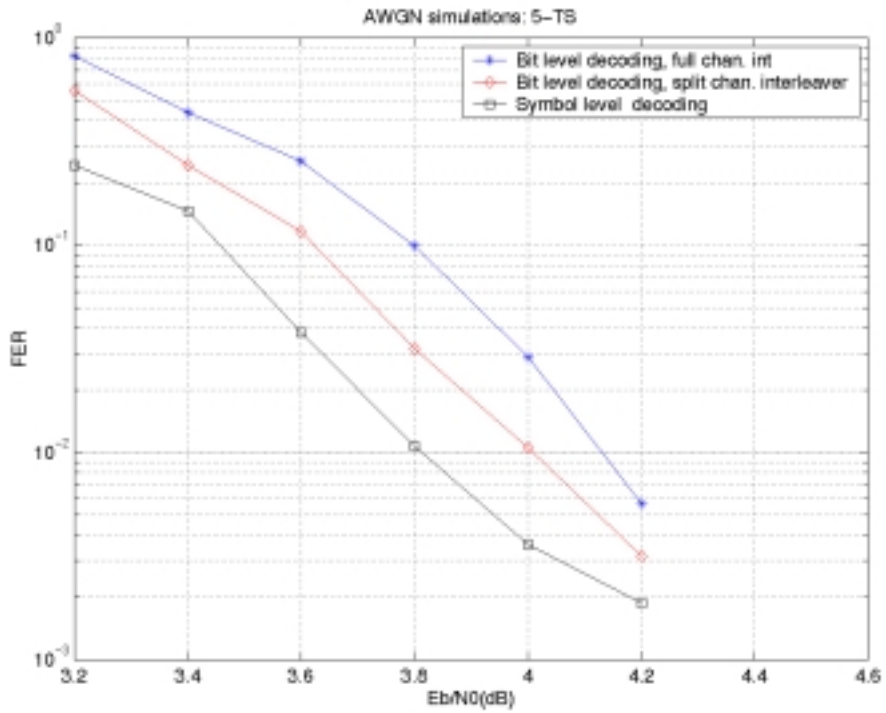


Figure 8: FER comparison of full, split bit level channel interleaver versus symbol level channel interleaver for AWGN.

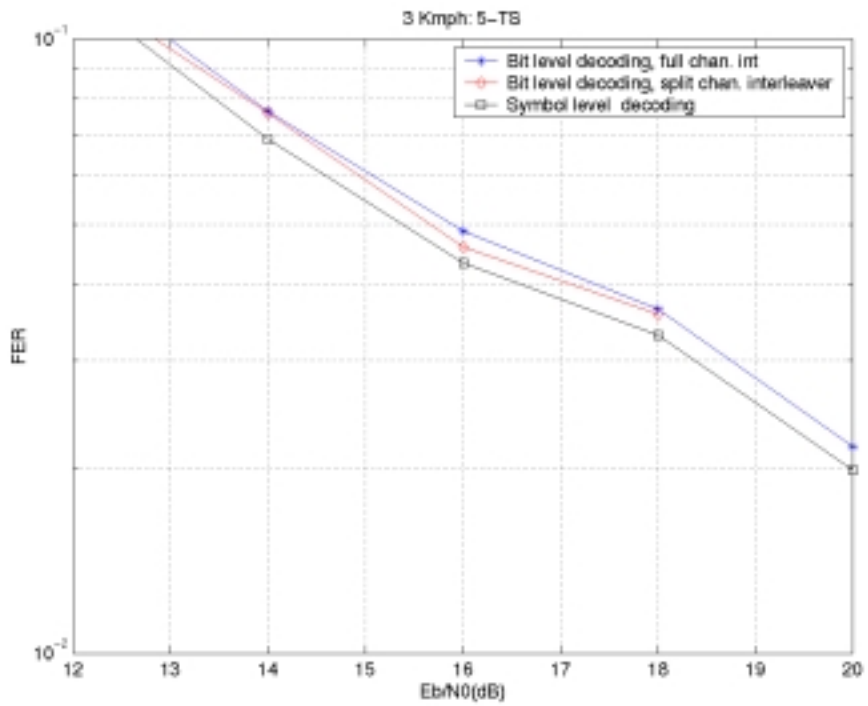


Figure 9: FER comparison of full, split bit level channel interleaver versus symbol level channel interleaver for 3 Kmph.

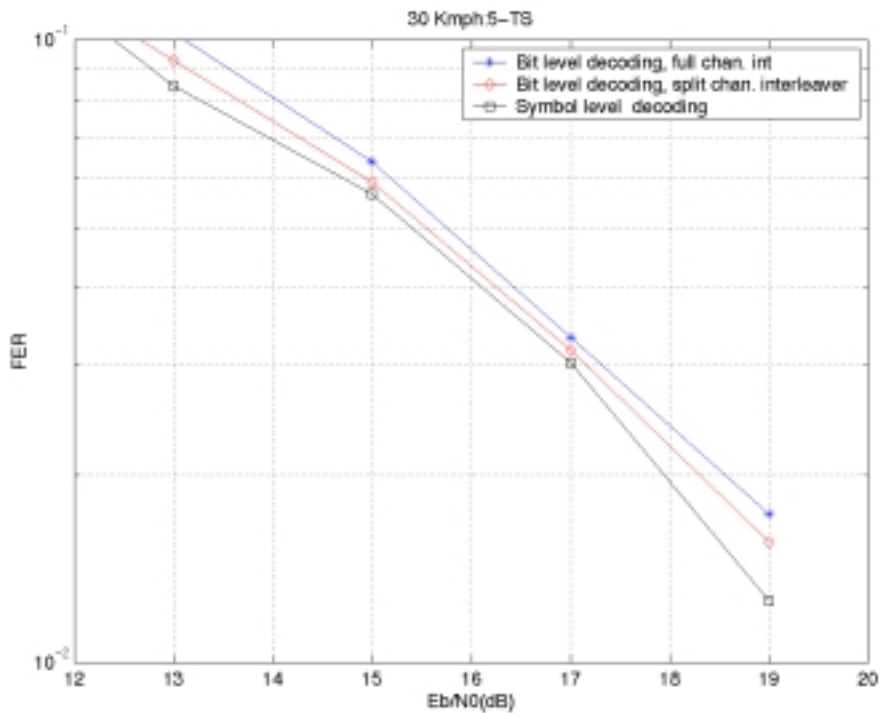


Figure 10: FER comparison of full, split bit level channel interleaver versus symbol level channel interleaver for 30 Kmph.

5. Conclusions

In the first part we compared the performance full bit level channel interleaving to split bit level channel interleaving in [1]. All the results in [1] are based upon BER simulations. However, in practise the FER is more relevant. Hence we show that the simulation results for [1] in terms of FER. We show that [1] has approximately 0.2 dB gain for 16 QAM, rate $\frac{1}{2}$ over the current HSDPA channel interleaving scheme in AWGN, 3 Kmph and 30 Kmph.

In the second part of the proposal we propose symbol level channel interleaving to further improve the performance over the current HSDPA scheme. The advantages of symbol level channel interleaving are as follows:

- (1) The performance the proposed symbol level channel interleaving is approx. 0.35 dB better than the current HSDPA scheme.
- (2) There is no increase in the Turbo decoding complexity of the receiver.
- (3) The receiver can do a full symbol level decoding, without converting the received symbols into bits. For chase combining, the receiver can accumulate symbol level soft decisions and use them directly for Turbo decoding without converting to bits. This avoids the necessity of two buffers at the receiver, one at the bit level for Turbo decoding and another at the symbol level before the channel interleaver for Chase combining.
- (4) Because of symbol level channel interleaving, the size of the channel interleaving remains the same whether QPSK rate $\frac{1}{2}$ or 16 QAM $\frac{1}{2}$ is employed.

Thus, symbol level channel interleaving is better than current HSDPA bit level channel interleaving because of improved performance and reduced buffer requirements.

References

- [1] Samsung Electronics, "Enhanced Symbol Mapping method for the modulation of Turbo-coded bits based on bit priority", Tdoc 12A010044, 3GPP TSG RAN WG1/WG2 Joint Meeting on HSDPA Sophia Antipolis, France April 5-6, 2001
- [2] 3Gpp Technical Specification for Physical Layer Aspects of UTRA High Speed Downlink Packet Access, 3G TR 25.848 V0.6.0.