TSG-RAN Working Group 1 meeting #19

Las Vegas, USA, Feb. 27 - Mar. 2, 2001

Agenda Item: AH21

Source: Siemens AG

To: TSG RAN WG1

Title: Uplink Synchronisation Procedure

Document for: Decision

1. Summary

In 1.28Mcps TDD option, the uplink synchronisation procedure is a physical layer procedure. A physical layer command sent in FPACH is to reach initial and coarse synchronization with Node B. And the physical layer procedure with SS commands in each sub-frame give UE to be UL synchronised with high accuracy to the Node B.

2. Introduction

In 3.84 Mcps TDD option, the timing advance is a complete high layer procedure. However, in 1.28Mcps TDD option, the uplink synchronisation is a physical layer procedure. A physical layer command sent in FPACH is to reach initial and coarse synchronization with Node B. Then SS commands in each sub-frame provide UE to be UL synchronised with high accuracy to the Node B.

The initial value for uplink synchronisation will be determined in the Node B by measurement of the timing of the UpPCH. The received SYNC_UL timing deviation UpPCH_{POS} is sent in the FPACH will be represented as an 11 bit number (0-2047) being the multiple of 1/8 chips which is nearest to received position of the UpPCH. The UE shall adjust the timing of its transmission accordingly in steps of $\pm 1/8$ chips with the UpPCH value in the FPACH.

During a 1.28 Mcps TDD to 1.28 Mcps TDD hand-over takes place the UE shall transmit in the new cell with timing advance TA adjusted by the relative timing difference? t between the new and the old cell:

$$TA_{new} = TA_{old} + 2? t$$

After the initial and coarse uplink synchronisation procedure, the UL Synchronisation with high accuracy is applied in order to enable synchronous CDMA in the UL. This procedure is continuously taking place during connected mode.

The Node B will continuously measure the timing of the UE and send the necessary UL synchronization commands each sub-frame. On receipt of this UL Synchronization command the UE will adjust the timing of its transmissions accordingly in steps of $\pm k/8$ chips or do nothing each M sub-frames.

The default value of M (1-8) and k (1-8) is broadcast in the BCH. The value of M and k can also be adjusted during call setup or readjusted during the call.

Support of UL synchronization is mandatory for the UE.

3. Proposal

We propose to add following paragraphs in the working CR for TS25.224 as the description of timing advance procedure in the 1.28Mcps TDD.

------Beginning of text proposal for working CR for 25.224 ------

5.2	Timing Advance
5.2.1	With UL Synchronization
5.2.1.1	General limits
5.2.1.2	— UpPTS
5.2.1.3	PRACH
5.2.1.4	DPCH and PUSCH
5.2.1.4.1	Out of synchronization handling
5.2.1.5	The establishment of uplink synchronization
5.2.1.5.1	Preparation of uplink synchronization (downlink synchronization)
5.2.1.5.2	Establishment uplink synchronization
5.2.1.6	Maintenance of uplink synchronisation

5.2 UL Synchronisation

5.2.1 General Description

Support of UL synchronization is mandatory for the UE.

5.2.1.1 Preparation of uplink synchronization (downlink synchronization)

When a UE is powered on, it first needs to establish the downlink synchronisation with the cell. Only after the UE has established the downlink synchronisation, it shall start the uplink synchronisation procedure.

5.2.1.2 Establishment of uplink synchronization

The establishment of uplink synchronization is done during the random access procedure and involves the UpPCH and the PRACH.

Although the UE can receive the downlink signal from the Node B, the distance to Node B is still uncertain. This would lead to unsynchronised uplink transmission. Therefore, the first transmission in the uplink direction is performed in a special time-slot UpPTS to reduce interference in the normal time-slots.

The timing used for the UpPCH is set e.g. according to the received power level of DwPCH and/or P-CCPCH.

After the detection of the SYNC UL sequence in the searching window, the Node B will evaluate the timing, and reply by sending the adjustment information to the UE to modify its timing for next transmission. This is done with the FPACH within the following 4 sub-frames. After sending the PRACH the uplink synchronization is established. The uplink synchronisation procedure shall also be used for the re-establishment of the uplink synchronisation when uplink is out of synchronisation.

5.2.1.3 Maintenance of uplink synchronisation

<u>Uplink synchronization is maintained in 1.28Mcps TDD</u> by sending the uplink advanced in time with respect to the timing of the received downlink.

For the maintenance of the uplink synchronization, the midamble field of each uplink burst can be used,

In each uplink time slot the midamble for each UE is different. The Node B may estimate the timing by evaluating the channel impulse response of each UE in the same time slot. Then, in the next available downlink time slot, the Node B will signal Synchronisation Shift (SS) commands to enable the UE to properly adjust its Tx timing.

5.2.2 UpPCH

Open loop uplink synchronisation control is used for UpPCH.

The UE may estimate the propagation delay? t_p based upon the path loss using the received P-CCPCH and/or DwPCH power.

The UpPCH is sent to the Node B advanced in time according to the timing of the received DwPCH.

The time of the beginning of the UpPCH T_{TX-UpPCH} is given by:

 $\underline{T}_{TX-UpPCH} = \underline{T}_{RX-DwPCH} - \underline{2? t_p} + \underline{12*16 T_C}$

in multiple of 1/8 chips, where

T_{TX-UpPCH} is the beginning time of UpPCH transmission with the UE's timing.

T_{RX-DwPCH} is the received beginning time of DwPCH with the UE's timing,

2? tp is the timing advance of the UpPCH (UpPCH_{ADV}).

5.2.3 PRACH

The Node B shall measure the received SYNC UL timing deviation UpPCH_{POS}. UpPCH_{POS} is sent in the FPACH and is represented as an 11 bit number (0-2047) being the multiple of 1/8 chips which is nearest to received position of the UpPCH.

Time of the beginning of the PRACH T_{TX-PRACH} is given by:

 $\underline{T_{TX-PRACH}} = \underline{T_{RX-PRACH}} - (\underline{UpPCH_{ADV}} + \underline{UpPCH_{POS}} - 8*16 \underline{T_{C}})$

in multiple of 1/8 chips, where

T_{TX-PRACH} is the beginning time of PRACH transmission with the UE's timing.

T_{RX-PRACH} is the beginning time of PRACH reception with the UE's timing if the PRACH was a DL channel.

5.2.4 DPCH and PUSCH

The closed loop uplink synchronisation control uses layer 1 symbols (SS commands) for DPCH and PUSCH. After establishment of the uplink synchronisation, NodeB and UE start to use the closed loop UL synchronisation control procedure. This procedure is continuous during connected mode.

The Node B will continuously measure the timing of the UE and send the necessary synchronisation shift commands in each sub-frame. On receipt of these synchronisation shift commands the UE shall adjust the timing of its transmissions accordingly, in steps of ±k/8 chips or do nothing, each M sub-frames.

Textproposal for working CR for 25.224

