TSG-RAN Working Group 1 meeting #18 *TSGR1#18(01)0179*
Boston, U.S.A, January 15-18, 2000

Agenda Item: **AH22**

Source: TSG RAN WG1

Title: Revision of TR25.840 Terminal Power Saving Features including changes to facilitate OL PC during gating and clarifications based on the comments made during R1 #18

Document for: Discussion and Approval

This revised TR includes changes by outer loop power control based on CRC attached to zero length transport block and reflects the agreement on Tdoc R1-01-0032 "Revision of TR 25.840 Terminal Power Saving Features". The comments made during R1#18 are also reflected in the revised TR as follows.

- Terminology is refined.
  - Common terminology "gating" is used as the abbreviation of "gated DPCCH transmission".
  - Instead of "normal gating period" and "embedded DPDCH period", "basic gating period" and "embedded data period" are used, respectively.
- Clarification on detection of DPDCH frame during gating has been made.
- Among the power control parameters, recovery period is removed.
- Clarification on interaction between gating and STTD has been made.
- Clarification on interaction between gating and SSDT has been made.
- Impact to WGs are revised
  - In section 7.1.1, TS 25.212 and TS 25.215 are added.
  - In section 7.1.4, TS 25.133 is added.
- Reference and history sections were corrected according to the comments.
- Minor editorial corrections have been made.

3G TR 25.840 V2.~~0~~1.0 (200~~0~~1-~~1~~12)

Technical Report

3rd Generation Partnership Project; Technical Specification Group Radio Access Network; Terminal Power Saving Features (Release 4)

Keywords
<keyword[, keyword]>

3GPP

Postal address

3GPP support office address
650 Route des Lucioles - Sophia Antipolis
Valbonne - FRANCE
Tel.: +33 4 92 94 42 00 Fax: +33 4 93 65 47 16

Internet
http://www.3gpp.org

Contents

Foreword

This Technical Specification has been produced by the 3rd Generation Partnership Project (3GPP).

The contents of the present document are subject to continuing work within the TSG and may change following formal TSG approval. Should the TSG modify the contents of the present document, it will be re-released by the TSG with an identifying change of release date and an increase in version number as follows:

Version x.y.z

where:

- x the first digit:
  - 1 presented to TSG for information;
  - 2 presented to TSG for approval;
  - 3 or greater indicates TSG approved document under change control.
- y the second digit is incremented for all changes of substance, i.e. technical enhancements, corrections, updates, etc.
- z the third digit is incremented when editorial only changes have been incorporated in the document.

1 Scope

The present document is the Technical Report of the Release 4 work item “Terminal Power Saving Features”.

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

?? References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.

?? For a specific reference, subsequent revisions do not apply.

?? For a non-specific reference, the latest version applies.

[<seq>] <doctype> <#>[([up to and including]{yyyy[-mm]|V<a[.b[.c]]>}[onwards])]: "<Title>".

[1] 3GPP TS 25.214: “Physical Layer Procedures (FDD)”.

[2] 3GPP TR 25.938: “Terminal Power Saving Features (Iur/Iub aspects)”.

[3] R1-00-1069, “Revised uplink interference reduction gain of gated DPCCH transmission”, Samsung

[4] R1-00-1029, “Clarification of UE battery life calculations”, Nokia

[5] R1-00-0686, “Discussion paper on DPCCH gating benefits”, Nokia

[6] R1-00-0856, “UE battery life improvement with DPCCH gating”, Nokia

[7] R1-00-1079, “Proposal of using both tx and rx gating”, Nokia

3 Abbreviations

For the purposes of the present document, the following abbreviations apply:

CFN	Connection Frame Number
DPCCH	Dedicated Physical Control Channel
DPDCH	Dedicated Physical Data Channel
DPCH	Dedicated Physical Channel
DSCH	Downlink Shared Channel
PDSCH	Physical Downlink Shared Channel

4 Background and Introduction

Battery life is an important resource in UE side but there’s few explicit features dedicated to UE battery saving in Release 99 specification. In order to enhance the UE battery life with respect to Release 99, terminal power saving feature is under discussion for Release 4 work item. In this technical report, the requirements and detail solutions are described.

5 Requirements to the Solution

This section describes the requirements to the solution of terminal power saving feature. It includes the level of changes and expected gains with respect to Release 99.

5.1 Level of Changes with respect to Release 99

5.1.1 Gated DPCCH Transmission Scheme in FDD

Detail parameters and procedure of gated DPCCH transmission (hereafter, called gating except for the section title) is covered in subclause 6.1.

5.1.1.1 Required Changes in UE

When a UE supports ~~gated transmission~~gating, the UE should have a capability of determining turn-on and turn-off time slot of uplink and/or downlink for transmission and reception. In gating ~~mode~~, the uplink power should be adjusted based on the power control command in latest downlink turned-on time slot.

5.1.1.2 Required Changes in Node B

When a Node B supports ~~gated transmission~~gating, Node B should be able to determine uplink and/or downlink turn-on and turn-off time slot for transmission and reception. In gating ~~mode~~, the downlink power should be adjusted based on the power control command in latest uplink turned-on time slot.

5.2 Expected Gain with respect to Release 99

5.2.1 Gated DPCCH Transmission Scheme in FDD

5.2.1.1 Expected Gains in UE Side

In Release 99, UE battery life was not considered explicitly as a requirement to the specification. With ~~the gated DPCCH transmission scheme~~gating, UE battery life can be extended with respect to Release 99 by turning off the transmitter intermittently, and also, if desired, by utilising the possibility to turn off the receiver, if 'RX gating DRX cycle' is defined to be greater than one.

5.2.1.2 Expected Gains in Network Side

By using uplink ~~gated DPCCH transmission~~gating, the interference in uplink can be reduced because the transmission rate is reduced. Similarly, by using downlink ~~gated DPCCH transmission~~gating, the interference in downlink can be reduced because the transmission rate is reduced. The reduction in interference level in uplink and downlink can be converted to the increased uplink and downlink capacity.

6 Terminal Power Saving Features

In this section, the solutions for the terminal power saving features are described.

6.1 Gated DPCCH Transmission Scheme in FDD

~~Gated DPCCH transmission~~Gating ~~scheme (hereafter, "gating" or "gating mode" are used interchangeably.)~~ is basically reduced power control rate operation to get power saving and interference reduction by turning off transmission intermittently. Gating can be applied when UTRAN and UE support gating, DSCH and associated DPCH in downlink and DPCH in uplink are set-up between UTRAN and UE, but there is no data to transmit on both uplink and downlink

for a while. UTRAN can initiate the gating by higher layer signalling. UTRAN can terminate the gating by higher layer signalling. Once gating is initiated data with restricted TFS can be transmitted on downlink DPDCH that is associated with DSCH as well as uplink DPDCH, without terminating gating.

There are two kinds of period in ~~gated DPCCH transmission~~gating depending on the transmission of data on DPDCH during gating. In ~~Normal Gating Period~~Basic Gating Period, both DPCCH and DPDCH will contain transmitted bits only in certain slots of the frame. DPDCH is sent in the same slot as DPCCH due to the fact that CRC is attached to zero length transport block to facilitate adequate performance for outer loop power control. If there is no CRC transmitted, i.e., only DPCCH is transmitted, then the outer loop power control target is considered frozen with ~~normal~~basic DPCCH only gating ~~as is done with normal operation~~ ~~DPDCH is not transmitted and~~. ~~t~~This period is described in section 6.1.4.1. However, even during ~~gating mode~~gating, ~~DPDCH~~ non-zero length transport block can be transmitted on DPDCH without terminating the gating exceptionally for the data with restricted TFS. This ~~Embedded DPDCH Period~~Embedded Data Period is described in section 6.1.4.2.

In addition to this, the network signals to the UE the 'RX gating DRX cycle', which defines in which frames ~~the data~~ transmission of non-zero length transport block can start again in downlink during gating. The concept of RX gating and parameter 'RX gating DRX cycle' is described in section 6.1.3.

6.1.1 Related Parameters

When the call is setup, UTRAN and UE negotiate the gating capability and parameters. The parameters controlling the gating operation are:

Table 1. Gating Parameters

Gating Rate	1	1/3	1/5
Gating Mode	Downlink Only	Uplink and Downlink	
TFS restrictions in downlink	Tbd		
TFS restrictions in uplink	Tbd		
RX gating DRX cycle	1	2	4

6.1.2 Initiation and Termination Indication of Gated DPCCH Transmission

The ~~gated DPCCH transmission~~gating can be initiated by the UTRAN's command to UE. ~~Gated DPCCH transmission~~Gating can be terminated by UE's request followed by UTRAN's permission or by UTRAN's notice to UE. That is, UTRAN determines whether ~~gated DPCCH transmission~~gating is initiated or terminated. Gating is initiated and terminated by higher layer ~~signaling~~signalling.

6.1.3 RX gating concept

During gating, it is possible for the network to allow battery savings for the UE also from the UE RX side. This is achieved so that network will signal 'RX gating DRX cycle' to the UE with the other gating parameters. If 'RX gating DRX cycle' >1 then it is possible for the UE to turn off the receiver during certain slots in the frames where it is known beforehand that UTRAN is not transmitting neither DPDCH or DPCCH for the UE.

Thus the 'RX gating DRX cycle' defines the cycle, in which frames the transmission of non-zero length transport block can start again during gating.

The definition is that transmission of non-zero length transport block can start again in radio frame CFN, which fulfils both of the two following relations:

a) CFN mod (RX gating DRX cycle) = 0.

b) CFN mod Fi = 0, where Fi is the number of radio frames in one TTI of the TrCHi carrying a non-zero length transport block [TS25.212].

6.1.3.1 Handover measurements during RX gating

During RX gating all the normal handover measurements are to be made, including initial search measurements. However, it is left for WG4 to define, whether for 'RX gating DRX cycle' >1 the measurement period could be different.

6.1.4 Operation in Gated DPCCH Transmission ~~Mode~~

During ~~gating mode~~gating, data with restricted TFS can be transmitted on DPDCH that is associated with DSCH without terminating the gating. The transmitter operation during ~~when the DPDCH is not transmitted~~ (~~Normal Gating Period~~Basic Gating Period~~)~~ is covered in section 6.1.4.1. The transmitter operation during ~~when the DPDCH is transmitted~~ (~~Embedded DPDCH~~Data Period~~)~~ is covered in section 6.1.4.2. Figure 1 and 2 are the conceptual diagram of "uplink and downlink" and "downlink only" ~~gated DPCCH transmission~~gating, respectively.

6.1.4.1 ~~Normal Gating Period~~Basic Gating Period

During ~~normal gating period~~basic gating period both DPCCH and DPDCH are transmitted in the same slot if CRC is attached to zero length transport block. This is due to the fact that outer loop power control is based on CRC attached to zero length transport block. Thus, the encoded CRC bits will be mapped only to those slots, where DPCCH is also transmitted. Consequently, this requires changes in transport channel multiplexing chains in uplink and downlink. The needed changes in the multiplexing chains are described in section 7.1.1.1. On the other hand, when there is no CRC attached to zero length transport block, i.e., only DPCCH is transmitted, then the outer loop power control target is considered frozen with basic DPCCH only gating ~~as is done with normal operation~~.

6.1.4.1.1 Uplink and Downlink Gating

In ~~Normal Gating Period~~Basic Gating Period in uplink, ~~only~~ the DPCCH is transmitted intermittently together with DPDCH consisting of CRC encoded bits if CRC is attached to zero length transport block ~~-~~and UE shall turn its transmitter on only for the time slots specified in Table 4 and turn its transmitter off in all other time slots.

In ~~Normal Gating Period~~Basic Gating Period in downlink, UTRAN shall turn on the transmission of TPC and PILOT field ~~together with~~ only for the time slots specified in Table 2. And, UTRAN also shall turn on the transmission of DPDCH consisting of CRC encoded bits, if CRC is attached to zero length transport block, ~~-~~only for the time slots ~~specified in Table 2~~in which TPC is transmitted.

In ~~Normal Gating Period~~Basic Gating Period, transmission of TFCI in downlink will depend on the CFN and 'RX gating DRX cycle' value. UTRAN shall turn on the transmission of TFCI

- in all the time slots in the radio frames where CFN mod (RX gating DRX cycle) = 0.
- in only those time slots specified in Table 2 in the radio frames where CFN mod (RX gating DRX cycle) ? 0.

UTRAN shall turn off the transmission in remaining part.

6.1.4.1.2 Downlink Only Gating

In ~~Normal Gating Period~~Basic Gating Period in downlink, UE shall always turn on its transmitter and transmit all the DPCCH fields (PILOT, TFCI, TPC, FBI)) together with DPDCH consisting of CRC encoded bits if CRC is attached to zero length transport block. However, because TPC field in uplink can be updated only for the associated downlink turn-on time slot, downlink power control rate is lower than non-gating operation. Similarly, uplink power control rate is also lower than non-gating operation.

In ~~Normal Gating Period~~Basic Gating Period, UTRAN shall turn on the transmission of TPC and PILOT only for the time slots specified in Table 2. And, UTRAN also shall turn on the transmission of ~~together with~~ DPDCH consisting of

CRC encoded bits, if CRC is attached to zero length transport block, -only for the time slots in which TPC is transmitted~~specified in Table 2~~.

In ~~Normal Gating Period~~Basic Gating Period, transmission of TFCI in downlink will depend on the CFN and 'RX gating DRX cycle' value. UTRAN shall turn on the transmission of TFCI

- in all the time slots in the radio frames where CFN mod (RX gating DRX cycle) = 0.
- in only those time slots specified in Table 2 in the radio frames where CFN mod (RX gating DRX cycle) ? 0.

UTRAN shall turn off the transmission in remaining part.

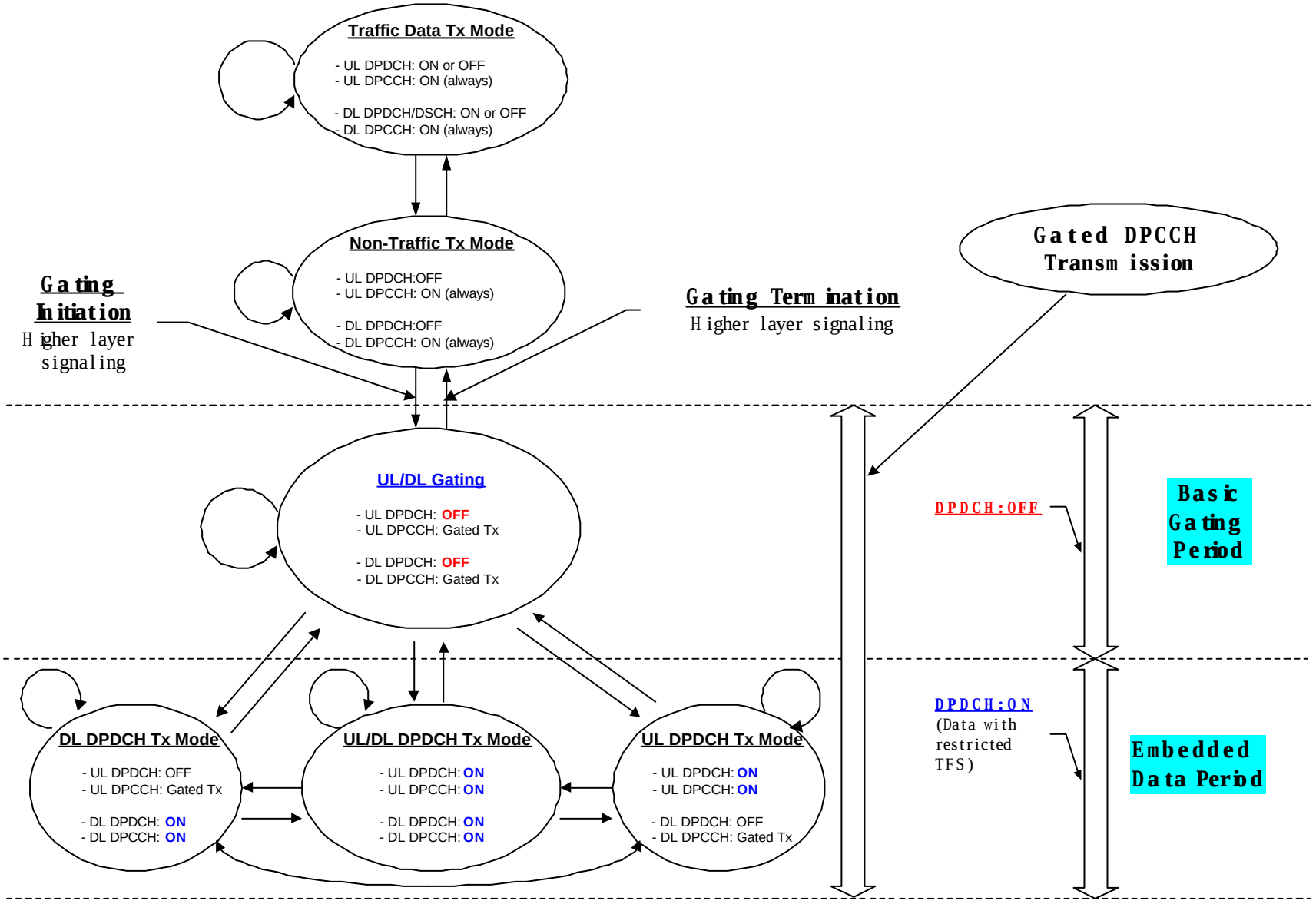

Figure 1. Conceptual Transition Diagram of Gating: Uplink and Downlink Gating

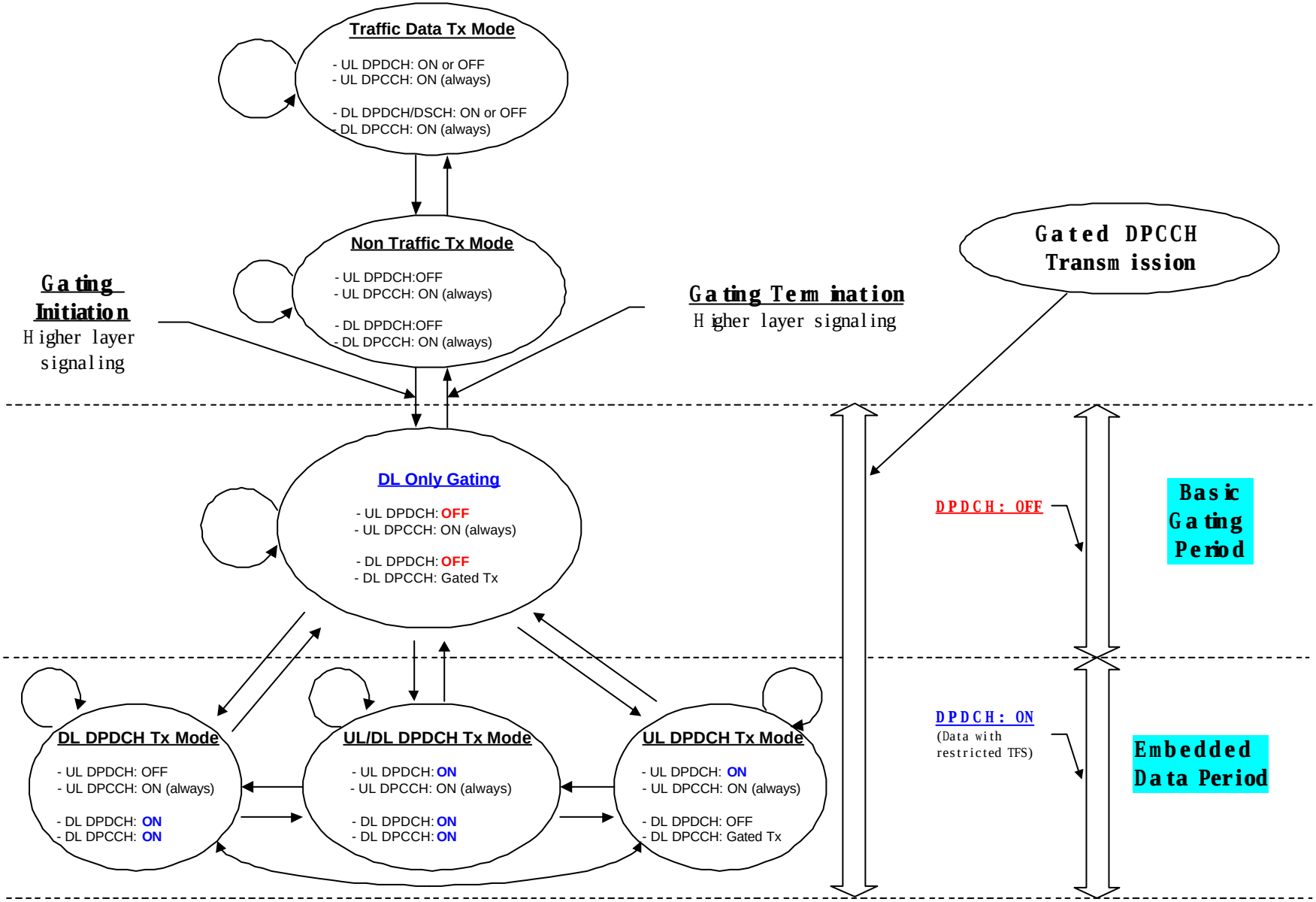

Figure 2. Conceptual Transition Diagram of Gating: Downlink Only Gating

6.1.4.2 ~~Embedded DPDCH Period~~Embedded Data Period

Once gating is initiated, there are a number of necessity and advantages by permitting transmission of data with restricted TFS on DPDCH without terminating the gating. First, unnecessary ~~signaling~~signalling to initiate and terminate gating can be avoided. Second, the average duration of gating can be increased and terminal power consumption and interference can be decreased further. Third, it should be allowed to minimise unnecessary delay in handover procedure. Fourth, it should be allowed to terminate gating by RRC ~~signaling~~signalling. One possible way to restrict the data rate that is permitted to transmit during gating is limiting TFS. If there is a possibility to restrict the allowed TFS during the gating, there will be no problems with capacity or coverage in the cell during the gating, even the required Tx power during the gating is somewhat increased. That is to say, ~~Embedded DPDCH Period~~Embedded Data Period does not affect the cell coverage or capacity at all with restricted data rate.

TTI of TrCH carrying data transmitted during ~~Embedded DPDCH Period~~Embedded Data Period in downlink may only start in a radio frame where CFN is fulfilling both of two following relations:

- CFN mod (RX gating DRX cycle) = 0, and
- CFN mod Fi = 0 , where Fi is the number of radio frames in one TTI of the TrCHi carrying the data [TS25.212].

In ~~Embedded DPDCH Period~~Embedded Data Period in downlink, UTRAN transmits ~~DPDCH~~ non-zero length transport block as well as DPCCH. In ~~Embedded DPDCH Period~~Embedded Data Period in downlink, UTRAN shall turn its transmission on in all the time slots and transmit all the DPCCH fields (PILOT, TFCI, TPC) as specified in Table 3, but TPC shall be updated only for the time slots specified in Table 2.

In ~~Embedded DPDCH Period~~Embedded Data Period in uplink, UE transmits ~~DPDCH~~ non-zero length transport block as well as DPCCH. In ~~Embedded DPDCH Period~~Embedded data period in uplink, UE shall turn its transmitter on in all the time slots and transmit all the DPCCH fields (PILOT, TFCI, TPC, FBI) as specified in Table 5, but TPC shall be updated only at the time slot specified in Table 4.

6.1.5 Detection of DPDCH frame during Gating

During gating, data with restricted TFS can be transmitted in uplink or downlink DPDCH frame, but receiver should detect the ~~transmitted frame~~transmission of non-zero length transport block because the receiver does not know when the transmission exists. UE can determine the existence of downlink transmission of non-zero length transport block~~DPDCH frame~~ by decoding downlink TFCI in the frames defined by RX gating DRX cycle because downlink TFCI field is always transmitted in the frames defined by RX gating DRX cycle length coefficient. In uplink, UTRAN shall not use TFCI to detect the uplink DPDCH frame, since part of uplink TFCI in a frame may not be transmitted. Since pilot bits are transmitted over the whole frame in which complete TFCI is transmitted, ~~O~~one possible solution for the frame detection in UTRAN is the pilot energy comparison. Pilot energy in the uplink time slots that do not contain pilot during gating is compared to pilot energy in those slots that contains pilot during gating. If this is above threshold, then UTRAN decodes the uplink TFCI and uplink DPDCH frame.

6.1.6 DPCCH Switch-On Time Slot

6.1.6.1 Downlink DPCCH Switch-On Time Slot

Table 2 and table 3 show in which time slots UTRAN shall turn on the DPCCH fields in downlink in ~~normal~~ basic gating period and in embedded ~~DPDCH~~data period, respectively. Furthermore, DPDCH carrying encoded CRC bits is mapped to those slots where TPC and TFCI~~PILOT~~ bits are transmitted if CRC is attached to zero length transport block.

In the table, the CFN of the radio frame is denoted by *i*, and the range of the gating group number *j* defined in subclause 6.1.6.3 is *j* = 0, 1, 2, 3, 4 for gating rate 1/3, and *j* = 0, 1, 2 for gating rate 1/5. The function *s(i,j)* used for the reference pattern is defined in subclause 6.1.6.3.

Table 2. Switched-on Time Slots for downlink DPCCH in ~~normal~~ basic gating period.

CFN	Gating Rate	Switched-on Time Slots for downlink DPCCH fields		
		Pilot	TPC	TFCI
CFN mod (RX gating DRX cycle) = 0	1	All slots (0, 1, …, 14)	All slots (0, 1, …, 14)	All slots (0, 1, …, 14)
	1/3	*j* ? 3 + *s*(*i*,*j*) – 1	*j* ? 3 + *s*(*i*,*j*)	All slots (0, 1, …, 14)
	1/5	*j* ? 5 + *s*(*i*,*j*) – 1	*j* ? 5 + *s*(*i*,*j*)	All slots (0, 1, …, 14)
CFN mod (RX gating DRX cycle) ? 0	1	All slots (0, 1, …, 14)	All slots (0, 1, …, 14)	All slots (0, 1, …, 14)
	1/3	*j* ? 3 + *s*(*i*,*j*) – 1	*j* ? 3 + *s*(*i*,*j*)	*J* ? 3 + *s*(*I*,*j*)
	1/5	*j* ? 5 + *s*(*i*,*j*) – 1	*j* ? 5 + *s*(*i*,*j*)	*J* ? 5 + *s*(*I*,*j*)

Table 3. Switched-on Time Slots for downlink DPCCH in embedded ~~DPDCH~~data period.

Gating Rate	Switched-on Time Slots for downlink DPCCH fields		
	Pilot	TPC	TFCI
1	All slots (0, 1, …, 14)	All slots (0, 1, …, 14)	All slots (0, 1, …, 14)
1/3	All slots (0, 1, …, 14)	All slots (0, 1, …, 14)	All slots (0, 1, …, 14)
1/5	All slots (0, 1, …, 14)	All slots (0, 1, …, 14)	All slots (0, 1, …, 14)

6.1.6.2 Uplink DPCCH Switch-On Time Slot

Table 4 and table 5 show in which time slots UE shall turn on the transmission of DPCCH fields in ~~normal~~ basic gating period and in embedded ~~mode~~data period, respectively. In addition, DPDCH carrying encoded CRC bits is mapped to those slots, where DPCCH is also transmitted if CRC is attached to zero length transport block.

Table 4. Switched-on Time Slots for uplink DPCCH in ~~normal~~ basic gating ~~mode~~period.

Gating Rate	Switched-on Time Slots for uplink DPCCH fields Pilot, TFCI, FBI, TPC
1	All slots (0, 1, …, 14)
1/3	*j* ? 3 + *s*(*i*,*j*)
1/5	*j* ? 5 + *s*(*i*,*j*)

Table 5. Switched-on Time Slots for uplink DPCCH in embedded ~~mode~~data period.

Gating Rate	Switched-on Time Slots for uplink DPCCH fields Pilot, TFCI, FBI, TPC
1	All slots (0, 1, …, 14)
1/3	All slots (0, 1, …, 14)
1/5	All slots (0, 1, …, 14)

6.1.6.3 Reference Pattern

15 slots of the radio frame are divided into N gating groups, each group consists of S consecutive slots. For gating rate 1/3, N = 5 and S = 3, and for gating rate 1/5, N = 3 and S = 5. Denote the CFN of the current radio frame by i, i = 0, 1, 2, …, 255. Further define the 19 bit sequence $(a_{18}, a_{17}, \ldots, a_0)$ = (1, 0, 0, 1, 0, 1, 1, 1, 0, 1, 1, 0, 0, 1, 0, 1, 1, 0, 1).

Table 6. Summary of Reference Pattern *s(I, j)*

Parameter	Value	
CFN	0, 1, …, 255 (8bits)	
$a_{18}, a_{17}, \ldots, a_0$	1, 0, 0, 1, 0, 1, 1, 1, 0, 1, 1, 0, 0, 1, 0, 1, 1, 0, 1	
gating rate	1/3	1/5
Number of gating group (N)	5	3
Gating group size (S)	3	5

For CFN i, i = 0, 1, 2, …, 255, concatenated CFN $C_i = i \cdot 256 + i$, and gating group j, the function $s(i, j)$ is defined as

$$s(i,j) = \begin{cases} (A_j + C_i)_{10} \bmod (S-1) + 1, & j = 0 \\ (A_j + C_i)_{10} \bmod S, & j = 1,\ldots,N-2 \\ S-1, & j = N-1 \end{cases}, \quad i = 0,1,\ldots,255$$

where $(X)_{10}$ represents the decimal representation of the number X, and $X + Y$ denotes bit-wise modulo 2 addition of the binary representation of the numbers X and Y. And $A_j = \sum_{k=j}^{j+15} 2^{k-j} a_k$, j=0,1,...,N-2.

6.1.7 Power Control

6.1.7.1 Power Control Parameters

In this subclause, the power control parameters during and after the ~~gated DPCCH transmission~~gating are described.

- DPC_MODE 0

  In DPC_MODE 0, if ~~gated DPCCH transmission~~gating is not initiated, the UE sends a unique TPC command in each slot and the TPC command generated is transmitted in the first available TPC field in the uplink DPCCH.

  During ~~gated DPCCH transmission~~gating, both of the transmit time slot and receive time slot in uplink and downlink are not continuous. UE sends a unique TPC command in each switch-on transmit time slot and the TPC command generated based on the switch-on receive time slot is transmitted in the first available TPC field in the uplink DPCCH.

- DPC_MODE 1

  In DPC_MODE 1, if ~~gated DPCCH transmission~~gating is not initiated, the UE repeats the same TPC command over 3 slots and the new TPC command is transmitted such that there is a new command at the beginning of the frame.

  During ~~gated DPCCH transmission~~gating, DPC_MODE 1 cannot be used because the transmission of DPCCH field is not continuous. One possible solution is that during gating, DPC_MODE 0 is used instead of DPC_MODE 1 without explicit ~~signaling~~signalling.

- Algorithm 1

  In Algorithm 1, if ~~gated DPCCH transmission~~gating is not initiated, UE shall derive a TPC_cmd based on the TPC command(s) received in each slot.

  During ~~gated DPCCH transmission~~gating, the UE derives a unique TPC command in each switch-on downlink time slot and adjust its transmission power in the first available switch-on transmit time slot.

- Algorithm 2

In Algorithm 2, if ~~gated DPCCH transmission~~gating is not initiated, UE shall process received TPC commands on a 5-slot cycle. It emulates smaller step sizes than the minimum power control step specified in subclause 5.1.2.2.1 of [1], or to turn off uplink power control by transmitting an alternating series of TPC commands.

During ~~gated DPCCH transmission~~gating, Algorithm 2 cannot be used because the downlink transmission of DPCCH field is not continuous. One possible solution is that during gating, Algorithm 1 is used instead of Algorithm 2 without explicit ~~signaling~~signalling.

- ~~Recovery period~~

  ~~During gated DPCCH transmission, the power control rate is reduced by the amount of gating rate. In order to compensate the effect of reduced power control rate during gating, power control recovery period is used similarly to compressed mode.~~

- Power control step

  During ~~gated DPCCH transmission~~gating, power control step can be different from ~~non-gating mode~~normal transmission (non-gating) in order to compensate the reduced power control rate.

6.1.7.2 Power Control Procedure

In this subclause, the power control procedure is described.

6.1.7.2.1 Uplink and Downlink Gated DPCCH Transmission

In the case that the ~~gated DPCCH transmission~~gating is enabled for both uplink and downlink, the power control operations are as follows.

Uplink transmit power adjustment

UE shall adjust the transmit power in switched-on time slot in response to the latest valid downlink TPC. The change in uplink transmit power shall take place immediately before the start of the pilot field on the uplink DPCCH.

Uplink TPC generation and transmission

UE shall generate the uplink TPC based on the latest valid downlink switched-on time slot, and shall transmit the TPC on the next valid uplink switched-on time slot

Downlink transmit power adjustment

UTRAN shall adjust the transmit power in switched-on time slot in response to the latest valid uplink TPC. The change in downlink transmit power shall take place immediately before the start of the pilot field on the downlink DPCCH

Downlink TPC generation and transmission

UTRAN shall generate the downlink TPC based on the latest valid uplink switched-on time slot, and shall transmit the TPC on the next valid downlink switched-on time slot

6.1.7.2.2 Downlink Only Gated DPCCH Transmission

In the case that the ~~gated DPCCH transmission~~gating is enabled only for the downlink, then the power control operations are as follows.

Uplink transmit power adjustment

UE shall adjust the transmit power in response to the downlink TPC received in the valid downlink switched-on time slot. And the uplink transmit power shall remain constant until next valid downlink TPC is received. The change in uplink transmit power shall take place immediately before the start of the pilot field on the uplink time slot.

Uplink TPC generation and transmission

UE shall generate and transmit an uplink TPC based on the valid downlink switched-on time slot. And the UE shall transmit the TPC repeatedly before receiving the next valid downlink switched-on time slot.

Downlink transmit power adjustment

UTRAN shall adjust the transmit power in switched-on time slot in response to the repeated uplink TPC(s) which are known to be the same. The change in downlink transmit power shall take place immediately before the start of the pilot field on the switched-on downlink time slot

Downlink TPC generation and transmission

UTRAN shall generate and transmit downlink TPC based on the uplink time slot(s) whose transmit power is known to be the same.

6.1.8 Operation with other Features

In this subclause, the required changes in operation of other features when the features are used with ~~gated DPCCH transmission~~gating are investigated.

6.1.8.1 Transmit diversity

6.1.8.1.1 Open Loop Transmit Diversity

Since STTD encoding is performed for each time slot unit, there does not exist the case that four consecutive bits overlap a slot border. Thus, there's no impact by ~~gated DPCCH transmission~~gating. For the convenience, STTD encoding of DL DPCH described in TS 25.211 is summarized as follows:

- The diversity antenna pilot bit pattern is obtained by STTD encoding only the pilot bits except the case that N_{pilot}=2.
- For N_{pilot} = 2, the diversity antenna pilot pattern is obtained by STTD encoding the two pilot bits with the last two bits (data or DTX) of the second data field (data2) of the slot.
- STTD encoding for the DPDCH, TPC, and TFCI fields is done as described in subclause 5.3.1.1.1 of TS 25.211.

The STTD encoding operation described above clearly reveals that there is no impact by gating.

6.1.8.1.2 Closed Loop Transmit Diversity

When the ~~gated DPCCH transmission~~gating is turned on during closed loop transmit diversity, gating impacts uplink feedback ~~signaling~~signalling. For closed loop transmit diversity Mode 1, it will work without changes. For closed loop transmit diversity Mode 2, one possible solution is that during gating, Mode 1 is used instead of Mode 2 without explicit ~~signaling~~signalling. If the Mode 1 is used instead of Mode 2 during ~~gated DPCCH transmission~~gating, the Tx diversity mode should ~~be~~ return to Mode 2 without explicit ~~signaling~~signalling when the ~~gated DPCCH transmission~~gating is terminated.

6.1.8.2 Compressed mode

If the compressed mode is initiated during ~~gated DPCCH transmission~~gating, gating shall be disabled by higher layer signaling before the compressed mode is initiated by higher layer signaling. It means that the gating should be terminated before inter-frequency and inter-system hard handover. Furthermore, gating is never used during the compressed mode, i.e., during the compressed mode pattern is active.

6.1.8.3 Soft Handover

If any of the Node Bs in the Active set do not support gated transmission, ~~gated DPCCH transmission~~gating shall be disabled. In other words, if a new radio link is setup during ~~gating mode~~gating and the Node B of the newly added radio link does not support gating, then the gating shall be terminated.

6.1.8.4 SSDT

~~Gated DPCCH~~ Gating shall be disabled by higher layer signaling when the soft handover is initiated with SSDT. The termination of gating and the initiation of SSDT can be performed by a single higher layer signaling message. Thus, no additional signalling is required.

7 Impacts to WGs

In this subclause, the technical specifications of each WG that may be impacted by each solution for terminal power saving features are listed.

7.1 Gated DPCCH Transmission Scheme

7.1.1 WG1

TS25.212

7.1.1.1 Changes needed in the transport channel multiplexing chains in TS 25.212

7.1.1.1.1 Physical channel mapping

It is defined in sections 4.2.12.1 and 4.2.12.2, physical channel mapping for uplink and downlink, ~~-~~that during compressed mode, bits are mapped only to certain slots of the frame. Consequently, similar kind of addition is needed for gating, saying that during gating, bits are mapped only to certain slots of the frame. In uplink :

- during ~~normal gating mode~~basic gating period, the bits are mapped only to those slots, where DPCCH is also transmitted.
- during embedded ~~mode~~data period, the bits are mapped to all slots in the frame

In downlink:

- during ~~normal~~basic gating ~~mode~~period the bits are mapped only to those slots where ~~DPCCH~~TPC is also transmitted
- during embedded ~~mode~~data period, the bits are mapped to all slots in the frame

Here : ~~normal~~basic gating ~~mode~~period = frames where only CRCs with zero length TrCH block(s) is (are) transmitted

embedded data ~~mode~~period = frames where at least one non-zero length TrCH block is transmitted

This means that during RX gating [5,6], in every Kth frame UE receiver needs to decode the TFCI, before it knows that in what slots the bits are mapped to. If TFCI defines that there are only zero length transport blocks in the frame, then UE knows that the bits are mapped to only certain slots of the frame. And if TFCI defines that there is at least one non-zero length transport block in the frame, then UE knows that the bits are mapped to all slots in the frame.

The similar procedure is required from Node B in uplink, in every frame. Node B has to use pilot energy comparison to detect whether the frame is in ~~normal gating mode~~basic gating period or in ~~embedded mode~~embedded data period. In ~~embedded mode~~embedded data period all the pilot fields ~~-~~exist. If it detects that the frame is in ~~normal gating mode~~basic gating period, it knows that DPDCH is transmitted in the same slots as DPCCH. If it detects that the frame is in ~~embedded mode~~embedded data period, then it decodes the TFCI, and decodes the data from all slots in the frame.

7.1.1.1.2 2nd Insertion of DTX indication bits in downlink

Presently it is defined in section 4.2.9.2. "2nd insertion of DTX indication bits " that:

- S is the number of bits from TrCH multiplexing
- P is the number of PhCHs bits

- R is the number of bits in one radio frame , including DTX indication bits

Required changes:

1) In ~~embedded mode~~embedded data period, the same definition can be used as before. So no changes are needed.

2) During ~~normal gating mode~~basic gating period, R needs to be replaced by Rgating, where:

- Rgating=R/3 if gating rate=1/3
- Rgating=R/5 if gating rate=1/5

7.1.1.1.3 Rate matching in uplink

Presently it is defined in section 4.2.7. "Rate matching" that:

- $N_{data,j}$ is the total number of bits that are available for the CCTrCH in a radio frame with transport format combination j.

Required changes:

1) In ~~embedded mode~~embedded data period, the same definition can be used as before. So no changes needed.

2) In ~~normal gating mode~~basic gating period, $N_{data,j}$ needs to be replaced by $N_{data,j}^{gating}$, where:

- $N_{data,j}^{gating} = N_{data,j,}$ /3 if gating rate=1/3
- $N_{data,j}^{gating} = N_{data,j}$ /5 if gating rate=1/5

TS 25.214

TS 25.215

7.1.2 WG2

TS 25.301

TS 25.302

TS 25.331

7.1.3 WG3

The impacts of gating to WG3 are described in [2].

7.1.4 WG4

TS 25.101

TS 25.133

8 Performance

8.1 Gated DPCCH Transmission Scheme

8.1.1 Uplink Interference Reduction Gain [31]

In gating ~~mode~~, the following transmission cases are possible.

- DPCCH only transmission
- DPDCH and DPCCH transmission

That is, as shown in Figure 3, DPCCH is always transmitted but DPDCH can be transmitted when there's data to transmit during gating mode. (Here, for example, DPDCH transfers data with restricted TFS such as ~~signaling~~signalling message that is usually transmitted occasionally. Let "DPDCH frequency" be the probability of transmitting DPDCH during gating mode.)

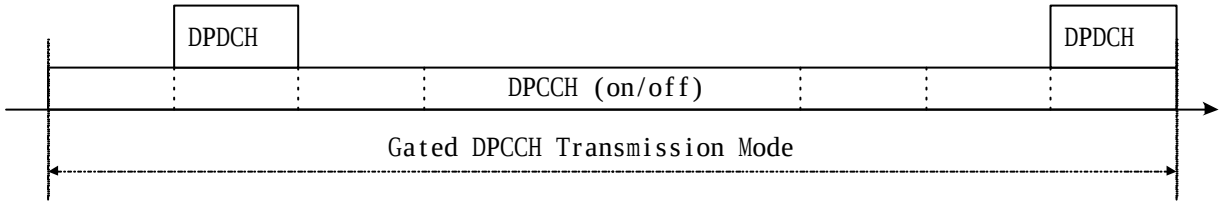

Figure 3. DPDCH Transmission during ~~gated DPCCH transmission~~gating ~~mode~~

The average interference reduction gain is defined as:

Average Uplink interference reduction gain

= (average transmit power when no gating)/(average transmit power when gating)

Note that the average uplink interference reduction gain is defined as the ratio of the average transmission power. Although the transmit power of DPDCH should be increased to compensate the reduced power control rate, the transmit power can be saved during DPCCH only transmission period. Thus the average interference reduction gain highly depends on the DPDCH frequency, and the results are shown with respect to the DPDCH frequency ranges from 1% to 30%.

Simulation and analysis results show that the average interference reduction gain is 4~6dB if the DPDCH frequency is 1%, 2.0~2.5dB if the DPDCH frequency is 10%. Since the average interference reduction gain is the ratio of average transmit power, the ~~gated DPCCH transmission~~gating provides gain in terms of UE Tx power saving.

8.1.1.1 Link level simulation

8.1.1.1.1 Simulation parameters

The link-level simulation was performed to evaluate the required Eb/No of uplink DPDCH during ~~gated DPCCH transmission~~gating ~~mode~~. Note that the performance of the uplink DPDCH depends on the uplink power control rate (downlink TPC rate). More precisely, the FER of uplink DPDCH is simulated when the downlink TPC is transmitted with rate 1, 1/3, and 1/5. The channel models are CASE1 for 3km/h and CASE3 for 120km/h. The detail simulation parameters are shown in table 7.

Table 7. Simulation parameters (uplink)

Carrier frequency		2.0 GHz
Chip rate		3.84 Mcps
Channel bit rate	DPDCH	60 kbps
	DPCCH	15 kbps
Modulation	Data	BPSK
	Spreading	QPSK
Slot structure	DPCCH	Pilot: 6, TPC: 2, TFCI: 2
	DPDCH	Data: 40
Channel model	Multi-path fading	2-path Rayleigh
	Finger	2 fingers
	Receiver antenna diversity	On
	Doppler frequency [Hz]	5.6(3km/h) , 222(120km/h)
DPCCH/DPDCH [dB]		-5dB
Power control	Dynamic range	Unlimited (assume ideal power amplifier)
	Step size	1.0 dB
	Rate	1500Hz(1/1 gating = no gating), 500Hz(1/3 gating), 300Hz(1/5 gating)
	TPC error	4%
Channel estimation		WMSA

8.1.1.1.2 Simulation results

Figure 4 and 5 show the uplink DPDCH FER when the downlink TPC is transmitted with rate 1, 1/3, and 1/5, where R represents gating rate.

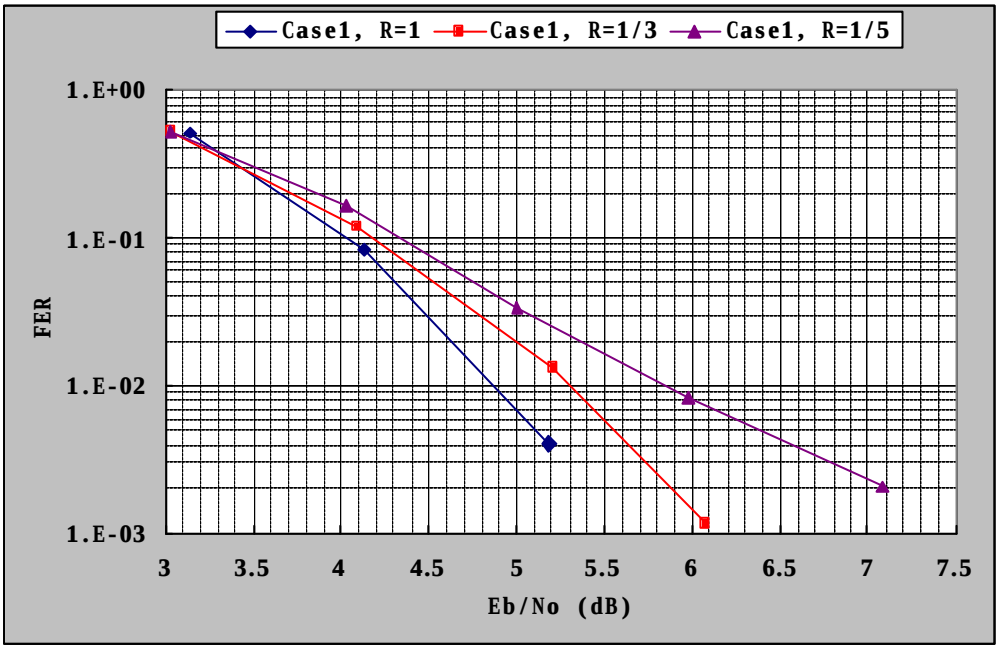

Figure 4. Uplink DPDCH Frame Error Rate with various gating rate and speed (Case 1)

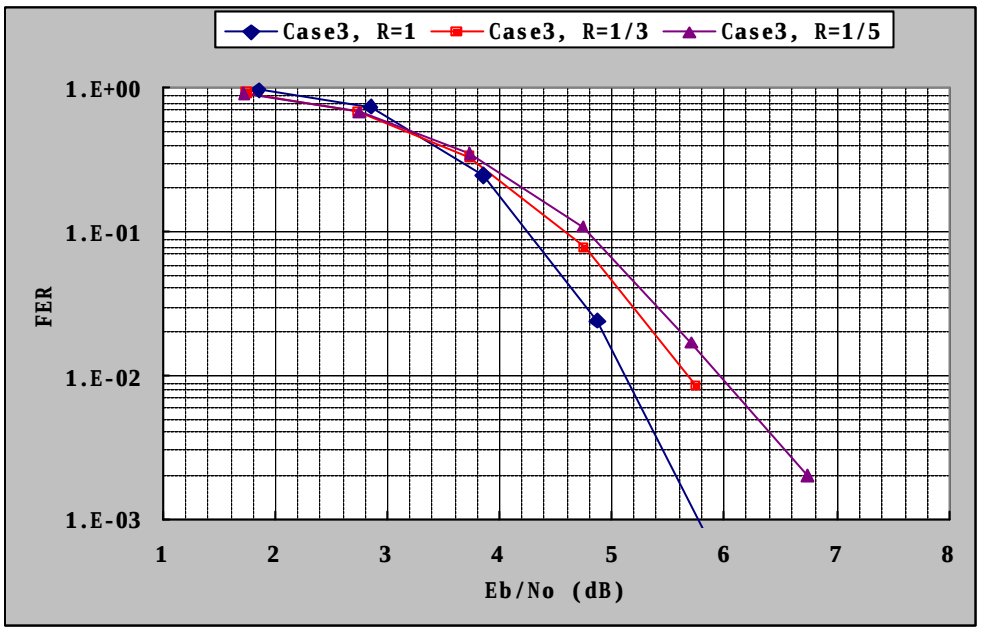

Figure 5. Uplink DPDCH Frame Error Rate with various gating rate and speed (Case 3)

The required transmit Eb/No for the uplink DPDCH to obtain 1% FER is summarised in table 8. In addition, the Eb/No difference compared with gate rate 1 is also given. From the results, we can see that the Eb/No loss by 1/3 rate gating at 3km/h is about 0.42dB, for example. The uplink DPCCH performance loss, which is measured by TPC BER, due to ~~gated DPCCH transmission~~gating is max. 0.5dB for gating rate=1/5.

Table 8. Required Tx E_b/N_0[dB] to maintain 1% FER

UE speed	Gating Rate		
	1/1	1/3	1/5
Case1(3km/h)	**4.88**	5.3(+0.42)	5.88(1.0)
Case3(120km/)h	**5.1**	5.68(0.58)	6.0(0.9)

* ( ) indicates Eb/No difference compared with 1/1(no gating)

Tx. E_b = E_{DPDCH} + E_{DPCCH} per one antenna

8.1.1.2 Uplink Interference Reduction Gain

In this subsection we analyse the average uplink interference reduction gain in ~~gated DPCCH transmission~~gating ~~mode~~ based on the link simulation results in subsection 8.1.1.1. The disadvantage of the ~~gated DPCCH transmission~~gating is the increase of the required Eb/No to obtain 1% DPDCH FER. In addition, the transmit power of DPCCH also should be increased due to reduced uplink power control rate. The average uplink interference reduction gain is defined at the beginning of section 8.1.1 and restated for convenience.

Average uplink interference reduction gain

= (Average transmit power when no gating)/(Average transmit power when gating)

In order to see the gain, let's assume the following parameters.

F = DPDCH frequency (%),

R = Gating rate (1, 1/3, or 1/5)

P_{DPCCH} = Power of DPCCH,

P_{DPDCH} = Power of DPDCH = ? ? P_{DPCCH} (? =5dB)

A_{DPCCH} = Additional Eb/No required for DPCCH only transmission (0.5dB)

A_{DPCH} = Additional Eb/No required for DPDCH+DPCCH transmission (Given in table 8)

From the assumed parameters, only DPCCH is transmitted in (1-F)% of time, and both (DPDCH+DPCCH) are transmitted in F% of time. The average uplink interference reduction gain is defined as the ratio of average transmission power as follows.

Average Uplink Interference Reduction Gain

Average uplink interference reduction gain = 10 * log10 (P(no gating)/P(gating))

where P(no gating) and P(gating) represents the average transmit power when the ~~gated DPCCH transmission~~gating is disabled and enabled, respectively.

P(no gating)

The average transmit power when the ~~gated DPCCH transmission~~gating is disabled is given by

P(no gating) = (Average transmit power when no gating) = (100-F) * P_{DPCCH} + F * (P_{DPCCH} + P_{DPDCH}) = (100+??F) P_{DPCCH}

P(gating)

The average transmit power when the ~~gated DPCCH transmission~~gating is enabled is given by

P(gating) = (Average transmit power during only DPCCH transmission when gating) + (Average transmit power during (DPDCH+DPCCH) transmission when gating)

During DPCCH only transmission period, the average transmit power is given by

(Average transmit power during only DPCCH transmission when gating) = (100-F) * P_{DPCCH} * 10^(0.1*A_{DPCCH})* R

During both (DPDCH+DPCCH) transmission period, there is E_{DPCH} loss, so the required power is

(Average transmit power during (DPDCH+DPCCH) transmission when gating) = F * (P_{DPCCH} + P_{DPDCH}) * 10^(0.1*A_{DPCH}).

Based on the above method, we calculate the average uplink interference reduction gain for 1% DPDCH frequency as table 9 (F=1).

Table 9. Uplink interference reduction [dB] (1% DPDCH frequency)

UE speed	Overall interference reduction gain [dB]	
	1/3	1/5
3km/h	**3.94**	**5.75**
120km/h	**3.93**	**5.77**

Consequently, in case of 1% DPDCH frequency, the uplink interference reduction gain (~5.77dB) can be achieved by ~~gated DPCCH transmission~~gating in spite of increasing transmission power of DPDCH during gating. The DPDCH frequency has an important role in the uplink interference reduction gain. Figure 6 shows the average uplink interference reduction gain against the DPDCH frequency. From this figure, we can see that more than 2.5dB gain can be achieved when the DPDCH frequency is 10%, and the gain increases as the DPDCH frequency decreases.

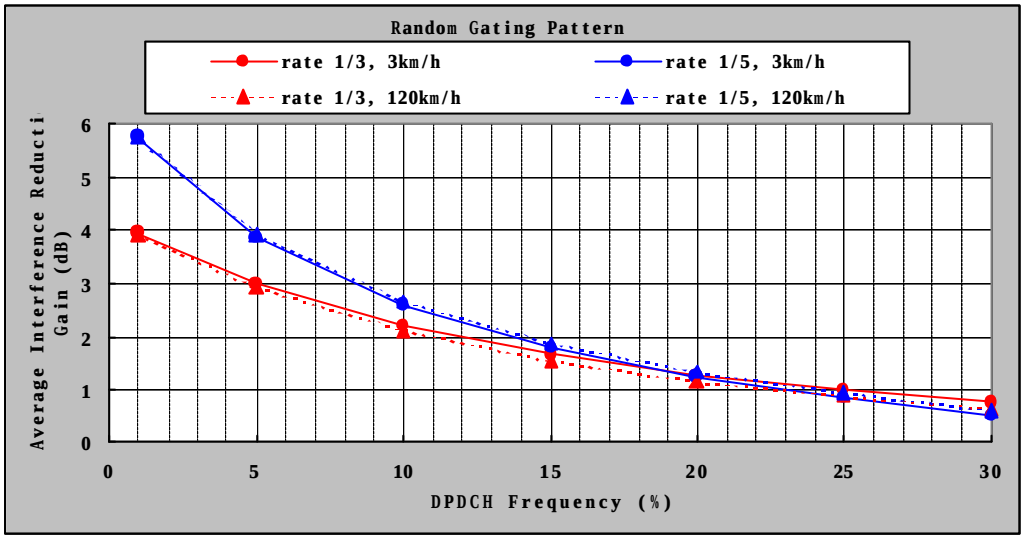

Figure 6. Average uplink interference reduction gain

8.1.1.3 Conclusion

From the simulation and analysis results, the uplink interference reduction gain is enough to use ~~gated DPCCH transmission~~gating. If the DPDCH frequency is 10%, the interference reduction gain is about 2.5dB, and the gain increases as the DPDCH frequency decreases. Consequently, the ~~gated DPCCH transmission~~gating is beneficial to the interference reduction, that is, the transmit power reduction.

8.1.2 UE Battery Life Enhancement [4~~2~~]

In this section, to show the advantage in UE battery life provided by gated DPCCH transmission, UE battery life enhancement calculation is described under the assumptions that the compressed mode is not initiated and that all Node Bs in the active set support gated DPCCH transmission.

8.1.2.1 Assumptions and models used in battery life calculations

8.1.2.1.1 Packet model

The same packet model was used as described in [5~~3~~]. The Figure 7 shows the structure of the packet session, where:

Tp = average duration of one packet call.

Tcr_dch = connection release time for DCH only case.

Tcr_dsch = connection release time for DSCH+DCH case.

One interesting point here is that Tcr_dsch can be quite large, larger than Tcr_dch, which means that it can be so long the connection does not have to be released between each packet call. This is because DCH associated with DSCH could use quite high spreading factor, e.g. SF=256. However, it does not make any difference to the battery life calculations. Meaning, that if the simplified assumption is that gap between two packet calls is equal or larger than Tcr_dch or Tcr_dsch, then following model, explained below can be used in the battery life calculations.

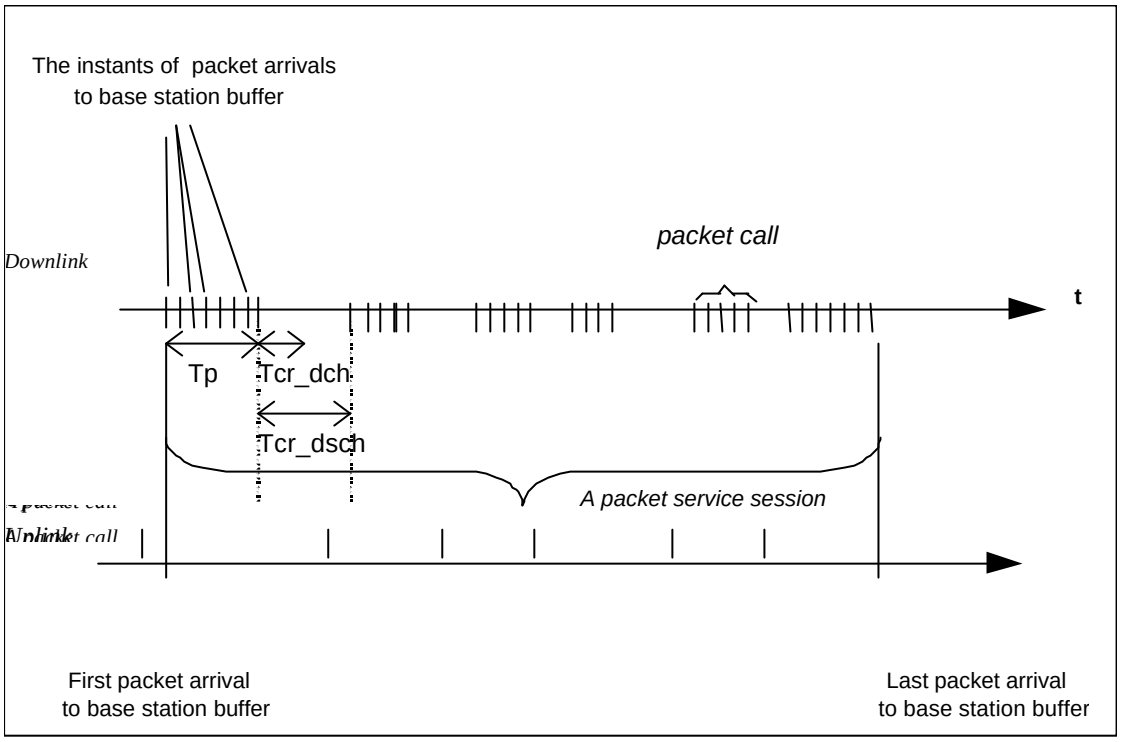

Figure 7. Packet model

Figure 8 shows the timing model, how the gating is assumed to be turned on in the battery calculations. Here Tgat_on is the time after the last packet when the gating is turned on. Note that Tgat_on should be larger than the time interval between individual packet bursts within Tp. Thus the percentage of time that the gating is on during the whole connection is

For DCH only case: $DPCCH\_gating\_\% = \frac{Tcr\_dch + Tgat\_on}{Tp + Tcr\_dch}$

For DCH+DSCH case: $DPCCH\_gating\_\% = \frac{Tcr\_dsch + Tgat\_on}{Tp + Tcr\_dsch}$

In [53], it was roughly calculated with these equations, that the percentage of time the DPCCH gating could be on, on average:

For DCH only case: DPCCH_gating_% = 0.30

For DCH+DSCH case: DPCCH_gating_% = 0.66

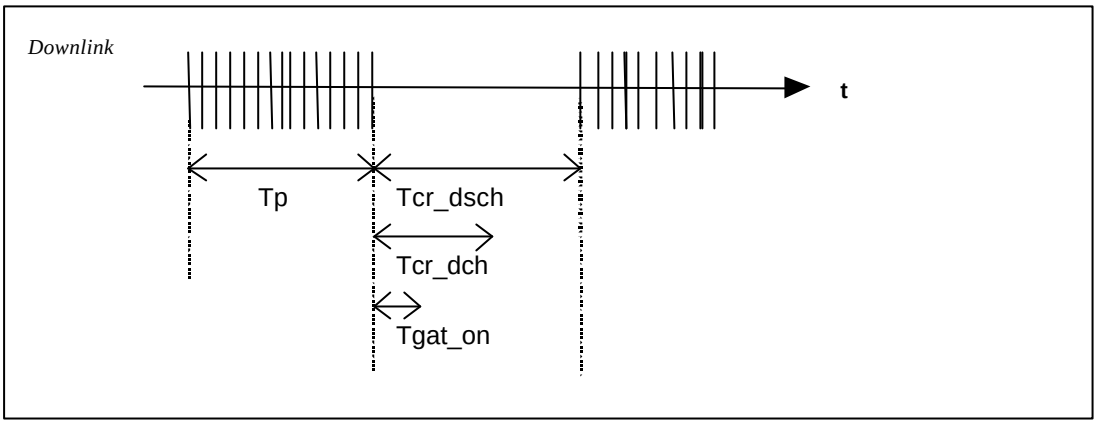

Figure 8. Timing for turning the gating on.

8.1.2.1.2 Assumptions in UE battery life calculations with tx only gating

Following assumptions were used in the simplified UE battery life calculations in [64].

1) First it was assumed what is the percentage of battery consumption of tx side and rx side, respectively, for certain tx power level, when gating is not used. Let's say that with tx power level , txpwr, this results in :

   - tx side consumes N1 mA @ txpwr
   - rx side consumes N2 mA

   No specific data rates were assumed here either in uplink or downlink, for simplification. This is because data rate change in downlink was assumed not to affect the battery consumption so much. The continuous decoding is needed anyway in downlink, since the packet transmission can be assumed to restart in any frame and handover measurements are running continuously. If continuous decoding in every frame could be avoided, then we could assume clearly a different figure for rx side battery consumption during gating state, but until then, the same value N2, is assumed for rx side throughout the whole connection.

2) Then it was calculated, what is the tx side battery consumption, if tx gating is used. Separate values were calculated for 1/3 gating and 1/5 gating, with the same corresponding tx power level tx pwr. This resulted in following value:

   - tx side consumes N1_gating mA, during gating @ txpwr

3) Finally it was calculated what is the overall battery life improvement:

$$Battery\_life\_improvement = \frac{N1 + N2}{(1 - DPCCH\_gating\_\%) \cdot N1 + DPCCH\_gating\_\% \cdot N1\_gating + N2}$$

8.1.2.1.3 Assumptions in UE battery life calculations with tx and rx gating

Following assumptions have been used in the simplified UE battery life calculations with tx and rx gating.

1) First it was assumed what is the percentage of battery consumption of tx side and rx side, respectively, for certain tx power level, when gating is not used. Let's say that with tx power level , txpwr, this results in :

   - tx side consumes N1 mA @ txpwr
   - rx side consumes N2 mA

   No specific data rates were assumed here either in uplink or downlink, for simplification.

2) Then it was calculated, what is the txside battery consumption, if tx gating is used. Separate values were calculated for 1/3 gating and 1/5 gating, with the same corresponding tx power level txpwr. This resulted in following value:

   - tx side consumes N1_gating mA, during gating @ txpwr

3) It was also calculated, what is the rx side battery consumption (average battery consumption over K frames), if rx gating is used. Here rx is on the whole frame in every Kth frame. And in the frames in between the rx is on only in every 3rd slot or every 5th slot, with 1/3 gating or 1/5 gating, respectively. This resulted in following value:

   - rx side consumes N2_gating mA, during gating

4) Finally it was calculated what is the overall battery life improvement:

$$Battery\_life\_improvement\ ?\ \frac{N1\ ?\ N2}{N1\_total\_new\ ?\ N2\_total\_new}$$

where:

N1_total_new = (1-DPCCH_gating_%)*N1 + DPCCH_gating_%*N1_gating

N2_total_new = (1-DPCCH_gating_%)*N2 + DPCCH_gating_%*N2_gating

8.1.2.2 UE battery life improvement calculations

8.1.2.2.1 UE battery life improvement calculations with tx only gating

The battery life improvement calculations from [64] are repeated here once more, for clarification.

Table 10 and 11 show UE battery lifetime improvements for DCH and DCH+DSCH case, for medium range tx pwr level and high tx power level, respectively. Thus the only difference in calculating DCH case and DCH+DSCH case, is the value used for DPCCH_gating_% value.

Table 10. UE battery life improvement due to gating, with medium range tx power level.

	DPCCH_gating_%	Gating rate	UE battery life improvement
DCH	30 %	1/3	8 %
		1/5	13 %
DCH+DSCH	66 %	1/3	21 %
		1/5	34 %

Table 11. UE battery life improvement due to gating, with maximum tx power level.

	DPCCH_gating_%	Gating rate	UE battery life improvement
DCH	30 %	1/3	10 %
		1/5	16 %
DCH+DSCH	66 %	1/3	26 %
		1/5	44 %

NOTE: Due to the fact that I/Q multiplexing is used in uplink the CRC attachment to zero length transport block will not introduce any deterioration to presented battery life improvement figures.

The results show that DPCCH gating means clear UE battery life improvement in DCH+DSCH case. For DCH only case it is maybe not as sensible to utilise it.

8.1.2.2.2 UE battery life improvement calculations with tx and rx gating

Here we show the UE battery life improvement calculations with tx and rx gating, where higher layer scheduling idea has been used, to allow battery savings also in rx side [75]. Values K=1,4 and 8 are used in the calculations, where K defines that rx side has to be on the whole frame in every Kth frame. Note, K=1 gives the same result, as was given in

our previous UE battery improvement calculations, where only tx side improvement could be achieved, since K=1 means that rx side has to be on in every frame.

Thus table 12 and 13 show UE battery lifetime improvements for DCH+DSCH case, with DPCCH_gating_%=0.66, for medium range tx pwr level and high tx power level, respectively. This time we did not calculate the case for DCH only case (DPCCH_gating_%=0.3), since the main point here is to evaluate, whether rx gating is giving clear enough improvement, or whether tx only gating (K=1 case) is sensible alone.

Table 12. UE battery life improvement due to tx and rx gating, with medium range tx power level.

Gating rate	K	UE battery life improvement
1/3	1	21 %
	4	32 %
	8	34 %
1/5	1	34 %
	4	56 %
	8	60 %

Table 13. UE battery life improvement due to tx and rx gating, with maximum tx power level.

Gating rate	K	UE battery life improvement
1/3	1	26 %
	4	35 %
	8	37 %
1/5	1	44 %
	4	61 %
	8	65 %

It can be seen that combined tx and rx gating clearly further improves the UE battery life compared to tx only gating.

NOTE: Due to the fact that I/Q multiplexing is used in uplink the CRC attachment to zero length transport block will not introduce any deterioration to presented battery life improvement figures. In addition, in downlink gating the achieved battery saving figures are calculated using the assumption that there is no switching within a slot.

8.1.2.3 Conclusion

With the help of DCH+DSCH concept, several packet calls in one packet session can be transmitted during the same connection without connection release between them, and without unnecessary usage of RACH between every packet call. With the help of DPCCH gating concept together with DCH+DSCH concept, we can offer the end user a very flexible and fast packet service in such way, that we do not sacrifice the UE battery life too much.

If DPCCH gating would not be specified, the relative long periods (=end user's reading time) between each packet call, will consume UE batteries unnecessarily, which does not make much sense. However, it should be understood, that if operator wants to use long connection release times, he is allowed to do that, since there are no limitations anyway in the specifications, how long the connection release time can be.

~~8.1.3 References~~

~~[1] R1-00-1069, "Revised uplink interference reduction gain of gated DPCCH transmission", Samsung~~

~~[2] R1-00-1029, "Clarification of UE battery life calculations", Nokia~~

~~[3]R1-00-0686, "Discussion paper on DPCCH gating benefits", Nokia~~

~~[4] R1-00-0856, "UE battery life improvement with DPCCH gating", Nokia~~

~~[5] R1-00-1079, "Proposal of using both tx and rx gating", Nokia~~

9 Backward Compatibility

A UE based on Release 99 can be used in Release 4 UTRAN with ~~gated DPCCH transmission~~gating capability without any impact because the gating capability is negotiated during call-setup. Similarly, a UE based on Release 4 with ~~gated DPCCH transmission~~gating capability can be used in Release 99 UTRAN without any impact by the same reason. Consequently, the backward compatibility is guaranteed with ~~gated DPCCH transmission~~gating in Release 4.

Annex A:
Change history

Change history							
Date	**TSG #**	**TSG Doc.**	**CR**	**Rev**	**Subject/Comment**	**Old**	**New**
2000.8	RAN1#15	R1-00-1166			Approval at TSG RAN WG1#15 meeting	-	0.0.1
2000.9	RAN#9	RP-00-0408			Presented at TSG RAN#9 plenary meeting. Comments were: 1. RRC blocking problem due to reduced power control rate 2. UE transmit power limitation in cell boundary	0.0.1	1.0.0
2000.10	RAN1#16	R1-00-1304			Include expected gains in Network side. Data with restricted TFS can be transmitted during gating. Enhance conceptual transition diagram.	1.0.0	1.1.0
2000.11	RAN1#17	R1-00-1444			Include RX gating features and calculation of UE battery life improvement obtained by TX and RX gating.	1.1.0	1.2.0
2000. 12	RAN#10	RP-000548			~~(will be approved and placed under change control at TSG-RAN #10)~~ Kept as version 2.0.0	1.2.0	2.0.0
2001. 1	RAN1#18	R1-01-0179			Include outer loop power control features based on CRC attached to zero length transport bloc k and some clarifications based on the comments made during RAN1#18.	2.0.0	2.1.0