TSG-RAN Working Group 1 meeting# 16 TSGR1#16(00) 1242

Pusan, Korea, Oct 10 - Oct 13 2000

Agenda Item: AdHoc#24, HSDPA

Source: Motorola

Control Channel Structure for High Speed DSCH (HS-DSCH)

Introduction

In this contribution, the uplink and downlink control channel structure for High Speed Downlink Shared Channel (HS-DSCH) is described.

0.0 Uplink DPCCH for HS-DSCH

The uplink DPCCH is modified from Release-99 specification so that it can be used to carry the control information to support HS-DSCH operation. The modified DPCCH is used to carry known pilots bits to support channel estimation for coherent detection, acknowledgement bits for hybrid ARQ operation, TFCI/Echo bits to transfer the hybrid ARQ state information for Fast Site Selection and Transport format for uplink, feedback information bits (FBI) and transmit power-control (TPC) bits. The FBI bits are used to support Fast Site Selection and closed loop mode transmit diversity. One of the functions of the FBI bits is to indicate the optimal Node-B from which the network should direct its data transmission on the HS-DSCH. Figure 1 shows the modified structure of DPCCH.

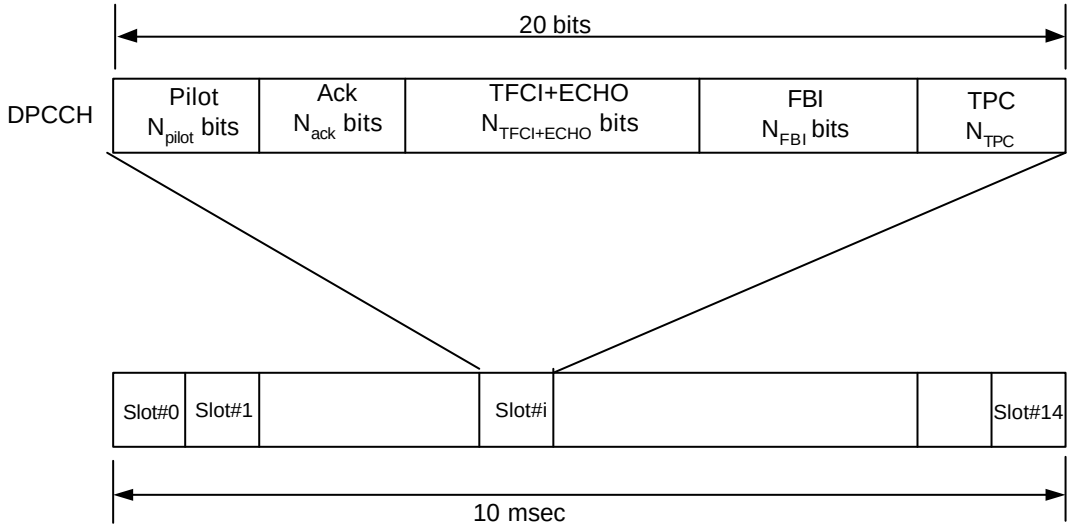

Figure 1. DPCCH Structure to support HS-DSCH

The tentative DPCCH fields are shown in Table 1. It may be noted that the TFCI+ECHO field are coded and interleaved over at least 4 slots if the frame length of the HS-DSCH is set to 3.33 msec or 5 slots. The ACK bits are set to '1' if the HS-DSCH is received correctly and set to '0' otherwise.

It may be noted that the spreading factor of the modified DPCCH have been reduced by a factor of 2 in comparison to original DPCCH to support the control features associated with the HS-DSCH (which results in increased data rates).

Table 1. DPCCH fileds in support of HS-DSCH

Slot Format	Sym Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{pilot}	N_{ack}	$N_{TFC+ECHO}$	N_{FBI}	N_{TPC}
0	30	128	300	20	4	3	8	3	2
1	30	128	300	20	4	4	6	4	2

1.0 Downlink Control Channel Structure for HS-DSCH

In Release-99 specification the DSCH is always associated with a dedicated downlink channel. For HS-DSCH a shared dedicated channel approach is proposed. The key concept behind the shared dedicated channel approach is that not all of the control fields are needed all of the time. Hence, a statistical approach can be taken which allows those pieces of information that are always needed to be placed in dedicated user channels while the other information that is intermittent is placed in shared channel resources. Statistically splitting the control information into multiple channels with larger Walsh codes provides enough Walsh code resources and enough bits at lower power levels. The efficient method to exploit the statistical nature of the control information is to use a dedicated pointer channel (DPTRCH) for each user which contains control information needed almost every slot and a pointer to a pool of shared control channels (SHCCHs) for control information required less frequently. The proposed structure of DPTRCH and SHCCH is shown in Figure 2.

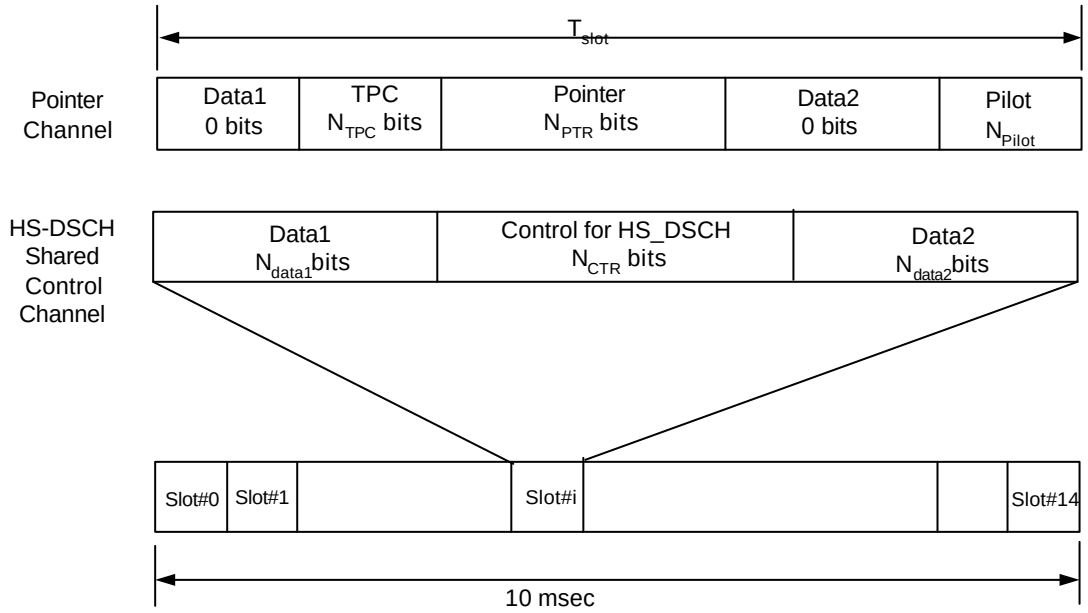

Figure 2. Frame Structure of DPTRCH and SHCCH

The tentative DPTRCH and SHCCH fields are shown in Table 2. The Walsh code allocation for the DPTRCH and SHCCH are TBD.

Table 2. DPTRCH and SHCCH Fields

Slot Format	Sym Rate (ksps)	SF	Bits/ Slot	N_{pilot}	N_{data1}	N_{PTR}	N_{data2}	N_{TPC}	N_{CNTR}
DPTRCH	15	512	10	4	n.a	4	n.a	2	n.a
SHCCH	30	256	20	n.a	6	n.a	6	n.a	8

References

[1] 3G TS 25.211 v3.2.0, "Physical Channels and Mapping of Transport Channels onto Physical Channels (FDD)"