## 3GPP TSG RAN WG1 Meeting #16 Pusan. Korea, 10<sup>th</sup> – 13<sup>th</sup> October, 2000

help.doc

# Document R1-00-1199 e.g. for 3GPP use the format TP-99xxx or for SMG, use the format P-99-xxx

CHANGE REQUEST  Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.	
	25.211 CR 081 Current Version: 3.4.0
GSM (AA.BB) or	3G (AA.BBB) specification number? ? CR number as allocated by MCC support team
For submissic	
Proposed change affects: (at least one should be marked with an X)  (U)SIM ME X UTRAN / Radio X Core Network	
Source:	Philips <u>Date:</u> 2000-10-03
Subject:	Clarification of uplink timing reference
Work item:	
Category:  (only one category shall be marked with an X)	F Correction A Corresponds to a correction in an earlier release B Addition of feature C Functional modification of feature D Editorial modification  X Release: Release 96 Release 97 Release 98 Release 99 Release 00
Reason for change:	UL transmit timing could be continually slewing in soft handover.
Clauses affect	ed: 7.6.3
Other specs affected:	Other 3G core specifications Other GSM core specifications MS test specifications BSS test specifications O&M specifications O&M specifications  ? List of CRs:
Other comments:	
$W_{\bullet}$	

<----- double-click here for help and instructions on how to create a CR.

### 7.6 DPCCH/DPDCH timing relations

#### 7.6.1 Uplink

In uplink the DPCCH and all the DPDCHs transmitted from one UE have the same frame timing.

#### 7.6.2 Downlink

In downlink, the DPCCH and all the DPDCHs carrying CCTrCHs of dedicated type to one UE have the same frame timing.

#### 7.6.3 Uplink/downlink timing at UE

When the UE has no more than one Node B in the active setAt the UE, the uplink DPCCH/DPDCH frame transmission at the UE shall takes place approximately  $T_0$  chips after the reception of the first detected path (in time) of the corresponding downlink DPCCH/DPDCH frame.  $T_0$  is a constant defined to be 1024 chips. The first detected path (in time) is defined implicitly by the relevant tests in [14]. More information about the uplink/downlink timing relation and meaning of  $T_0$  can be found in [5].

When the UE has more than one Node B in the active set, the uplink DPCCH/DPDCH frame transmission at the UE shall take place approximately  $T_0 + \frac{2}{10}$  chips after the reception of the first detected path (in time) of the corresponding downlink DPCCH/DPDCH frame from the first cell, where  $\frac{2}{10}$  shall be within the following range:

where 2<sub>tiff</sub> is equal to the number of chips between the arrival time of the first detected path (in time) of the first-received DL DPCH and the arrival time of the first detected path (in time) of the last-received DL DPCH.

The rate of timing adjustment which shall be used by the UE is detailed in [14].