TSG-RAN Working Group 1, AdHoc 21   ***TSGR1(00)0818***

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Title: general description of the physical layer for low chip rate TDD
Document for: Discussion and Approval

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Introduction

This paper give a general description of the physical layer in the low chip rate TDD option. The main differences between the two options are highlighted.

Conclusion

It's proposed to include the following text in TR25.928

--------------------------------- changes to TR25.928 begin ------------------------------------

[Description:]

Most of the physical character of the low chip rate TDD option is same as the high chip rate TDD option. But it still exists some little difference between these two mode basically due to the different operation frequency bandwidth. Here it give some general description of the physical layer in low chip rate TDD option.

[Rationale:]

6   Physical layer - General description

6.1   General description of Layer 1

Common with the high chip rate TDD mode
6.1.2   Service provided to higher layers

The physical layer offers data transport services to higher layers. The access to these services is through the use of transport channels via the MAC sub-layer. In addition to the functions listed in TS25.201, the physical layer for the low chip rate TDD option is expected to perform the following functions in order to provide the data transport service.:

-   beamforming

-   synchronisation shift control

6.2   General description of Layer 1

6.2.1   Multiple Access
In contrast to the high chip rate TDD option, the access scheme is Direct-Sequence Code Division Multiple Access (DS-CDMA) with information spread over approximately

1.6 MHz bandwidth only, thus also often denoted as low chip rate TDD option due that nature.

The frame structure of the low chip rate options differs from the high chip rate option in the following way: A 10 ms radio frame is divided into 2 sub-frames of 5ms. The frame structure (e.g. switching points) for each sub-frame in the 10ms frame length is the same. The sub-frame is divided into 7 traffic slots (864 chip/slot at the chip rate 1.28 Mcps) as described in subclause 7.2.1 'Frame Structure' and 3 timeslots with special functionality.

The information rate of the channel is different from the high chip rate option and varies with the symbol rate being derived from the 1.28 Mcps chip rate, the spreading factor and the modulation mode.

6.2.2 Channel coding and interleaving

Common with the high chip rate TDD mode

6.2.3   Modulation and spreading
The ordinary modulation scheme is QPSK, as for the the high chip rate option. In addition to that 8PSK is also possible.

For separating different cells the following solutions are additionally supported in the low chip rate option:
-       SYNC sequences, SYNC1 sequences.

For separating different UEs the following code families are additionally defined:
-       SYNC1 sequences

6.2.4   Physical layer procedures
There are several physical layer procedures involved with low chip rate TDD operation that are different and in addition to the high chip rate option. Such procedures covered by physical layer description are:
  1) The power control, for low chip rate TDD mode close loop control in both uplink and downlink.

  2) Cell search operation.

  3) Uplink synchronisation for low chip rate TDD mode.

  4) Random access / hand over

  5) Beamforming (optional)

6.2.5   Physical layer measurements
Common with the high chip rate TDD mode

[Explanation difference:]

Most of the physical characters of the low chip rate TDD option are same as the high chip rate TDD option. But due to the different operation frequency band width and some other different implementation consideration such as power control method, uplink synchronization, there still exist some difference and all these difference will be discussed in the main part of TR25.928.

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