TSG-RAN Working Group 1 meeting AH21 **TSGR1(00)0955**

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Agenda Item: AH21
Source: CATT/CWTS
To: TSG RAN WG1
Title: Monitoring GSM from low chip rate TDD
Document for: Discussion and Approval

Introduction

This paper describes some physical layer measurements of the low chip rate TDD which are different from the high chip rate TDD.

Conclusion

It's proposed to discuss and include the following text proposal into the clause 11 'physical layer measurements' of TR25.928.

---------- changes to TR25.928 begin ----------

[Description:]
This paper gives some general description about how to monitor GSM from the low chip rate TDD.

[Rationale:]

A.1 Low data rate traffic using 1 uplink and 1 downlink slot

NOTE: The section evaluates the time to acquire the FCCH if all idle slots are devoted to the tracking of a FCCH burst, meaning that no power measurements is done concurrently. The derived figures are better than those for GSM. The section does not derive though any conclusion. A conclusion may be that the use of the idle slots is a valid option. An alternative conclusion may be that this is the only mode to be used, removing hence the use of the slotted frames for low data traffic or the need for a dual receiver, if we were to considering the monitoring of GSM cells only, rather than GSM, TDD and FDD.

If a single synthesiser UE uses only one uplink and one downlink slot, e.g. for speech communication, the UE is not in transmit or receive state during 5 slots in each frame. According to the timeslot numbers allocated to the traffic, this period can be split into two continuous idle intervals A and B as shown in the figure below.

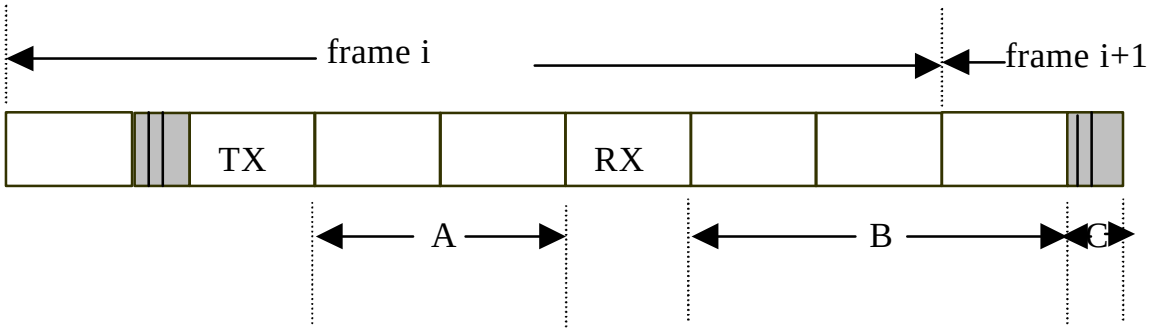

Figure A.1: Possible idle periods in a subframe with two occupied timeslots

A is defined as the number of idle slots between the Tx and Rx slots and B the number of idle

slots between the Rx and Tx slots. It is clear that A+B=5 time slots and C is equal to the DwPTS+GP+UpPTS.

In the scope of low cost terminals, a [0.5] ms period is supposed to be required to perform a frequency jump from low chip rate TDD to GSM and vice versa. This lets possibly two free periods of A*Ts-1 ms and B*Ts+C-1 ms during which the mobile station can monitor GSM, Ts being the slot period.
Following table evaluates the average synchronisation time and maximum synchronisation time, where the announced synchronisation time corresponds to the time needed to find the FCCH. The FCCH is supposed to be perfectly detected which means that it is entirely present in the monitoring window. The FCCH being found the SCH location is unambiguously known from that point. All the 5 idle slots and the DwPTS+GP+UpPTS are assumed to be devoted to FCCH tracking and the UL traffic is supposed to occupy the time slot 1.

Table A.1: example- of average and maximum synchronisation time with two busy timeslots per frame and with 0.5 ms switching time

Downlink time slot number	Number of free TS in A	Number of free TS in B	Average synchronisation time (ms)	Maximum synchronisation time (ms)
0	5	0	83	231
2	0	5	75	186
3	1	4	98	232
4	2	3	185	558
5	3	2	288	656
6	4	1	110	371

(*) All simulations have been performed with a random initial delay between GSM frames and low chip rate TDD subframes.
Each configuration of TS allocation described above allows a monitoring period sufficient to acquire synchronisation.

A.1.1 Higher data rate traffic using more than 1 uplink and/or 1 downlink TDD timeslot

The minimum idle time to detect a complete FCCH burst for all possible alignments between the GSM and the TDD frame structure (called ‘guaranteed FCCH detection’), assuming that monitoring happens every TDD frame, can be calculated as follows (t_{FCCH} = one GSM slot):

- (e.g for t_{synth} =0ms: 2 low chip rate TDD **consecutive** idle timeslots needed, for t_{synth} =0.3ms: 3

$$t_{\min\ ,\ guarante\ \ ed} = 2 \times t_{synth} + t_{FCCH} + \frac{5\,\text{ms}}{13} = 2 \times t_{synth} + \frac{25\ \text{ms}}{26}$$

  slots (or 2 slots and the DwPTS+GP+UpPTS), for t_{synth} =0.5ms: 3 slots, for t_{synth} =0.8ms: 4 slots). Under this conditions the FCCH detection time can never exceed the time of 660ms.

- (For a more general consideration t_{synth} may be considered as a sum of all delays before starting monitoring is possible).

- For detecting SCH instead of FCCH (for a parallel search) the same equation applies.

- In the equation before the dual synthesiser UE is included if the synthesiser switching time is 0ms.

Considering about the frame structure of the low chip rate TDD, there are total 7 timeslot in each frame that can be used as data traffic. If more than 1 uplink and/or 1 downlink TDD timeslot are used for data traffic, that means it will occupy at least 3 time slot, equal to 0.675*3=2.205ms. And more time slots for traffic data means more switching point are needed to switch between the GSM and the low chip

rate TDD. As it was mentioned above, each switching will take 0.5ms. As a result, the idle time left for monitoring the GSM will be very little. So monitoring GSM from low chip rate TDD under this situation will be considered in the future. It will need more carefully calculation and simulation.
For a synthesiser switching time of one or one half TDD timeslot the number of needed consecutive idle TDD timeslots is summarized in the table below:

Table A.2: Link between the synthesiser performance and the number of free consecutive TSs for guaranteed FCCH detection, needed for GSM monitoring

One-way switching time for the synthesiser	Number of free consecutive TDD timeslots needed in the frame for a guaranteed FCCH detection
1 TS (=864 chips)	4
0.5 TS (=432 chips)	3
0 (dual synthesiser)	2

[Explanation difference:]

Due to the different operating bandwidth and the different frame structure, some measurement method about how to monitor GSM are different between the high and low chip rate TDD.

---------- changes to TR25.928 end ----------