TSG-RAN Working Group 1 AH21 **TSGR1(00)0934**

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Introduction

This paper introduces some simulation results for the performance analysis of power control for low chip rate TDD service multiplexing 12.2kbps and 2.4kbps bit rate.

The benefit of power control with 5 ms update rate

Fundamentals

The purpose of power control is to minimise the receiver power fluctuations to within a value sufficient enough to obtain a required performance from a given link. The fluctuations are mainly due to slow fading (i.e. shadowing) and fast fading (Rayleigh fading). The optimum situation is that all users are received with the same power, and thus, the interferences among each user are the minimum. For near-far resistant receivers this is a minor issue. Another benefit from power control is that each user transmits only with the power that it really needs, as a result, the intercell interference in the network is reduced and the UE is able to save battery power. Finally, power control improves the fading statistics for the regarded UE, and thus, leads to a considerable performance improvement for environments with a low time variance. This would be the major effect for near-far resistant receivers in the link level. Therefore, an efficient power control scheme guarantees a high system capacity and is, thus, of major importance for low chip rate TDD option.

There are several ways to simulate power control schemes, say, ***ideal*** power control and ***normal*** power control, etc.

Ideal power control compensates the exact difference between Rx power and reference value in one time which always give the best control result. But it is not practical in implementation and thus can only be used for comparison with other schemes as the optimal bound.

The difference of normal power control from ideal simulations is that, it increases or decreases the transmit power at one certain step (i.e. 1~3dB) each control loop, and consequently it is much practical then ideal power control. For relatively time invariant environment, normal power control performs rather good. But fast time varying channel, it can not control the transmit power to follow the fast fluctuation of the received power which will result in frequent overshoot.

Simulation assumptions

Table 1 Outdoor to Indoor and Pedestrian Test Environment Tapped-Delay-Line Parameters

Tap	Channel A		Doppler Spectrum
	Rel. Delay (nsec)	Avg. Power (dB)	
1	0	0	CLASSIC
2	110	-9.7	CLASSIC
3	190	-19.2	CLASSIC
4	410	-22.8	CLASSIC
5	-	-	CLASSIC
6	-	-	CLASSIC

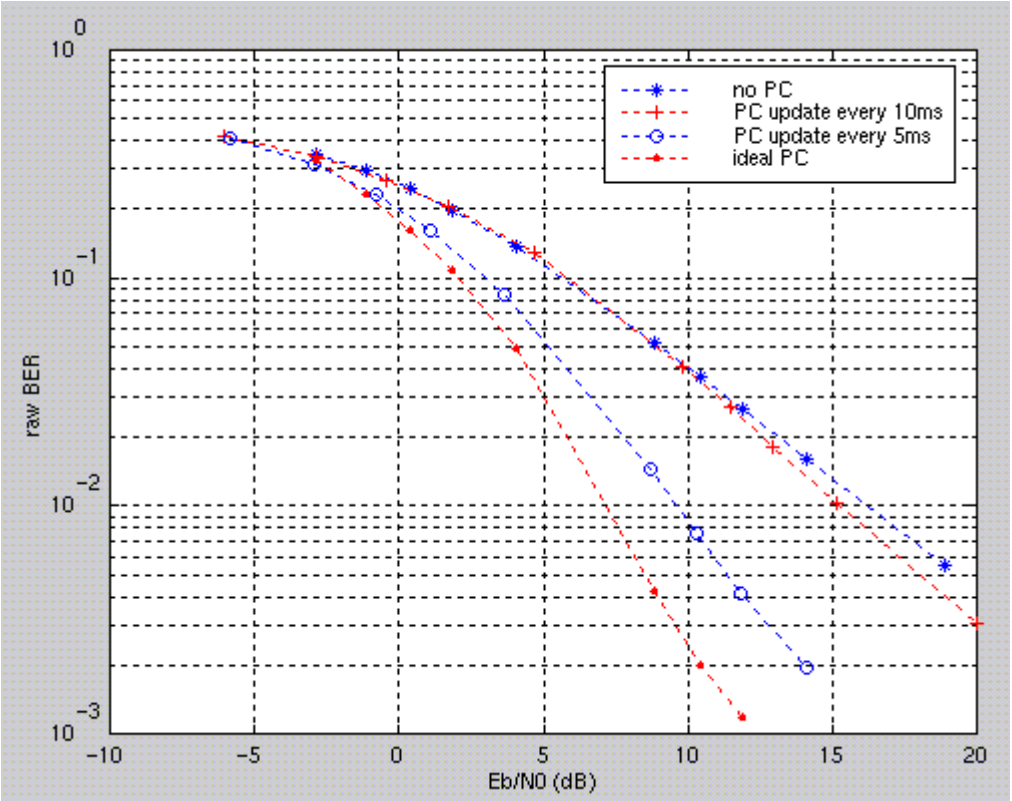
Channel used: OTI A.
Speed: 3 km/h.
Smart Antennas: No, only 1 RX antenna is used
Power control step: 3 dB closed loop

The service in the simulation multiplexes 12.2kbps data and 2.4kbps data. Totally up to 16 orthogonal codes is used for low chip rate TDD option. Each user with this service occupies 2 codes, so 8 users are tested in the simulation chain.

For the simulations the following service has been used:
Multiplexing of 12.2kbps data and 2.4kbps data -service mapping see section B.2 – B.3 of TR25.928.

Simulations result

Four schemes were used in the simulations, that is, ideal PC, PC update every 5ms, PC update every 10ms and no PC. The aim of using 5ms and 10ms update for PC is to find out an optimal update duration. Table 2~4 give the comparison results of raw BER, user BER and block error rate, respectively for all the four PC schemes. Table 2~4 give the corresponding Eb/N0 value of these schemes at certain bit error ratios. From the figures and tables, we can easily find out the considerable performance gains for power control than without PC, and the performance gains for 5ms update than 10ms update.

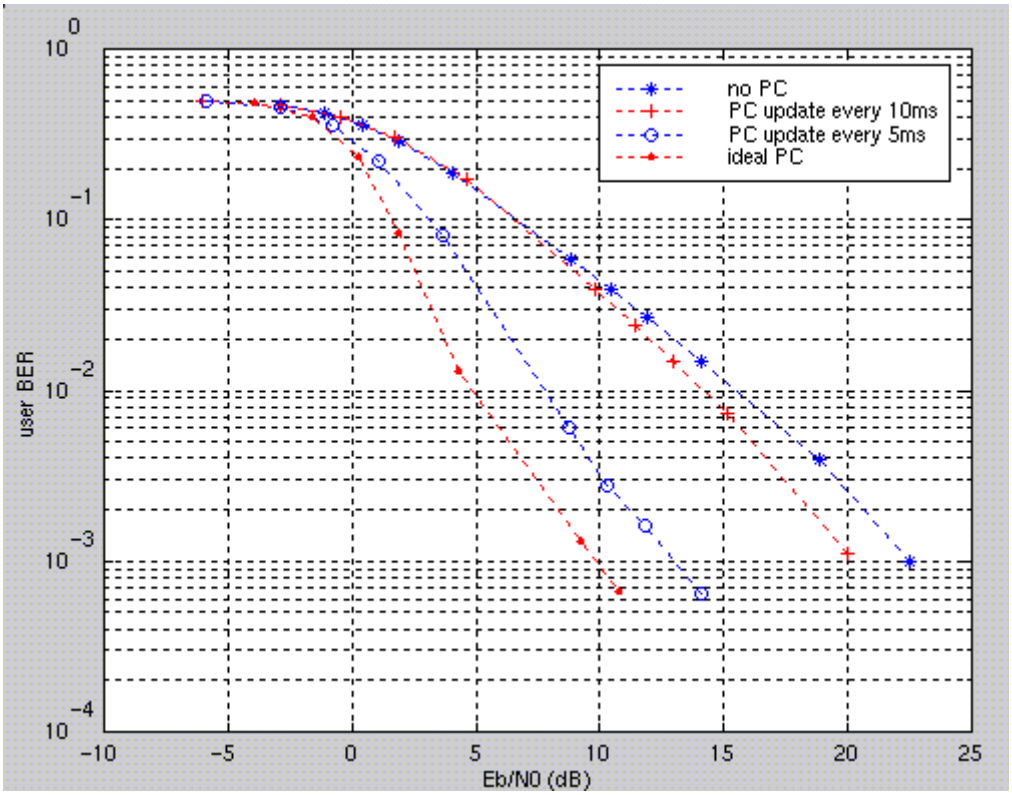


12.2kbps data multiplexing 2.4kbps data service,
OTI A/uplink, 8 users with 2 codes each.

Figure 1 Performance comparison of raw BER vs. Eb/N0

Table 2 Raw BER

	Performance improvement [dB]			
Raw BER	No PC	PC every 10ms	PC every 5ms	Ideal PC
0.1	0	0	2.7	3.5
0.05	0	0.3	3.9	4.9
0.02	0	0.5	5.5	7.0

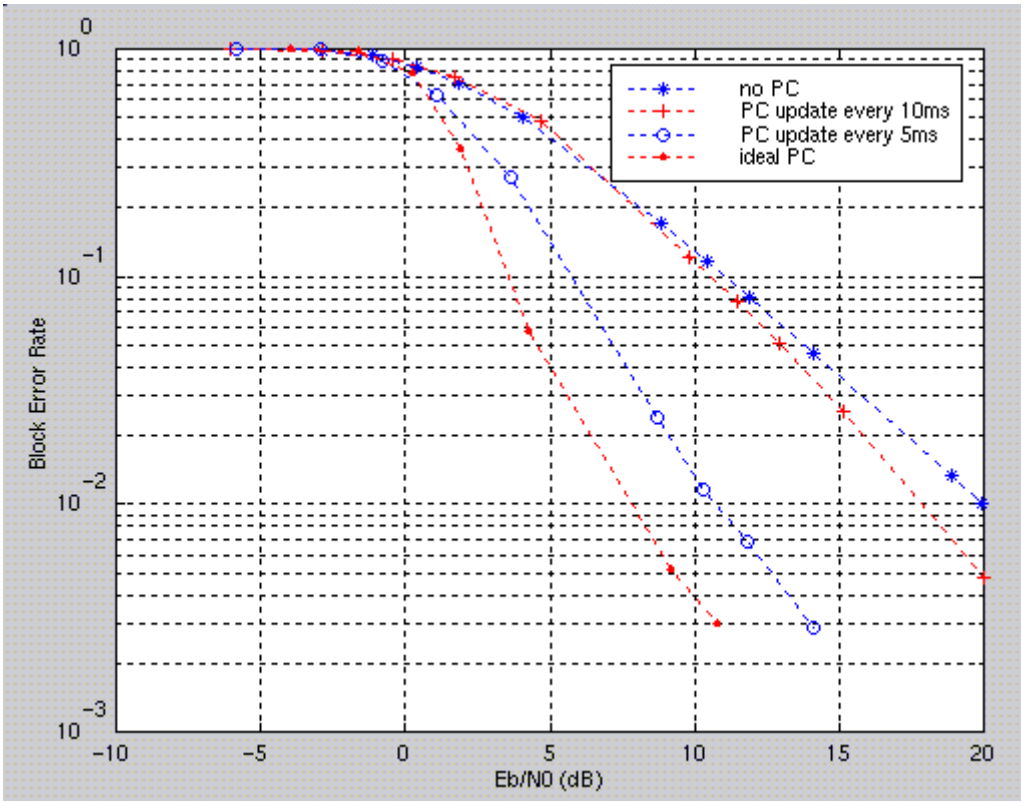


12.2kbps data multiplexing 2.4kbps data service,
OTI A/uplink, 8 users with 2 codes each.

Figure 2 Performance comparison of user BER vs. Eb/N0

Table 3 User BER

	Performance improvement [dB]			
User BER	No PC	PC every 10ms	PC every 5ms	Ideal PC
0.01	0	1.3	7.6	10.2
0.001	0	2.3	9.8	12.5



12.2kbps data multiplexing 2.4kbps data service,
OTI A/uplink, 8 users with 2 codes each.

Figure 3 Performance comparison of block error rate vs. Eb/N0

Table 4 Block Error Rate

	Performance improvement [dB]			
BLER	No PC	PC every 10ms	PC every 5ms	Ideal PC
0.2	0	0.2	3.9	5.2
0.1	0	0.6	4.7	7.1
0.01	0	2.5	8.1	12.2

Power control on a 10ms basis provides a visible improvement compared with no PC. As power control with 5 ms able to react more promptly to the fluctuation of received power due to Rayleigh fading it copes with more time invariant environment. So it can get considerable improvement compared with that of no power control. For 12.2kbit/s and 2.4kbit/s service with user BER at the level of 10^{-3}, it introduces about 10 dB improvement in Eb/N0 compared with no PC.

Conclusion

The benefit of power control shown in the link level simulation of this paper is considerable compared with no power control, and power control update every 5ms show considerable improvement compared to power control updates every 10ms. Therefore, the power control with 5 ms update rate should be used in the low chip rate low chip rate TDD option