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Introduction

This paper introduces some simulation results for low chip rate TDD for performance analysis of the uplink synchronization.

The benefit of uplink synchronization

Fundamentals

For low chip rate TDD there are two purposes of uplink synchronization control:

1. To keep the channel impulse response inside the channel estimation windows of the Steiner estimator. This concept is already well known in high chip rate TDD and is covered by the timing advance control.
2. To synchronize the UL reception of the UEs allocated to an UL time slot. Unlike the timing advance control this is done on sub-chip level. Thus, the functionality of the timing advance control is already covered by means of UL synchronization control. The performance improvement mechanism of UL synchronization control is sketched in the following figure.

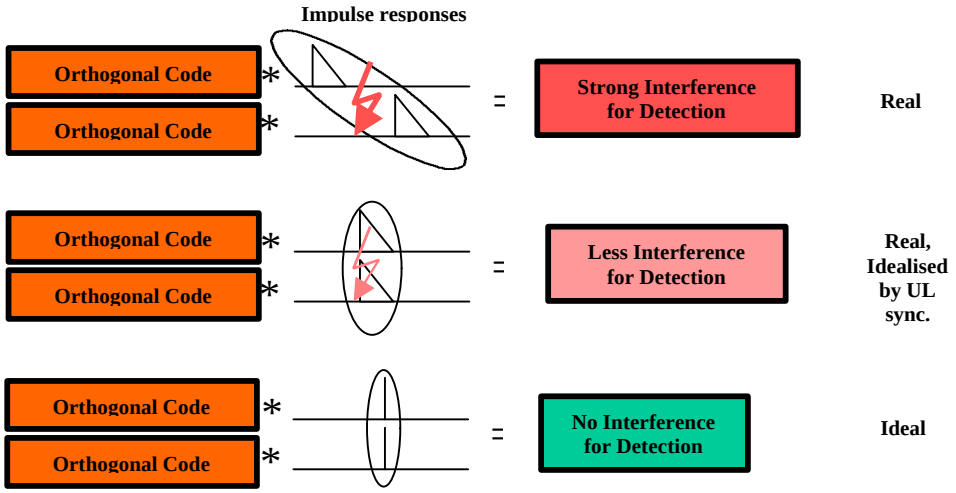

Figure 1 The performance improvement mechanism of UL synchronization control

For low chip rate TDD, a set of orthogonal codes (up to 16 codes) is used. An example of two UEs is shown in the above figure.

In case of **real** reception conditions without uplink synchronization, there is multiple path propagation and a too imprecise timing advance(uplink synchronisation) is unable to optimally synchronize the reception of the two UEs‘ signals. Thus, a strong interference is generated and needs to be cared for in the reception process.

UL synchronization applied in real reception conditions will lead to an optimal alignment of the channel impulse response as shown in the second part of the figure. This leads to a strong performance improvement while the multiple path propagation remains. Even if JD is applied

there can be a considerable performance improvement for the detection process due to missing noise amplification.
In the case of **ideal** reception there is no multiple path propagation visible in the receiver and the signals are received at exactly the same time. Thus, the UEs' signals will not interfere each other in the detection process.

Like for power control, uplink synchronization control can be implemented as slow uplink synchronization control, which is aligning the average channel impulse responses and fast uplink synchronization control which is aligning the instantaneous channel impulse responses.

Simulation assumptions

The following channels are used for the simulations in this section.

Table : Outdoor to Indoor and Pedestrian Test Environment Tapped-Delay-Line Parameters

Tap	Channel A		Channel B		Doppler Spectrum
	Rel. Delay (nsec)	Avg. Power (dB)	Rel. Delay (nsec)	Avg. Power (dB)	
1	0	0	0	0	CLASSIC
2	110	-9.7	200	-0.9	CLASSIC
3	190	-19.2	800	-4.9	CLASSIC
4	410	-22.8	1200	-8.0	CLASSIC
5	-	-	2300	-7.8	CLASSIC
6	-	-	3700	-23.9	CLASSIC

Speed: 3 km/h
Smart Antennas: No, (only 1 RX antenna is used)

For the modeling of uplink synchronization control it was assumed that the channel impulse response is shifted randomly with uniform distribution of +/- 1/2 steps of the uplink synchronization controller around the optimum position. These simulations are carried out under the assumption of perfect channel estimation and ideal power control to isolate the effect of UL synchronization.
The simulations are only carried out for the raw BER. The ZF-BLE was assumed to be the detector.

To access the performance improvement from timing advance control to uplink synchronization control, 1 chip uplink synchronization control was simulated for the performance of timing advance control. This is reasonable because for high chip rate TDD 4 chips timing advance increment are used. Considering that the channel impulse responses for low chip rate TDD are about 4 times shorter (measured in the number of chips) and that the chip rate for low chip rate TDD is 1/3 of that for high chip rate TDD, it is reasonable to assume 1 chip timing advance increment for low chip rate TDD. For uplink synchronization a precision of 1/8 chip is assumed for low chip rate TDD.
Depending on the speed and the service applied the raw BER typically needs to be around 10 % down to 2 % to maintain the required quality of service.

Simulation results

The following tables summarize the performance improvement from no ULSC to ULSC (OTI A):

2 UE (8 codes each)	Performance improvement [dB]			
Raw BER	1 chip prec. ULSC	1/8 chip prec. ULSC	ideal ULSC	AWGN
0.1	0	2.75	2.75	3.0
0.05	0	4.3	4.4	4.75
0.02	0	7.0	7.1	7.5
16 UE (1 code each)	Performance improvement [dB]			
Raw BER	1 chip prec. ULSC	1/8 chip prec. ULSC	ideal ULSC	AWGN
0.1	0	3.2	3.2	3.7
0.05	0	4.2	4.25	4.6
0.02	0	5	5.1	5.6

Discussion
For a single UE with full load in the time slot, the codes for that UE are already synchronised.
In case more than one UE is to be detected the asynchronous reception becomes very important – especially for the high load case. The performance improvement with uplink synchronization is about equal to the cases that 2, 4, 8 and 16 users (each full load) is simulated. In comparison to the performance of 1 chip uplink synchronization precision , the performance increases significantly (3.2@10%rawBER to 7 dB@2%rawBER) for 1/8 chip uplink synchronization precision. With high precision uplink synchronization control, nearly the ideal performance of the fading-less AWGN channel without multiple path propagation is reached.
Consequently uplink synchronization is easing to run low chip rate TDD under full load.

In other environments the performance difference between different precision of UL synchronization control can be even bigger.
This is shown with the following simulations taken for the outdoor to indoor B channel.
For the outdoor to indoor B channel the uplink synchronization control was simulated with 1/8 chip step.
The simulations are done with different numbers of active UE. Each UE uses 1 code.

The following table summarizes the performance improvement form slow ULSC to fast ULSC (OTI B):

	Performance improvement [dB]							
Raw BER	AWGN	1 UE	8 UE	10 UE	12 UE	14 UE	15 UE	16 UE
0.1	0	0	0.2	0.75	1.3	2.1	3.1	5.6
0.05	0	0	0.4	0.8	1.15	2.2	3.5	6.3
0.02	0	0	0.4	0.9	1.3	2.4	4.9	7.4

Discussion
For mobile radio channels with severe multiple paths the slow uplink synchronization control does not have a big performance difference with respect to the controller precision. When comparing the performance of slow uplink synchronization with that of fast uplink synchronization at full load, there is a performance difference of 5.6 dB at 10 % raw BER and of 7.4 dB at 2 % raw BER. The difference becomes smaller with less load.

Conclusion

The benefit of uplink synchronization control shown in the link level simulation of this section will take effect also on the system capacity of the low chip rate option. For this reason uplink synchronization should be included in the low chip rate option.