TSG-RAN Working Group 1 meeting #14
Oulu, Finland
July 4th – 7th, 2000

TSGR1#14(00)0923

Agenda item:

Source: Samsung

Title: DPCH timing offset when SF=512

Document for: Discussion and approval

Background

Now, the timing offset of DPCH is the multiples of 256 chips. When, however, the Spreading Factor is 512, the orthogonality of the may be broken due to the time offset of DPCH. We introduce an example of the similar situation when SF = 8 and the timing offset is the multiple of 4.

Let us consider two channelisation codes of SF =8. That is, the one is Code 1 = (11111111) and the other is Code 2=(1111-1-1-1-1). And the timing offset of DPCH of UE2 is delayed 4 chips compared to UE1 as in Fig.1. Now, let us assume that the first symbol of the UE1 is 1 and the second symbol is –1. As in Fig.2, the interference can not be rejected because transmitted symbols of the UE1 is the same as the channelisation code of the UE2.

```
               |                | ← One symbol period of UE 1
+1+1+1+1+1+1+1+1+1+1+1+1+1+1+1+1 ……  ← UE 1 channelisation code
        +1+1+1+1–1-1-1-1+1+1+1+1–1-1-1-1 …… ← UE 2 channelisation code
       |                | ← One symbol period of UE 2
```

Figure. 1 The diagram of the timing offset

```
               |                | ← One symbol period of UE 1
+1+1+1+1+1+1+1+1–1-1-1-1-1-1-1-1 ……  ← UE 1
        +1+1+1+1–1-1-1-1 +1+1+1+1–1-1-1-1 …… ← UE 2
       |                | ← One symbol period of UE 2
```

Figure. 2 The diagram of the transmitted symbols after channelisation

Proposed Solution

1. Increase the timing offset from 256 to 512 when only SF = 512.
2. When the UTRAN allocates the SF=512 channel, the UTRAN shall not allocate the same parent node (SF=256) to UE's.

Proposed One

We propose the number one of the proposed solutions. It doesn't waste the downlink channelisation codes.

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3GPP TSG RAN WG1 Meeting #14
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Document R1-00-923
e.g. for 3GPP use the format TP-99xxx
or for SMG, use the format P-99-xxx

CHANGE REQUEST

Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.

25.211	CR	067	Current Version:	3.3.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to:	RAN#9	for approval	X	strategic		*(for SMG use only)*
list expected approval meeting # here ↑		for information		non-strategic		

Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc*

Proposed change affects: *(at least one should be marked with an X)* (U)SIM [ ] ME [X] UTRAN / Radio [X] Core Network [ ]

Source: Samsung **Date:** 07/07/2000

Subject: Timing offset of DPCH when SF=512

Work item:

Category: *(only one category shall be marked with an X)*

F	Correction	X	**Release:**	Phase 2	
A	Corresponds to a correction in an earlier release			Release 96	
B	Addition of feature			Release 97	
C	Functional modification of feature			Release 98	
D	Editorial modification			Release 99	X
				Release 00	

Reason for change: When SF=512, to keep the orthogonality of the channelisation code, the timing offset of the DPCH is to be the multiples of the 512 chips.

Clauses affected: 7.1

Other specs affected:

Other 3G core specifications		→ List of CRs:
Other GSM core specifications		→ List of CRs:
MS test specifications		→ List of CRs:
BSS test specifications		→ List of CRs:
O&M specifications		→ List of CRs:

Other comments:

help.doc

<--------- double-click here for help and instructions on how to create a CR.

7 Timing relationship between physical channels

7.1 General

The P-CCPCH, on which the cell SFN is transmitted, is used as timing reference for all the physical channels, directly for downlink and indirectly for uplink.

Figure 28 below describes the frame timing of the downlink physical channels. For the AICH the access slot timing is included. Transmission timing for uplink physical channels is given by the received timing of downlink physical channels, as described in the following subclauses.

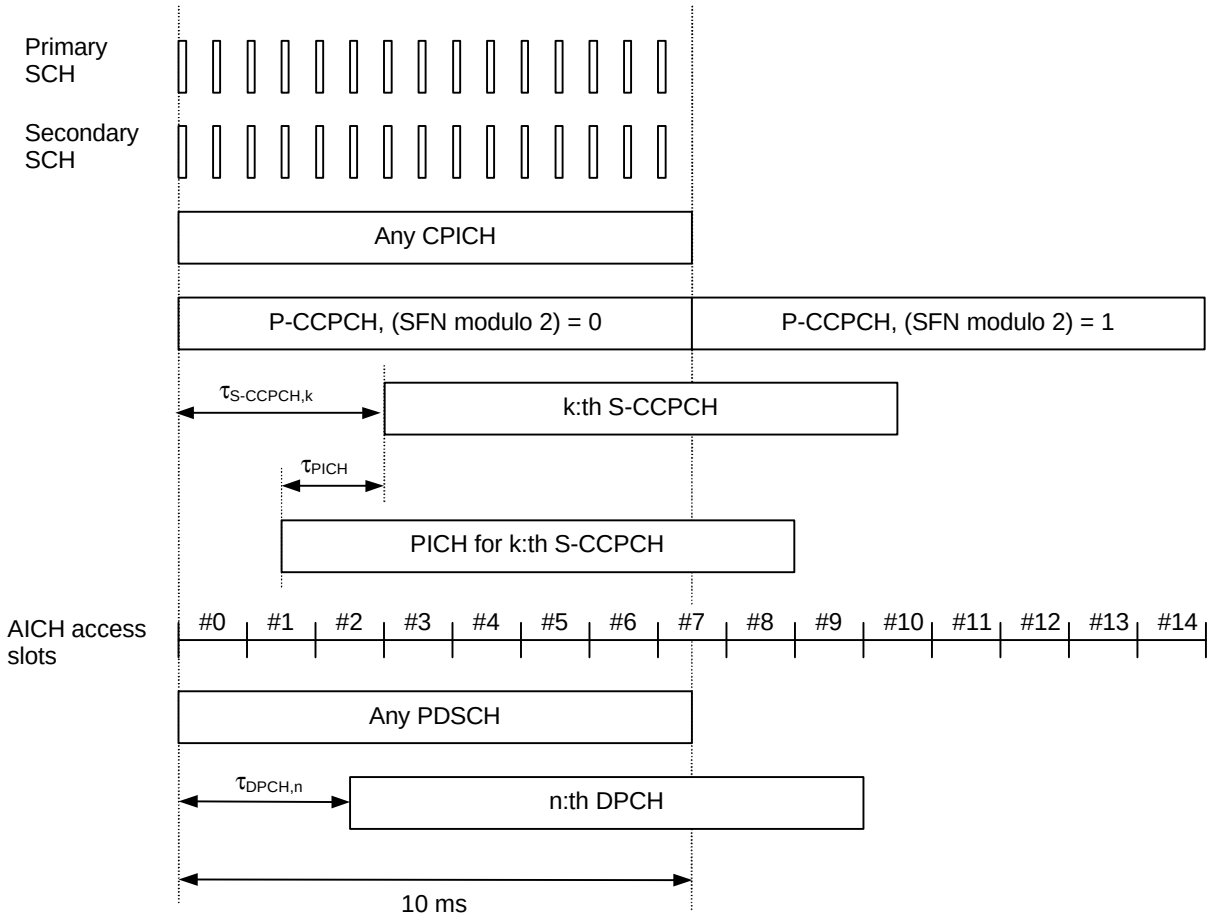

Figure 28: Frame timing and access slot timing of downlink physical channels

The following applies:

- SCH (primary and secondary), CPICH (primary and secondary), P-CCPCH, and PDSCH have identical frame timings.
- The S-CCPCH timing may be different for different S-CCPCHs, but the offset from the P-CCPCH frame timing is a multiple of 256 chips, i.e. $\tau_{S\text{-}CCPCH,k} = T_k \times 256$ chip, $T_k \in \{0, 1, \ldots, 149\}$.
- The PICH timing is $\tau_{PICH} = 7680$ chips prior to its corresponding S-CCPCH frame timing, i.e. the timing of the S-CCPCH carrying the PCH transport channel with the corresponding paging information, see also subclause 7.2.
- AICH access slots #0 starts the same time as P-CCPCH frames with (SFN modulo 2) = 0. The AICH/PRACH and AICH/PCPCH timing is described in subclauses 7.3 and 7.4 respectively.

- The relative timing of associated PDSCH and DPCH is described in subclause 7.5.
- The DPCH timing may be different for different DPCHs, but the offset from the P-CCPCH frame timing is a multiple of 256 chips when SF < 512 or 512 chips when SF = 512, i.e. $\tau_{DPCH,n} = T_n \times 256$ chip, $T_n \in \{0, 1, \ldots, 149\}$ when SF < 512 or $T_n \in \{0, 2, 4\ldots, 148\}$ when SF = 512. The DPCH (DPCCH/DPDCH) timing relation with uplink DPCCH/DPDCHs is described in subclause 7.6.

7.2 PICH/S-CCPCH timing relation

Figure 29 illustrates the timing between a PICH frame and its associated S-CCPCH frame, i.e. the S-CCPCH frame that carries the paging information related to the paging indicators in the PICH frame. A paging indicator set in a PICH frame means that the paging message is transmitted on the PCH in the S-CCPCH frame starting τ_{PICH} chips after the transmitted PICH frame. τ_{PICH} is defined in subclause 7.1.

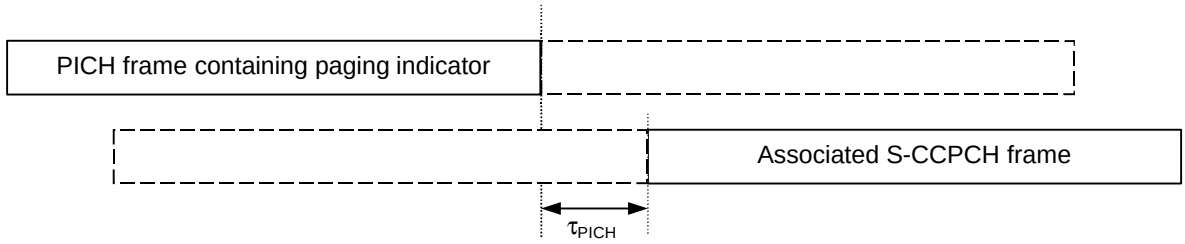

Figure 29: Timing relation between PICH frame and associated S-CCPCH frame

7.3 PRACH/AICH timing relation

The downlink AICH is divided into downlink access slots, each access slot is of length 5120 chips. The downlink access slots are time aligned with the P-CCPCH as described in subclause 7.1.

The uplink PRACH is divided into uplink access slots, each access slot is of length 5120 chips. Uplink access slot number *n* is transmitted from the UE $\tau_{p\text{-}a}$ chips prior to the reception of downlink access slot number *n*, *n* = 0, 1, …, 14.

Transmission of downlink acquisition indicators may only start at the beginning of a downlink access slot. Similarly, transmission of uplink RACH preambles and RACH message parts may only start at the beginning of an uplink access slot.

The PRACH/AICH timing relation is shown in figure 30.

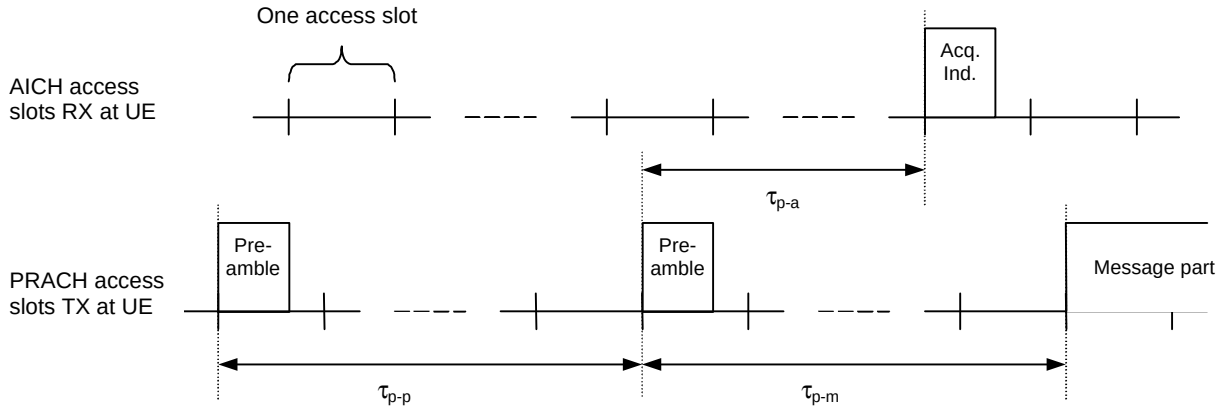

Figure 30: Timing relation between PRACH and AICH as seen at the UE

The preamble-to-preamble distance $\tau_{p\text{-}p}$ shall be larger than or equal to the minimum preamble-to-preamble distance $\tau_{p\text{-}p,min}$, i.e. $\tau_{p\text{-}p} \geq \tau_{p\text{-}p,min}$.

In addition to $\tau_{p\text{-}p,min}$, the preamble-to-AI distance $\tau_{p\text{-}a}$ and preamble-to-message distance $\tau_{p\text{-}m}$ are defined as follows: