TSG-RAN Working Group 1 meeting #14
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Agenda item: Release 2000 issues
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Title: UE battery life improvement with DPCCH gating
Document for: Discussion

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1. Introduction

In our last contribution on DPCCH gating, R1-00-0686, we showed some rough calculations what would be the percentage of time that the DPCCH gating could be on during the connection.

The calculations showed that with DCH only case in downlink the gating could be on about 30 % of the time , and with DCH+DSCH case it could be on about 66 % of the time. The reason why the percentage is bigger for DCH + DSCH case is that it is probable that in that case the DCH, carrying DPCCH, is transmitted with quite high spreading factor, in which case the connection release time can be larger.

In this contribution following issues are discussed:

- Simulation results :
  - Can uplink gating be on during downlink packet transmission, meaning how much downlink performance would be degraded during uplink gating. These simulations were done, since in offline discussions in last meeting, we got a comment, that maybe uplink DPCCH gating could be on all the time during the connection. These simulations however show that this is not feasible – we still think that the gating should be turned on only when there is longer DTX period in downlink.

  - Downlink performance during DTX. Is there big performance difference if only uplink gating is used, or both, uplink and downlink gating. The simulation results show that there is not a big difference.

- UE battery life increasement calculations. These were done with the assumption that gating can be used 30 % (DCH) or 66% (DCH+DSCH) of the time during the connection . These show that there is clear improvement in UE battery life due to gating in DCH+DSCH case.

- First draft proposal for Technical report contents on DPCCH gating

2. Simulation results

2.1 Can uplink gating be on during downlink packet transmission

In last WG1 meeting, one comment in offline discussions was that maybe the gating could be on all the time in uplink. That maybe the downlink performance would be not degraded too much because of that. We investigated this possibility by simulating downlink performance when power control rate would be 500 Hz (1/3 gating) or 300 Hz (1/5 gating).

The simulation parameters were following:

- Geometry factor G=0, 6 and 9dB
- Rayleigh fading one path channel model with UE speed of 3 km/h
- Target BLER 1% (probably for packet data BLER is higher, but should not affect the relative perf. figures so much)
- 12.2 kbit/s
- power control delay :
  - 1 slot. This means that DPCCH gating is not used in downlink (of course not during downlink packet transmission), only in uplink.

Figure 1 shows the simulation results. The performance degradations due to gating in different cases is gathered into table 1.

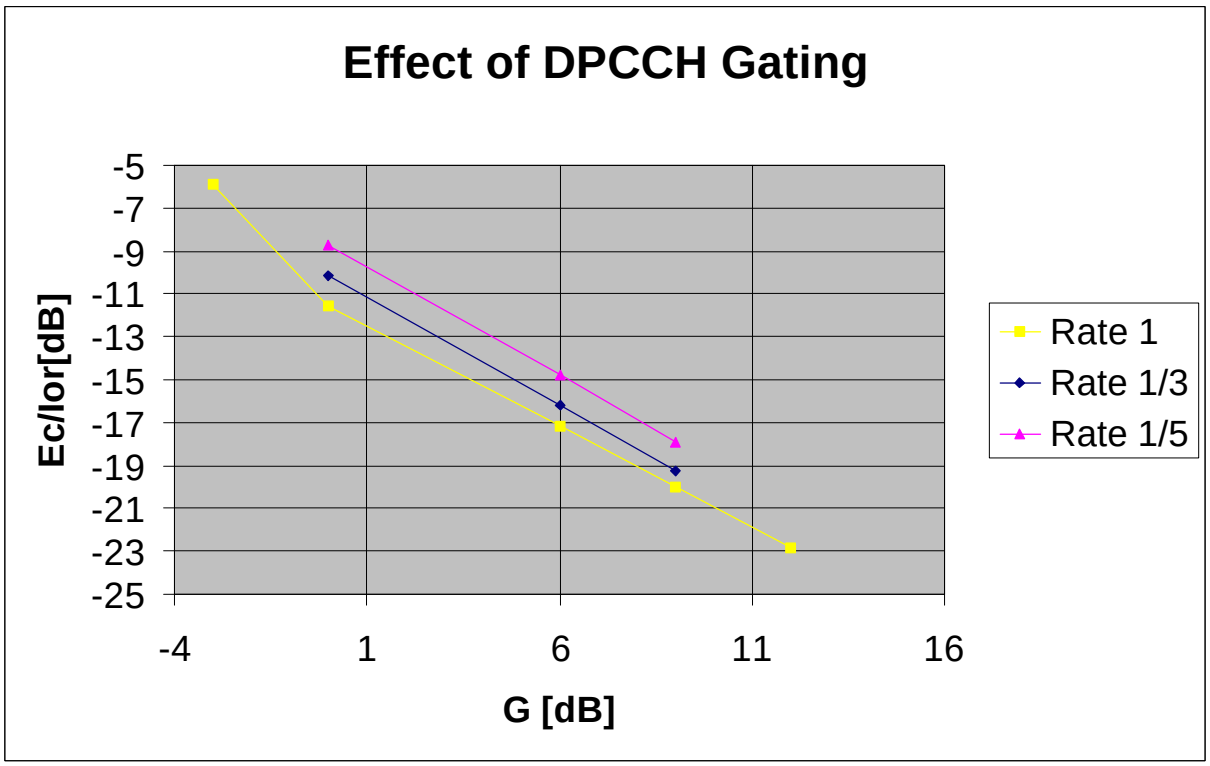

Figure 1. Downlink performance when uplink gating is on. Power control delay =1 slot, meaning that DPCCH gating is not used in downlink.

Gating ratio	Downlink performance degradation
1/3	0.9 dB
1/5	2.4 dB

Table 1. Downlink performance degradation in Ec/Ior due to uplink gating.

The results show that downlink performance degradation is quite high, that we don't think that it is feasible to keep the uplink gating on at the same time the packets are transmitted in downlink.

Thus the scenario how the gating should be used is only during longer DTX period in downlink, just as we suggested already in our previous contribution. When sending only DPCCH , it is not so critical if power control performance is not optimum, since DPCCH power level can be quite small, thus reserving not so much capacity.

2.2. Downlink performance during downlink DTX period

If the DPCCH gating is turned on during longer downlink DTX period, then there are two possibilities. Either only uplink gating is used, or both uplink & downlink gating is used. If only uplink gating is used, then power control delay can be 1 slot, and the results in figure 1 are valid. If both uplink and downlink DPCCH gating are used , then power control delay is 2 slots with 1/3 gating , and 3 slots with 1/5 gating.

Figure 2 shows simulation results for the case where longer power control delays are taken into account assuming simultaneous uplink & downlink gating.

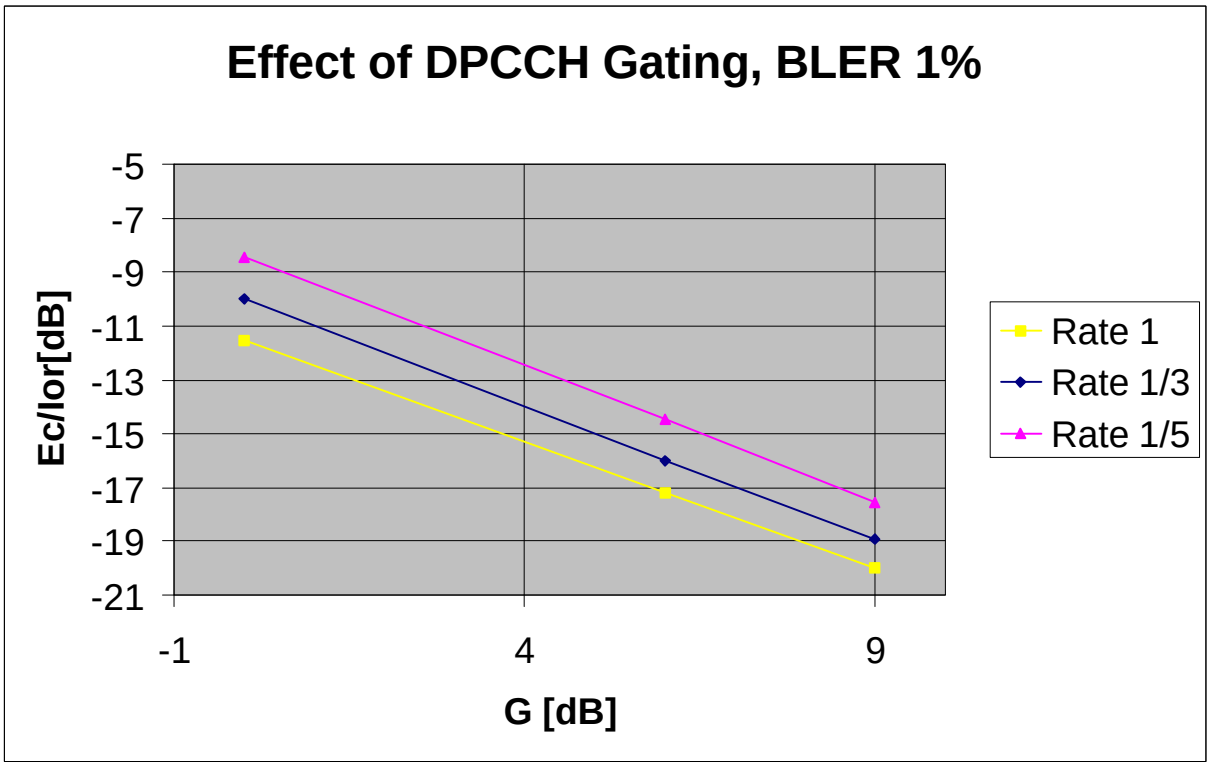

Figure 2. Downlink performance when gating is on. Power control delay =2 slots for 1/3 gating and 3 slots for 1/5 gating, meaning that both uplink and downlink DPCCH gating is used at the same time.

Gating ratio	Uplink gating	Uplink and downlink gating	Difference
1/3	0.9 dB	1.1 dB	0.2 dB
1/5	2.4 dB	2.7 dB	0.3 dB

Table 2. Downlink performance degradation in Ec/Ior .

Table 2 shows that the performance degradation due to longer power control delay is quite negligible, only 0.2 …0.3 dB. Thus it should be thought about whether only uplink gating would be used or uplink + downlink DPCCH gating at the same time. Either one looks quite feasible, since data rate is anyway quite low.

3. UE battery life improvement calculations

In the earlier analysis from Samsung , R1-99-669, it has been calculated that UE battery life can be increased by 32 % by 1/4 gating. That analysis was based on the assumption that DPCCH gating would be used about 70 % of the time during the connection.

We have made also some analysis about the UE battery life improvement due to DPCCH gating, which show similar results. Table 3 and 4 show UE battery lifetime improvements for DCH and DCH+DSCH case, for medium range tx pwr level and high tx power level, respectively.

	Percentage of time gating is on (R1-00-0686) during the connection	Gating rate	UE battery life improvement
DCH	30 %	1/3	8 %
		1/5	13 %
DCH+DSCH	66 %	1/3	21 %
		1/5	34 %

Table 3. UE battery life improvement due to gating, with medium range tx power level.

	Percentage of time gating is on (R1-00-0686) during the connection	Gating rate	UE battery life improvement
DCH	30 %	1/3	10 %
		1/5	16 %
DCH+DSCH	66 %	1/3	26 %
		1/5	44 %

Table 4. UE battery life improvement due to gating, with maximum tx power level.

4. Conclusion and way forward

Our analysis shows that there are clear benefits from DPCCH gating for UE battery life. We see that it is important to try to improve the UE battery life in WCDMA, since it will bring clear benefits to the end user and enhance the usage of services.

Thus we suggest that a Technical report on DPCCH gating is produced for WG1 #15 meeting, including the changes needed for physical layer specifications and other working groups. Then the decision whether TSG RAN WG1 supports the addition of such a feature can be done in WG1#15 which allows to provide the TR for TSG RAN#9 for co-ordination with other WGs (as TSG RAN approval is needed for a study item to proceed to a CR phase) If WG1 conclusions are positive (in WG1#15) the other working groups are informed and enquired do they want to cover their part in a TR of their own or not. Final CRs would then need to be available for TSG RAN#10 (for all TSG RAN WGs impacted).

5. First draft ideas for the contents of TR on DPCCH gating

Following issues could be listed for WG1, to be specified

1) Parameterisation of DPCCH gating

To be included

- gating rates: 1, 1/3, 1/5

Open issues to be decided:

- do we need both random and regular gating pattern, or can we specify only one of them, e.g. random pattern, since that is anyway needed for EMC reasons
- should we have uplink gating only, or simultaneous uplink and downlink gating

2) Definition / generation of patterns

- e.g. text proposal shown in the R1-00-0505 from Samsung

3) Method how is it detected that DPDCH is transmitted after DTX & gating period

Open issue to be decided

- last year in R1-99-870 from Samsung, it was proposed that pilot energy comparison is used. Meaning that pilot energy in all slots in the frame is compared to pilot energy in those slots that contain pilot during gating. If this is above threshold, it means that DTX period has ended. Simulation results were shown that this method works pretty well.
- If no other method is introduced, this could be adopted.

4) TX diversity and DPCCH gating

Open issue to be decided:

It should be noted that when uplink gating is turned on during longer DTX period, it means that also TX diversity feedback signaling is affected. We think that this is acceptable during DTX , since nothing except DPCCH is transmitted in downlink. Thus TX diversity performance is still working , but somewhat degraded performance.

Our understanding is that feedback signaling for mode 1 will work without changes. For mode2, one solution could be e.g. that during gating, mode1 is used.

What needs to be specified, is how NodeB filters the feedback commands during gating.

Following issues could be listed for WG2/ WG3, to be specified

1) Parameterisation of DPCCH gating

To be included

- gating rates: 1, 1/3, 1/5

Open issue:

- both random and regular gating or only one of them

2) Signaling for turning the gating on

- this needs to be specified both in WG2 and WG3

3) Signaling for turning the gating off

Open issue:

Is RRC signaling needed for signaling this to the UE ? Maybe the pilot energy comparison could (or some other method) be some kind of implicit signaling for the UE , to command it to turn the gating off.

4) Anything else?