TSG-RAN Working Group 1 AdHoc 21 **TSGR1(00)0830**

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Agenda Item: AH21
Source: CWTS
To: TSG RAN WG1
Title: Timeslot Formats
Document for: Discussion and Approval

Introduction

This paper describes timeslot formats for low chip rate TDD option.

Conclusion

It's proposed to discuss and include the following text proposal into the clause 7.2.2.2.3 Timeslot formatsTR25.928.

---------- changes to TR25.928 begin ----------

7.2.2.2.3 Timeslot formats

[Description:]

The timeslot format depends on the spreading factor, midamble length, the TPC and SS signals presence and on the number of the TFCI bits. In the case that L1 signals is used, different amount of bits are mapped to the two data fields. In our contributions "transmission of TPC/SS", there are three possible configurations for the number of TPC/SS symbols:

1. 1 symbol TPC and 1 symbol SS
2. No TPC and No SS.
3. 16/SF symbol TPC and 16/SF symbol SS.

So, in case 3 , when SF=1 , the number of TPC/SS is 16 symbol corresponding 32 bits (for QPSK) and 48 bits (for 8PSK).

16/SF TPC/SS symbols is for the case that the number of L1 signalling bits of one given RU after spreading are same although different SFs are used. Thus, the mapping of user data on the payload can stay the same regardless what the spreading factor is.

The timeslot formats are depicted in the following subclause.

[Rational:]

7.2.2.2.3.1 Timeslot formats for Downlink

Table 1: Time slot formats for the Downlink

Slot Format #	Spreading Factor	Midamble length (chips)	N_{TFCI} (bits)	N_{SS} & N_{TPC} (bits)	Bits/slot	$N_{Data/Slot}$ (bits)	$N_{data/data\ field(1)}$ (bits)	$N_{data/data\ field(2)}$ (bits)
0	16	144	0	0 & 0	88	88	44	44
1	16	144	4	0 & 0	88	84	42	42
2	16	144	8	0 & 0	88	80	40	40
3	16	144	16	0 & 0	88	72	36	36
4	16	144	32	0 & 0	88	56	28	28
5	16	144	0	2 & 2	88	84	44	40
6	16	144	4	2 & 2	88	80	42	38
7	16	144	8	2 & 2	88	76	40	36
8	16	144	16	2 & 2	88	68	36	32
9	16	144	32	2 & 2	88	52	28	24
10	1	144	0	0 & 0	1408	1408	704	704
11	1	144	4	0 & 0	1408	1404	702	702
12	1	144	8	0 & 0	1408	1400	700	700
13	1	144	16	0 & 0	1408	1392	696	696
14	1	144	32	0 & 0	1408	1376	688	688
15	1	144	0	2 & 2	1408	1404	704	700
16	1	144	4	2 & 2	1408	1400	702	698
17	1	144	8	2 & 2	1408	1396	700	696
18	1	144	16	2 & 2	1408	1388	696	692
19	1	144	32	2 & 2	1408	1372	688	684
20	1	144	0	32 & 32	1408	1344	704	640
21	1	144	4	32 & 32	1408	1340	702	638
22	1	144	8	32 & 32	1408	1336	700	636
23	1	144	16	32 & 32	1408	1328	696	632
24	1	144	32	32 & 32	1408	1312	688	624

7.2.2.2.3.2 Timeslot formats for Uplink

Table 2: Time slot formats for the Uplink

Slot Format #	Spreading Factor	Midamble length (chips)	N_{TFCI} (bits)	N_{SS} & N_{TPC} (bits)	Bits/slot	$N_{Data/Slot}$ (bits)	$N_{data/data\ field(1)}$ (bits)	$N_{data/data\ field(2)}$ (bits)
0	16	144	0	0 & 0	88	88	44	44
1	16	144	4	0 & 0	88	84	42	42
2	16	144	8	0 & 0	88	80	40	40
3	16	144	16	0 & 0	88	72	36	36
4	16	144	32	0 & 0	88	56	28	28
5	16	144	0	2 & 2	88	84	44	40
6	16	144	4	2 & 2	88	80	42	38
7	16	144	8	2 & 2	88	76	40	36
8	16	144	16	2 & 2	88	68	36	32
9	16	144	32	2 & 2	88	52	28	24
10	8	144	0	0 & 0	176	176	88	88
11	8	144	4	0 & 0	176	172	86	86
12	8	144	8	0 & 0	176	168	84	84
13	8	144	16	0 & 0	176	160	80	80
14	8	144	32	0 & 0	176	144	72	72
15	8	144	0	2 & 2	176	172	88	84
16	8	144	4	2 & 2	176	168	86	82
17	8	144	8	2 & 2	176	164	84	80
18	8	144	16	2 & 2	176	156	80	76
19	8	144	32	2 & 2	176	140	72	68
20	8	144	0	4 & 4	176	168	88	80
21	8	144	4	4 & 4	176	164	86	78
22	8	144	8	4 & 4	176	160	84	76
23	8	144	16	4 & 4	176	152	80	72
24	8	144	32	4 & 4	176	136	72	64
25	4	144	0	0 & 0	352	352	176	176
26	4	144	4	0 & 0	352	348	174	174
27	4	144	8	0 & 0	352	344	172	172
28	4	144	16	0 & 0	352	336	168	168
29	4	144	32	0 & 0	352	320	160	160
30	4	144	0	2 & 2	352	348	176	172

Slot Format #	Spreading Factor	Midamble length (chips)	N_{TFCI} (bits)	N_{SS} & N_{TPC} (bits)	Bits/slot	$N_{Data/Slot}$ (bits)	$N_{data/data\ field(1)}$ (bits)	$N_{data/data\ field(2)}$ (bits)
31	4	144	4	2 & 2	352	344	174	170
32	4	144	8	2 & 2	352	340	172	168
33	4	144	16	2 & 2	352	332	168	164
34	4	144	32	2 & 2	352	316	160	156
35	4	144	0	8 & 8	352	336	176	160
36	4	144	4	8 & 8	352	332	174	158
37	4	144	8	8 & 8	352	328	172	156
38	4	144	16	8 & 8	352	320	168	152
39	4	144	32	8 & 8	352	304	160	144
40	2	144	0	0 & 0	704	704	352	352
41	2	144	4	0 & 0	704	700	350	350
42	2	144	8	0 & 0	704	696	348	348
43	2	144	16	0 & 0	704	688	344	344
44	2	144	32	0 & 0	704	672	336	336
45	2	144	0	2 & 2	704	700	352	348
46	2	144	4	2 & 2	704	696	350	346
47	2	144	8	2 & 2	704	692	348	344
48	2	144	16	2 & 2	704	684	344	340
49	2	144	32	2 & 2	704	668	336	332
50	2	144	0	16 & 16	704	672	352	320
51	2	144	4	16 & 16	704	668	350	318
52	2	144	8	16 & 16	704	664	348	316
53	2	144	16	16 & 16	704	656	344	312
54	2	144	32	16 & 16	704	640	336	304
55	1	144	0	0 & 0	1408	1408	704	704
56	1	144	4	0 & 0	1408	1404	702	702
57	1	144	8	0 & 0	1408	1400	700	700
58	1	144	16	0 & 0	1408	1392	696	696
59	1	144	32	0 & 0	1408	1376	688	688
60	1	144	0	2 & 2	1408	1404	704	700
61	1	144	4	2 & 2	1408	1400	702	698
62	1	144	8	2 & 2	1408	1396	700	696

Slot Format #	Spreading Factor	Midamble length (chips)	N_{TFCI} (bits)	N_{SS} & N_{TPC} (bits)	Bits/slot	$N_{Data/Slot}$ (bits)	$N_{data/data\ field(1)}$ (bits)	$N_{data/data\ field(2)}$ (bits)
63	1	144	16	2 & 2	1408	1388	696	692
64	1	144	32	2 & 2	1408	1372	688	684
65	1	144	0	32 & 32	1408	1344	704	640
66	1	144	4	32 & 32	1408	1340	702	638
67	1	144	8	32 & 32	1408	1336	700	636
68	1	144	16	32 & 32	1408	1328	696	632
69	1	144	32	32 & 32	1408	1312	688	624

7.2.2.2.3.3 Timeslot formats for 8PSK modulation (both for Uplink and Downlink)

Table 3 Timeslot formats for 8PSK modulation

Slot Format #	Spreading Factor	Midamble length (chips)	N_{TFCI} (bits)	N_{SS} & N_{TPC} (bits)	Bits/slot	$N_{Data/Slot}$ (bits)	$N_{data/data\ field(1)}$ (bits)	$N_{data/data\ field(2)}$ (bits)
0	1	144	0	0 & 0	2112	2112	1056	1056
1	1	144	6	0 & 0	2112	2106	1053	1053
2	1	144	12	0 & 0	2112	2100	1050	1050
3	1	144	24	0 & 0	2112	2088	1044	1044
4	1	144	48	0 & 0	2112	2064	1032	1032
5	1	144	0	3 & 3	2112	2106	1056	1050
6	1	144	6	3 & 3	2112	2100	1053	1047
7	1	144	12	3 & 3	2112	2094	1050	1044
8	1	144	24	3 & 3	2112	2082	1044	1038
9	1	144	48	3 & 3	2112	2058	1032	1026
10	1	144	0	48 & 48	2112	2016	1056	960
11	1	144	6	48 & 48	2112	2010	1053	957
12	1	144	12	48 & 48	2112	2004	1050	954
13	1	144	24	48 & 48	2112	1992	1044	948
14	1	144	48	48 & 48	2112	1968	1032	936
15	16	144	0	0 & 0	132	132	66	66
16	16	144	6	0 & 0	132	126	63	63
17	16	144	12	0 & 0	132	120	60	60
18	16	144	24	0 & 0	132	108	54	54
19	16	144	48	0 & 0	132	84	42	42
20	16	144	0	3 & 3	132	126	66	60
21	16	144	6	3 & 3	132	120	63	57
22	16	144	12	3 & 3	132	114	60	54
23	16	144	24	3 & 3	132	102	54	48
24	16	144	48	3 & 3	132	78	42	36

[Explanation difference:]

Based on the burst structure and the TFCI,SS and TPC control signals, the low chip rate TDD option has a different burst type from that of high chip rate TDD option. When 2M service is transmitted, the timeslot formats are based on 8PSK modulation,. but the timeslot formats in table 3 are not restricted to the use for 2Mbps only..

---------- changes to TR25.928 end ----------