TSG-RAN Working Group 1, Adhoc 21 **TSGR1(00)0820**

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**Agenda Item:** AH21
**Source:** CWTS
**To:** TSG RAN WG1
**Title:** Low chip rate characteristics
**Document for:** Discussion and Approval

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# Introduction

In this paper, the general characteristics for low chip rate TDD are described. These parameters will provide a general introduction and summarization of low chip rate TDD option.

# Conclusion

It is proposed to include the following text into TR25.928.

---------- changes to TR25.928 begin ----------

## 5 High level characteristics

| Parameter/Feature | Value/Expression | Note |
|---|---|---|
| Chip rate | 1.28 Mcps | |
| Modulation | QPSK (8PSK) | |
| Spreading Factor | 1/2/4/8/16 | |
| Nominal Channel Spacing | 1.6MHz / Carrier | |
| Burst Format | 1 burst type | |
| Radio Frame Length | 10ms (divided into 2 sub-frames) | |
| Sub-frame length | 5ms | |
| Time slot number (traffic) | 7 | |
| Time slot length (us) | 675 | |
| Downlink pilot slot (us) | 75 | DwPTS |
| Uplink pilot slot (us) | 125 | UpPTS |
| Guard Period (us) | 75 | GP After DwPTS |
| Range of uplink slot | 1 – 6 | |
| Range of downlink slot | 1 – 6 | |
| Receiver type | Multi-user Detection (option), Rake | |
| Pilot aided detection | DwPTS, UpPTS, Midamble | |
| Synchronization aspect | Downlink and uplink synchronization | |
| Precision for UL sync. | 1/8 chip | |
| Antenna processing | Smart antenna with beam forming | |
| Switching point | Two switching points / sub-frame | |
| Power control / rate | Open loop power control<br>Closed loop power control / 200Hz (max rate) | |

| | | |
|---|---|---|
| Variable bit rate service | Supported (using TFCI) | |
| Basic resource unit | One code, one slot with Spreading factor =16 (use of same resource in both consecutive sub-frames) | |
| Service mapping | Multi-code, multi-slot combination (variable spreading factor) | |
| Interleaving period | 10/20/40/80ms | |
| Intra-system HO | Baton handover (optional) | |
| HO capability | Low chip rate TDD to High chip rate TDD, FDD, GSM, etc. | |
| Tx Diversity | same capability as high chip rate TDD for DwPTS,DPCH, but not for P-CCPCH; the TxDiversity scheme used for the DPCH is used for the FPACH, as well. | Refer to sub clause 10.5 of TR |

---------- changes to TR25.928 end ----------