Agenda	5
Source:	GBT
Subject:	CR023 r6.0 25.211 CPCH-related editorial changes, technical changes and additions and some clarification on PCPCH/AICH timing relation
Document for	Approval

Document is a revision of Tdoc#434

Current document is a revision of Tdoc# 411 which was in turn a revision of Tdoc#336 which was presented to Ad-Hoc 14. Some more comments were received which have been incorporated here.

Please note that Tdocs R1(00)0200 CR023 r2 of 25.211 and R1(00)0203 CR032 of 25.211 have been combined and are replaced by this Tdoc R1(00)0336_CR023 r3

The first revision of this CR partially included most of the changes that GBT proposed in the WG1#9 meeting. These changes were approved pending changing the format of the document. However, GBT has added new items to this CR that have been discussed on the reflector. Specifically several tables have been added to provide the DPDCH and DPCCH fields for the CPCH message part. Also the editorial change of CD-AICH to CD-ICH necessitates introduction of new physical channel which is also proposed in this CR.

TSG Working Group 1 # 11 San Diego, CA, USA, Feb 29 - Mar 3, 2000



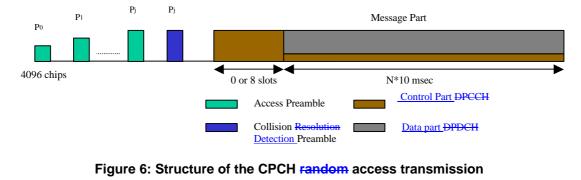
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<u>Other</u> comments:								

3 Abbreviations

For the purposes o	f the present document, the following abbreviations apply:
AI	Acquisition Indicator
AICH	Acquisition Indicator Channel
AP	Access Preamble
BCH	Broadcast Channel
ССРСН	Common Control Physical Channel
CCTrCH	Coded Composite Transport Channel
CD	Collision Detection
CPCH	Common Packet Channel
CPICH	Common Pilot Channel
DCH	Dedicated Channel
DCH DPCCH	Dedicated Channel Dedicated Physical Control Channel
DPCH	Dedicated Physical Control Channel
DPDCH	Dedicated Physical Data Channel
DIDCH	Downlink Shared Channel
DSCH DSMA-CD	Digital Sense Multiple Access – Collison Detection
DTX	Digital Sense Multiple Access – Comson Detection Discontinuous Transmission
FACH	Forward Access Channel
FBI	Feedback Information
MUI	Mobile User Identifier
PCH	Paging Channel
P-CCPCH	Primary Common Control Physical Channel
PCPCH	Physical Common Packet Channel
PDSCH	Physical Downlink Shared Channel
PI	Page Indicator
PICH	Page Indicator Channel
PRACH	Physical Random Access Channel
PSC	Primary Synchronisation Code
RACH	Random Access Channel
RNC	Radio Network Controller
S-CCPCH	
SCH	Secondary Common Control Physical Channel Synchronisation Channel
SF	Spreading Factor
SFN	System Frame Number
SSC	System Prane Runber Secondary Synchronisation Code
STTD	Space Time Transmit Diversity
TFCI	Transport Format Combination Indicator
TSTD	Time Switched Transmit Diversity
TPC	Transmit Power Control
UE	
UTRAN	User Equipment UMTS Terrestrial Radio Access Network
UINAN	UNITS TETTESUTAT RAUTO ACCESS INCLWOIK

5.2.2.2.1 CPCH transmission

The CPCH transmission is based on DSMA-CD approach with fast acquisition indication. The UE can start transmission at <u>the beginning of</u> a number of well-defined time-<u>intervals</u>, relative to the frame boundary of the received BCH of the current cell. The access slot timing and structure is identical to RACH in section 5.2.2.1.1. The structure of the CPCH <u>random</u> access transmission is shown in figure 6. The <u>PCPCH</u> random access transmission consists of one or several Access Preambles [A-P] of length 4096 chips, one Collision Detection Preamble (CD-P) of length 4096 chips, a DPCCH Power Control Preamble (PC-P) which is either 0 slots or 8 slots in length, and a message of variable length Nx10 ms.



5.2.2.2.4 CPCH power control preamble part

The power control preamble segment is <u>called the a DPCCH-CPCH</u> Power Control Preamble (PC-P) <u>part</u>. The following table 9 is identical to Rows 2 and 4 of table 2 in section 5.2.1. Table 9 defines the DPCCH fields which only include Pilot, FBI and TPC bits. The Power Control Preamble length is a parameter which shall take the values 0 or 8 slots, as set by the higher layers.

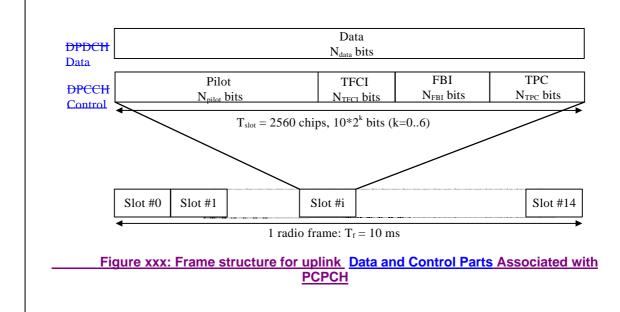
Table 9: DPCCH fields for CPCH	power control preamble segment

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N _{pilot}	N _{tfci}	N _{FBI}	N _{TPC}
0	15	15	256	150	10	8	0	0	2
1	15	15	256	150	10	7	0	1	2

5.2.2.2.5 CPCH message part

Figure 1in section 5.2.1 shows the structure of the CPCH message part. Each message consists of up to N_Max_frames 10 ms frames. N_Max_frames is a higher layer parameter. Each 10 ms frame is split into 15 slots, each of length $T_{slot} = 2560$ chips. Each slot consists of two parts, a data part that carries higher layer information and a control part that carries Layer 1 control information. The data and control parts are transmitted in parallel.

Figure xxx shows the frame structure of the uplink common packet physical channel. Each frame of length 10 ms is split into 15 slots, each of length $T_{slot} = 2560$ chips, corresponding to one power-control period.



The data part consists of $10*2^k$ bits, where k = 0, 1, 2, 3, 4, 5, 6, corresponding to spreading factors of 256, 128, 64, 32, 16, 8, 4 respectively. Note that various rates might be mapped to different signature sequences.

The spreading factor for the UL-DPCCHmessage control part is 256. The entries in table 1 corresponding to spreading factors of 256 and below and table 2 [both in section 5.2.1] apply to the DPDCH _and DPCCH fields respectively for the CPCH message part.

The entries of table 1 in section 5.2.1 apply to the data part of the CPCH message part. The spreading factor for the control part of the CPCH message part shall be 256. The slot format of the control part of CPCH message part shall be the same as the control part of CPCH PC-P. The pilot bit patterns of table 3 and 4 in section 5.2.1 shall be used for pilot bit patterns of the CPCH message part.

5.3.2.3 DL-DPCCH for CPCH

The spreading factor for the <u>PCPCH message control part UL DPCCH (message control part)</u> is 256. The spreading factor for the DL-DPCCH (message control part) is 512. The following table 15 shows the DL-DPCCH fields (message control part) which are identical to the first row of table 11 in section 5.3.2.

Table 15: DPDCH and DPCCH fields for CPCH message transmission

Slot Format	Channel Bit	Channel Symbol	SF	Bits/Frame		Bits/ Slot	DPDCH Bits/Slot		DPCCH Bits/Slot			
#i	Rate (kbps)	Rate (ksps)		DPDCH	DPCCH	тот		NData1	NData2	NTFCI	NTPC	NPilot
0	15	7.5	512	60	90	150	10	2 0	2 4	0	2	4

7.4 PCPCH/AICH timing relation

Transmission of random access bursts on the PCPCH is aligned with access slot times. The timing of the access slots is derived from the received Primary CCPCH timing The transmit timing of access slot n starts $n\times 20/15$ ms after the frame boundary of the received Primary CCPCH, where n = 0, 1, ..., 14. In addition, transmission of access preambles in PCPCH is limited to the allocated access slot subchannel group which is assigned by higher layer signalling to each CPCH set. Twelve access slot subchannels are defined and PCPCH may be allocated all subchannel slots or any subset of the twelve subchannel slots. The access slot subchannel identification is identical to that for the RACH and is described in table 6 of section 6.1 of [5]. Everything in the previous section [PRACH/AICH] applies to this section as well. The timing relationship between preambles follow the access preambles in PCPCH/AICH. However, the timing relationships between CD-Preamble and CD-AICH is identical to RACH Preamble and AICH. The timing relationship between CD-AICH and the Power Control Preamble in CPCH is identical to AICH to message in RACH. The T_{cpch} timing parameter is identical to the PRACH/AICH transmission timing parameter. When T_{cpch} is set to zero or one, the following PCPCH/AICH timing values apply.

Note that a1 corresponds to AP-AICH and a2 corresponds to CD-AICH.

 τ_{p-p} = Time to next available access slot, between Access Preambles.

Minimum time = 15360 chips + 5120 chips X Tcpch

Maximum time = 5120 chips X 12 = 61440 chips

Actual time is time to next slot (which meets minimum time criterion) in allocated access slot subchannel group.

 $\tau_{p-a1} =$ Time between Access Preamble and AP-AICH has two alternative values: 7680 chips or 12800 chips, depending on T_{cpch}

 $\tau_{a1-cdp} = \underline{T}$ ime between receipt of AP-AICH and transmission of the CD Preamble-has one value . $\underline{\tau_{a1-cdp}}$ -has a minimum value of $\underline{\tau_{a1-cdp, min}} = 7680$ chips.

- $\tau_{p-cdp} = \underline{T}$ ime between the last AP and CD Preamble. $\underline{\tau_{p-cdp}}$ has a minimum value of $\underline{\tau_{p-cdp-min}}$ which is either 3 or 4 access slots, depending on T_{cpch}
- $\tau_{cdp-a2} =$ Time between the CD Preamble and the CD-AICH has two alternative values: 7680 chips or 12800 chips, depending on T_{cpch}
- $\tau_{cdp-pcp} =$ Time between CD Preamble and the start of the Power Control Preamble is either 3 or 4 access slots, depending on T_{cpch} .

The message transmission shall start 0 or 8 slots after the start of the power control preamble depending on the length of the power control preamble.

Figure 25 illustrates the PCPCH/AICH timing relationship when T_{cpch} is set to 0 and all access slot subchannels are available for PCPCH.

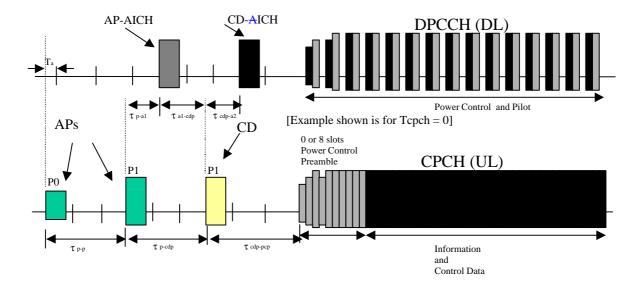


Figure 25: Timing of PCPCH and AICH transmission as seen by the UE, with $T_{\mbox{\scriptsize cpch}}\mbox{=}0$